A 3.3-V 12-b 50-MS/s A/D Converter in 0.6-μm CMOS with over 80-dB SFDR

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***Abstract*—A 12-b analog-to-digital converter (ADC) is optimized for spurious-free dynamic range (SFDR) performance at low supply voltage and suitable for use in modern wireless base stations. The 6–7-b two-stage pipeline ADC uses a bootstrap circuit to linearize the sampling switch of an on-chip sample-and-hold (S/H) and achieves over 80-dB SFDR for signal frequencies up to 75 MHz at 50 MSample/s (MSPS) without trimming, calibration, or dithering. INL is 1.3 LSB, differential nonlinearity (DNL) is 0.8 LSB. The 6-b and 7-b flash sub-ADCs are implemented efficiently using offset averaging and analog folding. In 0.6-μm CMOS, the 16-mm^2 ADC dissipates 850 mW.**

***Index Terms*—A/D converter, analog folding, bootstrap circuit, CMOS analog integrated circuits, IF sampling, spatial filter, spurious-free dynamic range.**

I. Introduction

MODERN wireless base stations digitize the IF band, and separate individual channels with digital filters [1], [2]. Digitizing at IF poses challenges on the design of the analog-to-digital converter (ADC). First, the spurious-free dynamic range (SFDR) must be over 80 dB so that a weak received channel is not confused with the artifacts arising from digitizing strong channels. The SFDR of an ADC is defined as [3] the difference in decibels (dB) between the full-scale (FS) fundamental and the maximum spurious tone in the output spectrum. The signal-to-noise ratio (SNR) is relatively less important here, because of the digital processing gain. Second, the conversion rate must be on the order of 50 Msample/s (MSPS) to accommodate a typical 20-MHz IF band. Third, it is also desirable to maintain a constant SFDR performance beyond the Nyquist input frequency to give more freedom in placing the IF. This requires an on-chip sample-and-hold (S/H) with good dynamic performance. So far, only bipolar and BiCMOS ADCs come close to these specifications [4]–[7], and they all operate from a 5-V supply.

This paper presents a 3.3-V 0.6-μm 50-MSPS CMOS A/D converter demonstrating SFDR greater than 80 dB for input frequencies up to 75 MHz without trimming, calibration, or dithering. The fundamental objective is to develop an efficient (compact and low power) and calibration-free ADC architecture optimized for SFDR. Although 0.6-μm CMOS can operate at 5 V, part of the research was to anticipate the low voltage needs of scaled technologies in the future. After a brief introduction to the fundamentals in Section II, a 12-b two-stage pipeline architecture with a 6–7-b partition is chosen, as described in Section III. Section IV derives the efficient sub-ADCs. Circuit implementation of the major building blocks is described in Section V. Finally, experimental results are discussed in Section VI, followed by conclusions in Section VII.

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II. SFDR: Fundamentals

An n-bit ideal quantizer exhibits a sawtooth error characteristic. With the FS input amplitude normalized to one (FS/2 = 1), the periodic error function is parameterized with its frequency $\omega_x = 2\pi/\text{LSB} = 2^n\pi$, where the least significant bit (LSB) represents the quantization step. The error distorts an FS input sinewave and creates wideband harmonics, with significant spectral energy up to the order of ω_x. The Fourier series of either the quantized sinewave or the periodic sawtooth error function lead to closed-form expressions for the harmonics [8]–[11] and plots of distortion spectra as shown in Fig. 1(a). The plots for various n show that the largest harmonic is located near ω_x, and is about $9n$ dB below the fundamental, that is

$$k_{\max} \approx \omega_x = 2^n\pi \tag{1}$$

and

$$\text{SFDR} \approx 9n - c \quad \text{(dB)} \tag{2}$$

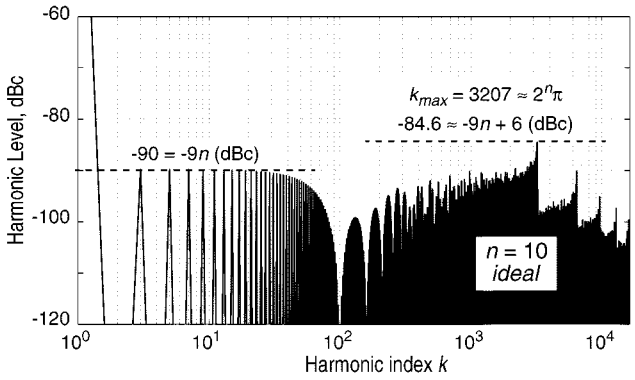
where $k_{\max}$ is the index of the largest harmonic and the offset c ranges from 0 for low resolutions to 6 for high resolutions [10].

Though strict validation of these empirical equations is mathematically interesting, it gives better insight to derive (2) from energy conservation. As n increases by one, the quantization error is halved in amplitude, and the total error energy LSB^2/12, which is *asymptotically independent* of the signal distribution [12]–[15], decreases by 6 dB. This leads to the signal-to-noise-and-distortion ratio (SNDR)

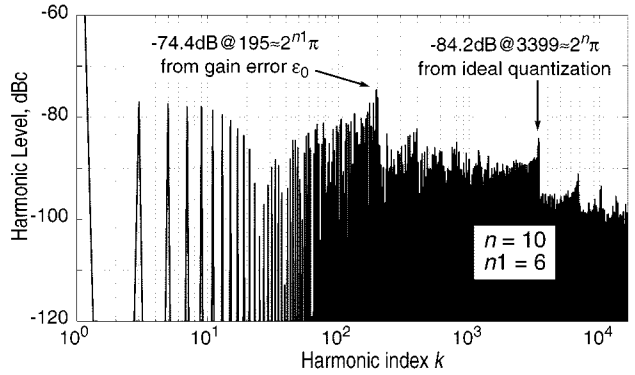
$$\text{SNDR} = 6n + 1.76 \quad \text{(dB)}. \tag{3}$$

Also, now the error sawtooth at double the frequency produces twice as many important harmonics, so the overall spur level must go down by an additional 3 dB to keep the total harmonic energy unchanged, resulting in the $9n$ term in (2). This suggests that the key to high SFDR should be to spread a given error energy across as large a number of spurs as possible.

Imperfections in real ADCs add errors. The linear superposition of those error characteristics on the ideal quantization approximates the overall quantization error to the first order. For example, interstage gain error ε in a two-stage pipeline ADC contributes a sawtooth error [16] of frequency $\omega_{x1} = 2^{n1}\pi$, and



(a)



(b)

Fig. 1. Spectra of quantized sinewave. (a) Ideal 10-b quantizer. (b) 10-b two-stage ADC with 6-b in the first stage and interstage gain error $\varepsilon = \varepsilon_0 = 2^{-4}$.

amplitude $(\varepsilon/2\varepsilon_0)$ LSB, where $n1 =$ the bit number of the first stage, and $\varepsilon_0 = 2^{-(n-n1)}$. This error function generates spurs that resemble an $n1$-bit ideal quantization [except for an offset of 20 $\log\varepsilon$ (dB) in the spur level] and these superimpose on the n-bit ideal quantization. The superposition is clearly seen in Fig. 1(b) which plots the fast Fourier transform (FFT) of the output of a two-stage (n = 10 and $n1$ = 6) ADC programmed in Matlab oversampling a sinewave of frequency f_{in} at conversion rate f_s, with $\varepsilon = \varepsilon_0$. The oversampling ratio $f_s/(2f_{in})$ is set much larger than $N = 2^n$ to prevent aliasing which scrambles the superposition. Therefore, the SFDR dominated by interstage gain error is given by

$$\text{SFDR} \approx (9n1 - c) - 20\log\varepsilon \tag{4}$$

with the maximum spur located at

$$k_{\max} \approx 2^{n1}\pi. \tag{5}$$

Unlike the asymptotically constant quantization error energy, spurs are sensitive to the waveform being quantized. For example, an ideal quantization of an FS sawtooth input signal leads to a sawtooth error waveform which contains spurs much higher than what is given by (2); a tiny deviation ($\sim$LSB/4) from FS amplitude may null some low-order harmonics. The largest spur rises by 3 dB for each 6-dB reduction in input amplitude, because the input signal sees half of the error sawtooth spreading the same amount of spur energy. This contradicts the "common sense" that nonlinearity improves as signal decreases in power.

TABLE I
SFDR AND SNDR VERSUS FIRST-STAGE RESOLUTION ($n1$) FOR 12-b TWO-STAGE PIPELINE ADCS WITH THE ONLY IMPERFECTION OF INTERSTAGE GAIN ERROR $\varepsilon_0 = 2^{-(n-n1)}$

$n1$	ε_0	SNDR (dB)	SFDR (dB) simulated	SFDR (dB) from Eq. (4)
1	2^{-11}	72.1	79.6	75 - c
2	2^{-10}	71.3	79.6	78 - c
3	2^{-9}	71.0	81.5	81- c
4	2^{-8}	70.9	83.1	84 - c
5	2^{-7}	70.9	86.3	87 - c
6	2^{-6}	70.9	88.3	88 - c

As a result, small-signal SFDR gets worse and a few bits of margin is required over what (2) specifies to determine the resolution. In addition, the spurs can be drastically affected by the noise (dither) at the input and the sampling frequency. Those details are discussed in [11].

III. ARCHITECTURE CHOICE

From the foregoing, over 80-dB SFDR requires at least 12-b resolution allowing a margin of about 2 b. With a 1-V FS, this implies an LSB size more than one order of magnitude smaller than, say, 10-mV offset [17], [18] in CMOS comparators. There are two logical solutions: either reduce the offsets, or amplify the signal prior to comparison. This converter amplifies the residue, because it not only effectively amplifies the FS without running into headroom problem, but it also allows distribution of overall quantization across multiple stages.

The 1.5-b/stage of quantization and residue amplification in a pipeline is commonly used [19] to implement a binary search. As ADC resolution increases, this algorithmic efficiency becomes increasingly important. Also, the two-level (or three-level differential) interstage reconstruction digital-to-analog converter (DAC) is inherently perfectly linear. However, our numerical investigation shows that inaccuracy in the interstage gain of the front-end stages in this type of ADCs is the bottleneck to both SFDR and SNDR. The first residue amplifier gain must be accurate to better than 0.05% in a 1.5-b/stage 12-b ADC for the target 80-dB SFDR (see Table I). This is difficult to realize with switched-capacitor (SC) amplifiers due to imperfections such as mismatch between the sampling and feedback capacitors, finite dc gain of the operational transconductance amplifier (OTA), and the parasitic capacitance between the input and output nodes. Trimming or calibration [20]–[25] is usually necessary. Incomplete settling of the amplifier output at high clock frequencies can not be easily calibrated, and as error concentrates in a few tones, it is characteristic of these ADCs that SFDR degrades rapidly at high conversion rates.

Fig. 2 shows the top-level block diagram of the implemented A/D converter. Allotting 6-b to the first stage relaxes the interstage gain accuracy. As a result, SFDR of 88 dB requires only 1.6% accuracy in the interstage gain (see Table I). For higher bandwidth, the interstage gain of 2^5 is realized with a pipelined cascade of five similar $2\times$ SC amplifiers. Since the (percentage)

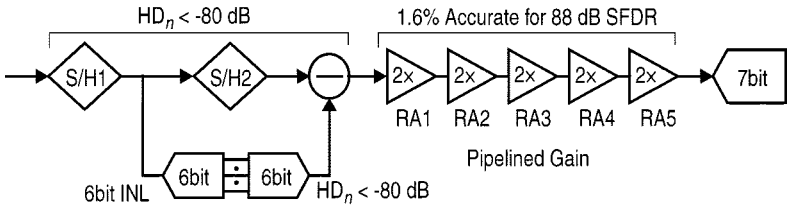


Fig. 2. 12-b two-stage pipeline ADC block diagram.

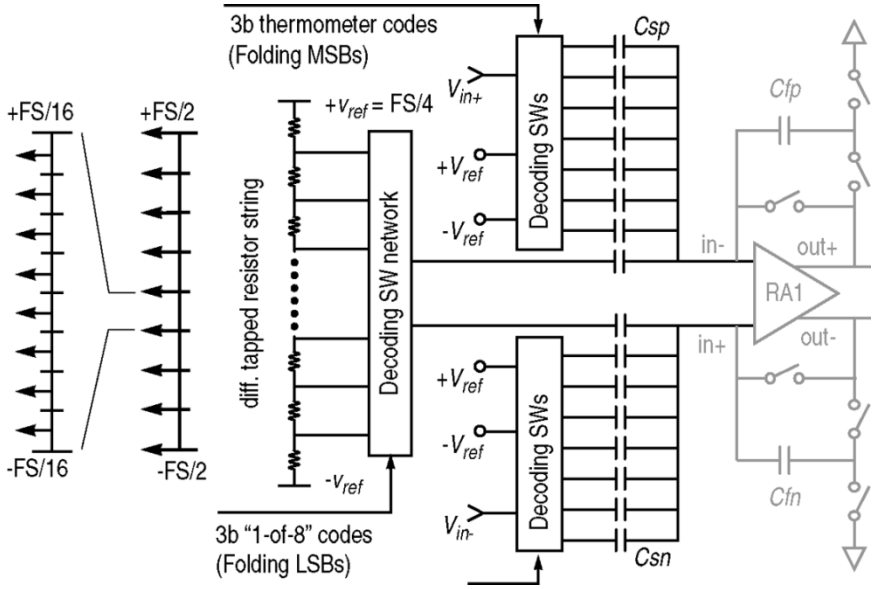


Fig. 3. Two-step hybrid reconstruction DAC block diagram.

gain errors cumulate linearly, each amplifier on average needs to be accurate to $\pm 1.6\%/5 \sim \pm 0.32\%$, which is possible without calibration or trimming.

The DAC must be nominally 12-b linear to meet 12-b SNDR, although this is somewhat relaxed in terms of SFDR requirement because the higher resolution of the first-stage quantization spreads the random error in the DAC across more harmonics. Fig. 3 shows the two-step hybrid DAC used. It consists of an eight-capacitor array (differential) and a fine interpolating resistor ladder, driven by the coarse 3-b thermometer codes and the fine 3-b 1-of-8 codes, respectively, from the first-stage 6-b folding ADC. Capacitor matching dominates the DAC linearity; the resistor ladder can be 3-b less accurate. In terms of spreading errors across more spurs, the 3b–3b configuration is not as effective as the 6-b fully segmented. However, the reduced complexity eases layout matching. Monte Carlo simulations show that 3-sigma yield of 80-dB SFDR requires about 230 ppm matching in the total DAC capacitance $(C_{sp} + C_{sn})$, which is chosen to be 8 pF based on the published data on capacitor matching [53]. It can be shown that with this level of capacitor matching, the 1.5-b/stage counterpart yields less than 3-sigma in SFDR. Well-thought-out capacitor layout is essential to avoid systematic mismatch.

The harmonics HD$_n$ $(n = 2, 3, \cdots)$ in the S/Hs must be kept below -80 dB. S/H2 pipelines the latch regeneration in the AD-DA critical path, and the 6-b sub-ADC must be low latency. The second-stage 7-b sub-ADC reuses the 6-b design. Both ADCs are made compact with folding and interpolation [26]–[33], accompanied by offset averaging [34], [33].

IV. Efficient Sub-ADCs

Low-latency flash sub-ADCs require large amounts of hardware. How to make efficient ADCs with the low latency of flash is the subject of this section.

A. Analog Folding

A generic flash ADC consists of zero-crossing (ZX) generators (e.g., difference amplifiers), ZX detectors (e.g., regenerative latches), and an encoder. To reduce complexity by F times, an F-to-1 mapping function precedes the ADC. A compact coarse quantizer resolves the ambiguity in the many-to-one mapping. In the signal path, the F-to-1 folds the signal while preserving the overall linearity [36], [37]. Rectifying devices that fold the signal are not as easy to realize in CMOS as with bipolar circuits [4], [38]–[41].

A compromise is to map F-to-1 *after* the ZX generators but before the detectors. Now, the F-to-1 mapping is on discrete ZXs and requires no linearity. This amounts to the multiplexing of the ZXs. Fig. 4(a) shows such a case where only the group of ZXs in which the input falls is multiplexed for detection. The coarse quantizer identifies the group and activates the multiplexer (MUX). This architecture is *serial*, because the MUX

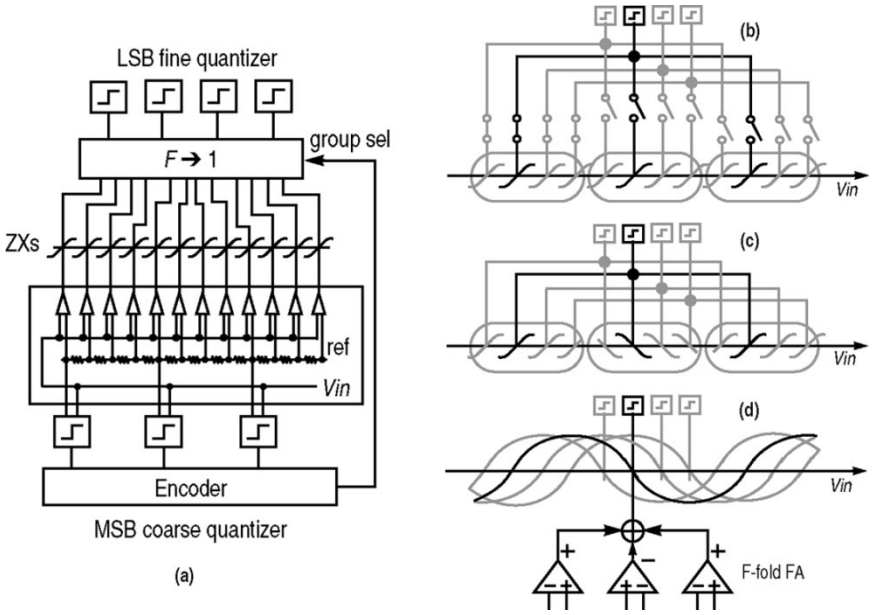


Fig. 4. Multiplexing of ZXs. (a) Modified flash ADC. (b) SW MUX. (c) Auto MUX. (d) Folding.

waits for the coarse decision. To preserve the flash-like nature, this latency must be removed by automating the MUX.

Fig. 4(b) shows the MUX realized as switches. However, the switches can be bypassed if the signals from the groups away from the zerocrossing cancel each other. Cancellation happens when the ZXs of each adjacent group are reversed in polarity and peg at the same level [Fig. 4(c)]. The flipped polarity does not change the result of the fine quantization because the cut point of the thermometer codes remains the same. Now, the multiplexer is automatic; the ZXs (characteristics) merge into the folding characteristic [Fig. 4(d)], which is referred to as ZX *folding*, to distinguish from the signal folding aforementioned.

The folding is therefore the automatic multiplexing of ZXs, and it realizes a *multi-step flash* ADC [11]. Signals may be folded in many ways. The method described above sums an odd number of ZXs of alternative polarity [30]. The summation can be realized in two steps: subtotal first and then grand total, leading to the summation-based cascaded folding [33]. This gives the advantage that less parasitics and mismatch in tail currents aggregate at the merging node.

Folding multiplies the input signal frequency and the folding signal may exceed the bandwidth of the folding circuit. This ceases to be a problem when a S/H provides a dc-like input to the folding amplifiers, such as in the sub-ADCs in this pipeline architecture.

B. Interpolation and Averaging

Interpolation and averaging lower the number and size of the ZX generators [33]. In the commonly used voltage interpolation, a resistive voltage divider connects the output of each adjacent ZX generator. Often the buffers driving the interpolating network set the interpolating ZX voltages [30], [31]. With sufficient dummies extending the array, the buffers can be removed, because the interfering signals cancel each other and the ZXs within the FS are not disturbed. Without the buffers, the interpolation turns into the offset averaging [34].

In this work, offset averaging is optimized based on *spatial filtering*. Fig. 5 shows an infinite preamp array with the lateral resistors $R1$ inserted for offset averaging. The load impedance $R0$ of the preamps and the averaging resistors $R1$ form a spatial filter with impulse response [35]

$$h(n) = h(0)b^{|n|}, \quad b = e^{-|\operatorname{acosh}(1+R_1/2R_0)|} \tag{6}$$

where the node index $n = 0, \pm 1, \pm 2, \cdots$. The input differential-pair g_m stages provide the stimuli, with the small-signal currents $\Delta I_s(n) = g_m(n)\Delta V_{in}$ constituting the signal part. The offset currents and the tail current mismatch together approximate white noise. The input referred offset is minimized when the impulse response width $W_{\rm IR}$ is equal to the signal window $W_{\rm ZX}$ (i.e., the number of active preamps around zero crossing). This corresponds to a *matched* filter.

For a linear finite array, the boundary condition, $W_D > W_{\rm IR}$,[1] must be satisfied to avoid integral nonlinearity (INL) curvature at the extremes of input range, where W_D is the total number of dummy preamps. Conversely, this condition implies that $W_{\rm IR}$ must be the minimum W_D for a given INL curvature.

Dummies not only cost extra hardware but also consume precious voltage headroom. The input-referred rms offset normalized to LSB is optimum [11] when

$$W_D = (1/3)W_{\rm total} \tag{7}$$

where $W_{\rm total}$ is the total number of preamps allowed by the available headroom. Thus, the overall optimum condition becomes

$$W_D = W_{\rm IR} = (1/3)W_{\rm total} \le W_{\rm ZX} \tag{8}$$

[1]When the differential outputs at the two ends of a preamp array are cross-coupled through R1 to form a circular array [33], the boundary condition is changed to $W_D > \min(W_{\rm IR}, W_{\rm ZX})$.

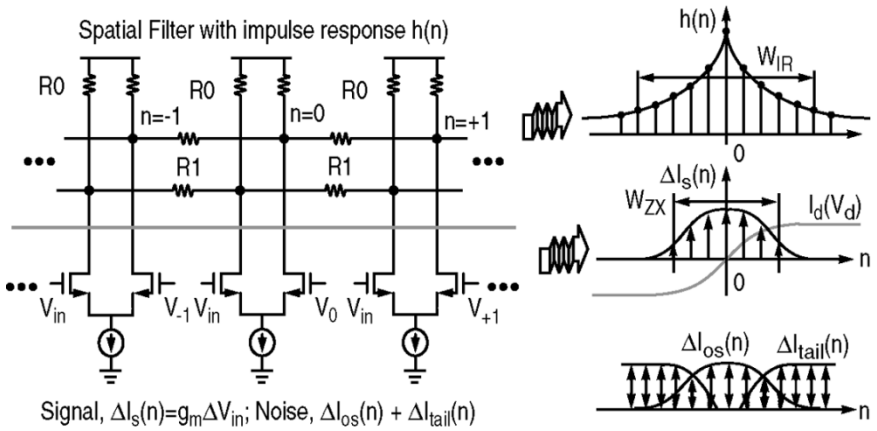


Fig. 5. Offset averaging as spatial filtering.

where $W_{\rm ZX}$ is defined as the flat portion of the signal window. At this optimum, preamp bandwidth is preserved to the first order, because the $R1$s do not diminish the *net* current driving each $R0$.

Even though averaging is not directly effective if the INL errors all lie in one direction, it can be made effective if the direction alternates. For example, in the 6-b and 7-b sub-ADCs, both the differential inputs and outputs of the neighboring preamps in the array are flipped in connection to place any spatially correlated comparator offsets (from, say, the second class of mismatch discussed in [17]) out of the passband of the spatial filter. Equivalently, the spatially alternated connections act like a spatial mixer which up-converts the succeeding spatial filter to highpass (or bandpass). A systematic treatment on folding, interpolation and averaging is presented in [11].

C. Optimum Bandwidth

Given a total gain $G_{\rm T}$, the overall bandwidth is optimized with respect to the number of cascaded amplifier stages m, and the dc gain G_i of each stage, $i = 1, 2, \cdots, m$. Assuming each stage has the same unity-gain bandwidth BW_u, i.e., $BW_i = BW_u/G_i$, the optimal condition is given by

$$m = ln\, G_{\rm T} \quad \text{and} \quad G_i = G_{\rm T}^{1/m}. \tag{9}$$

D. 7-b Sub-ADC

Fig. 6 shows the 7-b sub-ADC block diagram. The residue signal goes to an 84-preamp array in which offset averaging is applied. Monte Carlo simulations show that the standard deviation of the zero-crossing points at the output of each preamp within the FS, or the input-referred rms offset, is reduced by 3.6×. Seventy-two out of 84 ZX signals from the preamps are fed to the two cascaded three-fold amplifier stages, which multiplex the ZX signals by 3× each. The following 2× interpolation doubles the ZX signals. Among the nine folds of 72 ZXs, eight folds are within the FS. The half fold of ZXs on each side of the FS along with the extra 12 ZXs serves as dummies for averaging. Overall, the random INL error normalized to LSB is reduced by $3.6 \times 64/84 \sim 2.8$. If offset averaging were not used, the preamp FETs should be sized by $2.82 \sim 7.5$ to improve the random INL by the same amount. Using eight fewer dummies than the optimum given by (7) gives an acceptable practical tradeoff between the INL and noise, which improves with large FS. Based on (9), a modest voltage gain of $2.5 \sim 3\times$ is allotted to the preamps and the two folding amplifiers each to maximize the overall bandwidth for a given gain of $15\times$, enough to defeat the dynamic offsets in the latches which is on the order $30 \sim 50$ mV [33].

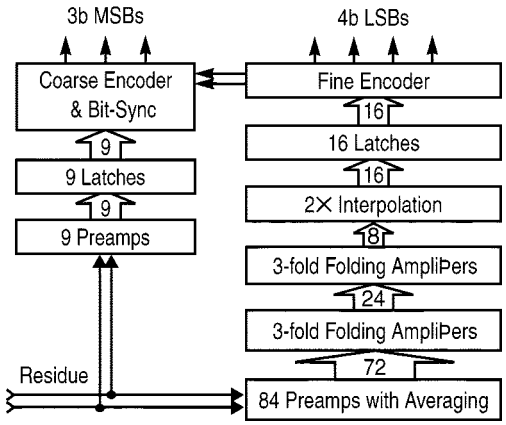


Fig. 6. 7-b sub-ADC block diagram.

This sub-ADC is similar to the previous art [33], but different in that a preamp array with optimum offset averaging appears before the folding stages. A pFET in triode between the preamp differential output nodes implements finite $R0$. A master–slave bias scheme sets the $R0$ value to about 5 kΩ. In the master preamp, $R0$ is realized with a precise unsilicided poly resistor of about 100-Ω sheet resistance; otherwise, the master preamp is identical to the slave and the preamps to be biased. The output difference between the slave and master which share the same input voltage of 0.05 V is sensed by an op amp whose output biases the gates of the pFETs in the slave preamp and those in the array. The negative feedback loop formed by the op amp forces the pFET resistance equal to the master $R0$. The lateral averaging resistor $R1$ is implemented with the same unsilicided poly. $R0$-to-$R1$ ratio is set to 10 so that the INL curvature is less than a quarter LSB. Averaging is relatively insensitive to this exact ratio.

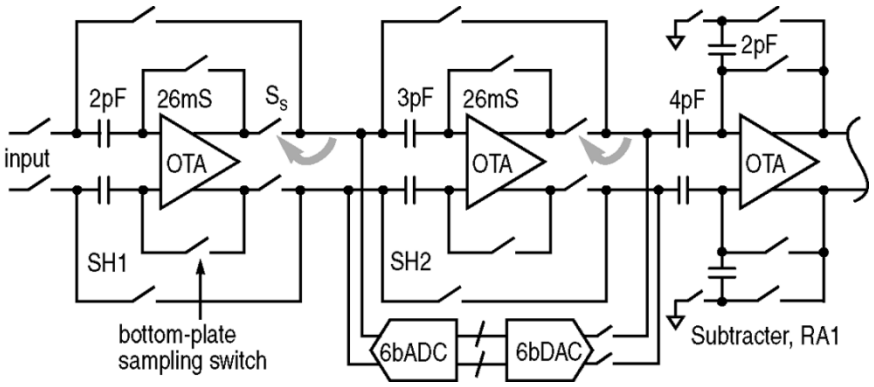


Fig. 7. S/H circuit.

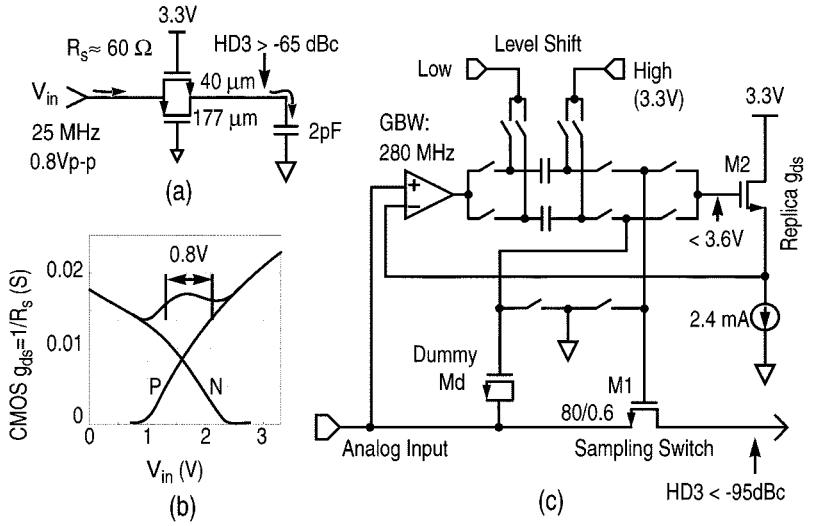


Fig. 8. Switch nonlinearity and the bootstrap circuit. (a) Hold capacitor. (b) Switch on-conductance g_{ds} as a function of input voltage. (c) Bootstrap circuit.

V. Circuit Implementation

A. S/H Circuit

The op amp-based bottom-plate sampling circuit (Fig. 7) prevents signal-dependent charge injection from degrading the linearity below 80 dB. Given that the 6-b sub-ADC loads S/H1 by 2 pF, and the reconstruction DAC loads S/H2 by 6 pF (including 2-pF parasitic), a compromise between power consumption and kT/C noise results in g_m of 26 mS for the OTAs in both S/H1 and S/H2, and 2 and 3 pF hold capacitance for S/H1 and S/H2, respectively.

As V_{dd} is lowered to 3.3 V, the interstage sampling switches become problematic. First, the switch *RC* delay is increasingly significant. Usually, the switch drives a load capacitance C_L which is much larger than the output capacitance C_o of the preceding closed-loop amplifier. If the switch on-resistance R_s is comparable to the closed-loop output resistance $R_o \sim 1/(g_m f)$, where f is the feedback factor, it considerably lengthens the settling time constant $\tau \sim (R_o + R_s)\, C_L$. Second, the switch nonlinearity in the front-end S/H severely distorts the sampled signal during track mode.

Complementary switches are used to ease those problems, but they are not enough. In this implementation, both problems are solved by moving the sampling switch S_s within the feedback loop of the preceding stage, as shown in Fig. 7. The effect of the in-loop switch S_s on the closed-loop transfer function (including the phase margin) is negligible because S_s is preceded by an OTA g_m stage of very high impedance and small parasitic capacitance ($C_{\rm op} < C_o$) relative to the output-node capacitance ($C_L + C_o - C_{\rm op} \sim C_L$) of the closed-loop. The time constant is reduced to $\tau \sim R_o C_L$. The feedback loop also linearizes the switch. In the front-end stage, the input switch sampling the analog input is linearized with the bootstrap circuit described next.

B. Bootstrap Circuit

Consider a complementary switch driving a hold capacitor [Fig. 8(a)]. Fig. 8(b) shows the switch on-conductance g_{ds} as a function of input voltage. Across the single-ended input range of 0.8 V, g_{ds} can not be made constant even at the best size ratio of 40 (nMOS)/177 (pMOS). This is partly due to the nonlinear body effect but especially due to the carrier mobility dependence on the *vertical* field (or V_{gs}) [42]. The latter is related to ill-behaved surface mobility [43] that can not be well compensated. The input-dependent on-resistance R_s distorts the track-mode current flowing into the hold capacitor at high input frequencies. The distortion gets worse at low V_{dd} and can not be scaled down due to the nonlinear junction capacitance. Simulations show that complementary switches attain, at best, -65 dBc track-mode

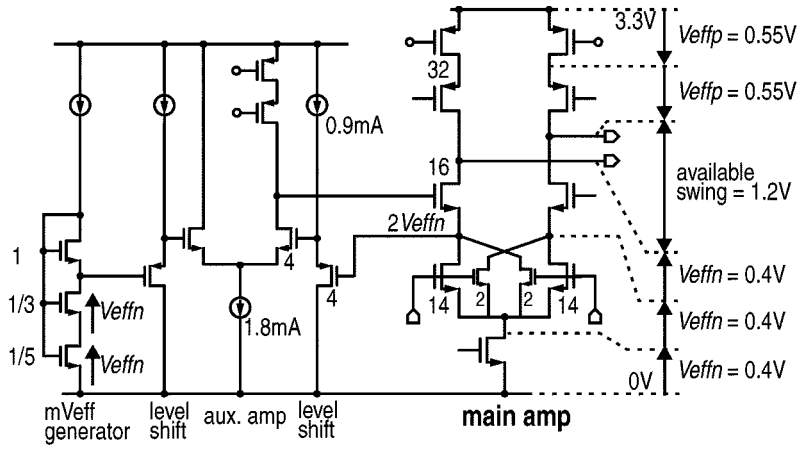


Fig. 9. Multiple-$V_{\rm eff}$-based OTA design.

distortion for single-ended 0.8-V_{p-p} at the Nyquist input frequency of 25 MHz.

To suppress the distortion below the required -80 dB level, a bootstrap circuit is used, as shown in Fig. 8(c). The nMOS sampling switch $M1$ is turned ON with the gate voltage of a replica FET $M2$ carrying a constant current of 2.4 mA. The op amp forces the source of $M2$ to track the analog input. This way, the sampling switch copies the g_{ds} of the replica, held constant by the fixed bias current. When the sampling switch turns off, the dummy switch Md switches in to balance the loading of the op amp. At the start of track mode, $M1$ is switched in before the dummy is switched off so that the dummy provides correlated initial charge to turn on $M1$ quickly. The precharged level-shift capacitors set the output common-mode voltage of the op amp. Simulations show that 280-MHz gain-bandwidth product (GBW) of the op amp ensures track-mode distortion lower than -95 dB with maximum gate voltage of 3.6 V. Other passive bootstrap schemes [44], [45] dissipate less power but can not remove the body effect.

C. OTA Design

Some OTA topologies are tailored for implementation at low V_{dd} [45]–[47]. Usually, signal swing is maximized to scale down the capacitor size. In this case, however, the third-order nonlinearity in the "linear capacitor" [48] implementing the switched capacitors limits the swing to 1.6-V peak-to-peak differential. Conventional super-cascode topology is suitable for this swing.

Multiple-$V_{\rm eff}$-based design, as shown in Fig. 9, maximizes the available swing. All stacked transistors of the same type are assigned the same $V_{\rm eff}$ $(= V_{gs} - V_t)$ with no margin. This requires a well-thought-out biasing scheme to operate reliably across process spreads. Multiple-$V_{\rm eff}$ biases are generated by scaling W/L based on the square law of the MOSFET. The biasing and biased transistors when well-matched in layout track each other, immune to process and temperature variations.

Since the linear g_m region set by $V_{\rm eff} = 0.4$ V is less than the input swing of 1.6-V_{p-p}, the OTA is not free of slewing, which causes dynamic nonlinearity or effectively reduces the available settling time. As a result, 12-b accuracy is obtained after settling for more than $10\times$ the time-constant. The closed-loop bandwidth of the S/Hs is 250 MHz, which simulation shows guarantees 12-b settling accuracy in half-cycle of 75-MHz clock. This gives enough margin for 50-MHz sampling in practice.

DC gain is 80 dB for sufficient margin to obtain the required closed-loop linearity. The auxiliary amplifiers provide about $30\times$ gain boost. The GBW must be over 250 MHz so that the zero-pole doublet corresponding to the auxiliary amplifier unity-gain frequency is positioned out of the closed-loop bandwidth to suppress the slow settling component [46]. It should not be too high either; otherwise, the auxiliary amplifier loop may become unstable. As a result, the final GBW is 300 MHz. The level-shift source followers add a pole to the loop, which however does not destabilize the loop, since it is about three times higher than the auxiliary amps GBW. The four auxiliary amplifiers dissipate a total power comparable to the main circuit. The OTAs in the first four residue amplifiers use double cascode topology to take advantage of the reduced residue swing, and this dissipates 50% less power due to absence of the auxiliary amplifiers.

Two small input transistors with their drains cross-connected maintain the minimum bias necessary to keep the cascode transistors ON at the beginning of each phase when the large input swing steers all the tail current to one leg. Another option is use of a resistor between the cascode sources [49]. Cutoff of the cascode transistors is harmful not only because the recovery slows down the settling, but also the auxiliary loop becomes unstable since the drastically reduced C_{gs} of the cascode transistor can not compensate the auxiliary amplifier.

The OTA output common-mode (CM) voltage is shorted to the input CM, $V_{\rm th} + 2V_{\rm eff}$, in the reset phase, but is raised to $V_{dd}/2 \sim 1.7$ V in the hold phase to maximize output swing. The dual common-mode voltages are realized by two pairs of switched level-shift capacitors precharged to two different voltages [50].

D. Reconstruction DAC

In Fig. 3, the first (most negative differential) coarse tap, -FS/2, is formed by connecting the top plates (bottom plates in layout) of all the eight-unit capacitors (C_{sp}) on the positive side to $-V_{\rm ref} = -$FS/4 and those (C_{sn}) on the negative side to $+V_{\rm ref} = +$FS/4; the second tap corresponds to one of the seven

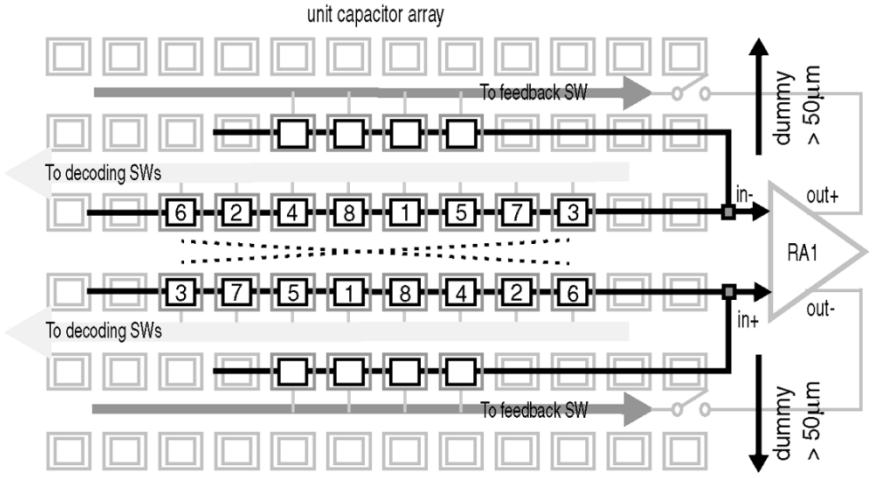


Fig. 10. DAC capacitors in differential common-centroid layout.

differential capacitor pairs (those not connected to the resistor ladder) flipped in connection, and so on. Although the circuit and the reference taps are differential, the errors in the taps are not. This is generally true for fully segmented DACs controlled by thermometer codes.

A differential common-centroid layout averages the differential capacitance based on the expression for residue gain, $G = (C_{sn} + C_{sp})/2C_f$. Fig. 10 shows two rows of differential unit capacitors in common-centroid layout, addressed in scrambled order across the array to suppress possible cumulative gradient effects [51]. Grounded metal-3 shield on top of the array eliminates mismatch due to long-range fringes [52]. Dummy capacitors extending over a distance of 50 μm prevent uneven lithography at the boundaries from encroaching on the array [52]. Each (linear) capacitor consists of a polysilicon plate over thin oxide and a heavily doped n+ diffusion.

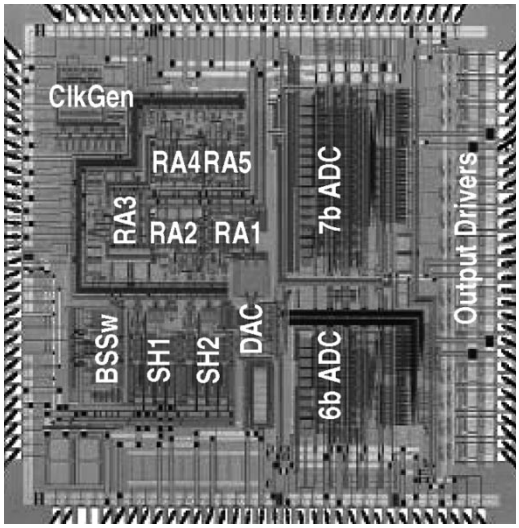


Fig. 11. 12-b ADC chip micrograph.

VI. Performance Evaluation

The chip (see the micrograph in Fig. 11) is fabricated through MOSIS in a 0.6-μm, triple-metal, single-poly standard digital CMOS process with analog options of linear capacitor and unsilicided poly resistor. First silicon is successful, due to the whole-chip simulation methodology used [11]. The active chip area is 4×4 mm^2 and the ADC excluding the output drivers dissipates 850 mW from 3.3-V supply.

All clocks are generated on-chip from an external low phase noise, balanced sinewave. Both CMOS inverter-type and differential (open-drain) output buffers are built on-chip. The digital noise from the CMOS buffers is intentionally coupled to the internal circuits by tying all on-chip V_{dd}'s and Gnd's together, respectively. This allows for comparison between the CMOS and differential buffers in terms of their effect on the SFDR. To suppress power bounce, total 2-nF decoupling capacitance between V_{dd} and Gnd is laid out in unused areas all over the chip, and 18 pins are assigned to V_{dd} and Gnd, respectively. Discrete fifth-order low-pass filters and crystal filters suppress the harmonics and noise from the test signal generator.

Code density test yields 1.3 LSB INL and 0.8 LSB differential nonlinearity (DNL) (Fig. 12). The eight segments clearly visible in the measured INL plot reflect small mismatch among the eight-unit capacitors of the reconstruction DAC. The spikes, numbering about 64×2, come from an unexpected systematic INL in the 7-b sub-ADC, which appears as an eight-fold or four-period profile. The measured INL of the 6-b sub-ADC also shows such pattern that is typical of folding ADCs. On average, half of the four periods are traversed by the 64 residue segments, yielding total 64×2 peaks in the overall INL.

Fig. 13(a) shows this ADC achieves over 80-dB SFDR for signal frequencies up to 75 MHz at 50 MSPS. The SFDR rolloff at 80-MHz input and at 50 MSPS is due to the finite bandwidth of the bootstrap circuit and the DAC, respectively. SNR, defined as the SNDR subtracted by the first seven harmonics, is 64 dB at maximum. The maximum SNR shown in Fig. 13(b) is smaller than that in Fig. 13(a) by 1 dB due to absence of band-pass filter in the signal path during testing. The 4-dB rolloff at 200-MHz input corresponds to 0.61-ps sampling jitter, which is confirmed with a locked histogram test and is close to the simulated 0.44 ps. The measured output histogram is fitted to a binned

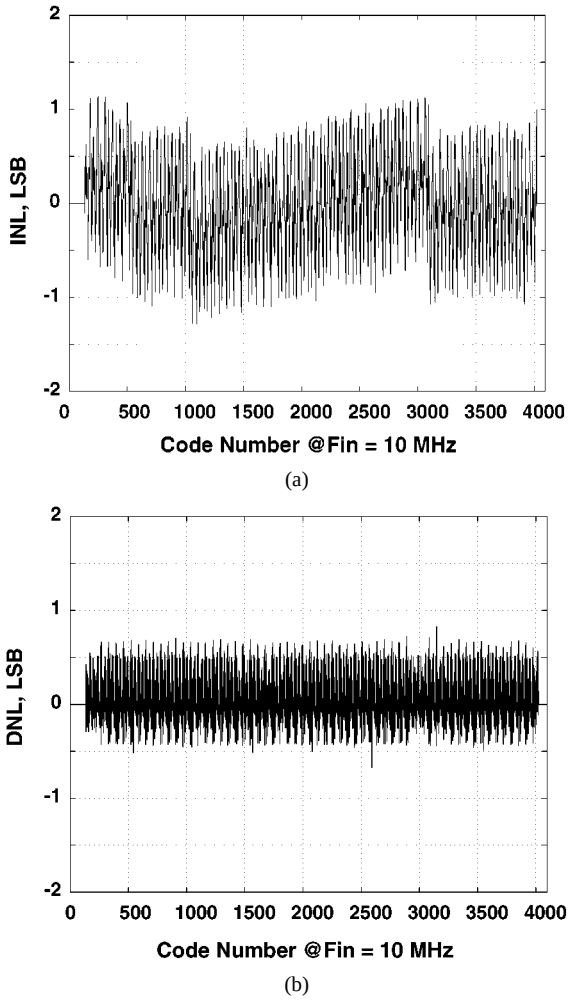


Fig. 12. Code density test results. (a) INL at $f_s = 50$ MS/s, with 16.4 million samples. (b) DNL at $f_s = 50$ MS/s, with 16.4 million samples.

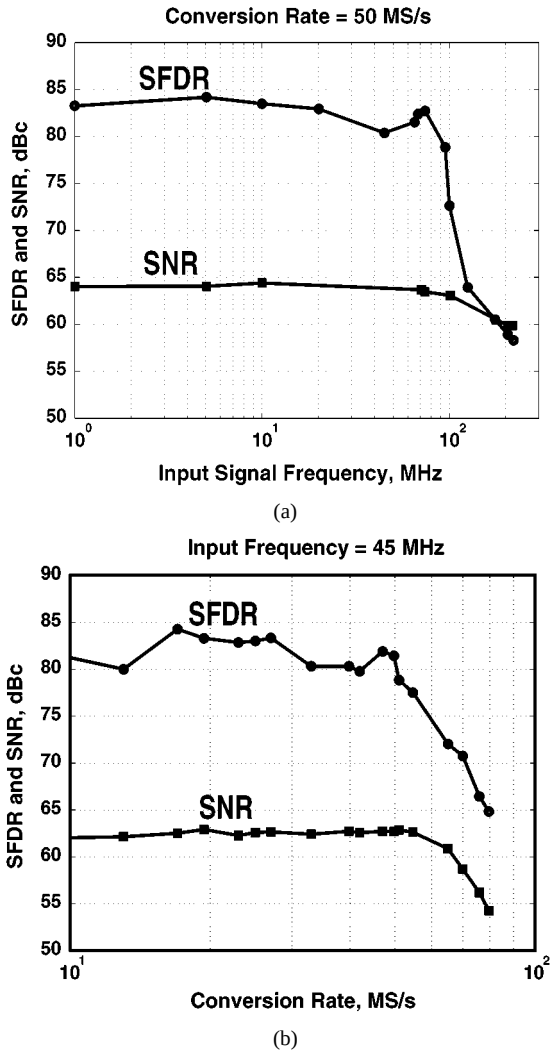


Fig. 13. Dynamic performance.

Gaussian distribution. Jitter is calculated from the best-fit standard deviation. Perfect fitting can not be achieved unless the bin sizes are adjusted with the measured DNL.

The labeled high-order ($349\sim365$) spurs in Fig. 14(a) are characteristic of the INL in the 7-b ADC, based on the following calculations. Since the fundamental is -0.8 dB FS, the input sinewave sees about 91% of the 64×2 periods (spikes) in the FS INL plot. From (5), those spikes produce peak harmonics located around (91% $\times 64 \times 2)\ \pi \sim 367$. The maximum level of those spurs, which is about -86 dB, is close to what (4) predicts for the case of $n_1 = 7$ and $\varepsilon = 2\,\varepsilon_0 = 2^{-5}$, which approximates the measured INL profile.

Using CMOS inverter-type output buffers, the measured SNR and SFDR remain unchanged at low input frequencies, but decay faster as the input increases in frequency. The rolloff corresponds to about 1.8-ps sampling jitter. This indicates that the bounce from the CMOS output drivers is picked up by the inverter-type clock buffers but rejected by other differential circuits. Fig. 14(b) shows how the output spectrum is affected. The dominant even-order harmonics confirm the single-ended noise coupling. The bounce brings down the SNR by 2.9 dB (from 61.3 to 58.4 dB), but still not enough to apparently spread out the high-order spurs. This makes sense because dithering is not effective until the noise reaches a level comparable to the period of the INL pattern responsible for the high-order spurs. In this case, the period is about 7-b LSB, which corresponds to about 42 dB SNR.

The largest spur is among the second to the fifth harmonics, which tend to fluctuate by up to 3 dB between measurements. The fluctuation can be ascribed to the finite FFT points and noise [54], but more likely in this case to the sensitivity to variation in input amplitude and offset, typical of the low-order harmonics arising from quantization [11]. If it were not for the DAC nonlinearity, the largest spur should be among the high orders ($349\sim365$). Since the largest spur actually appears at low-order and is only a few decibels higher, the DAC must contribute low-order harmonics comparable to those from the 7-b INL. Even though the high-order spurs limit small-signal SFDR because they increase by 0.5 dB for each decibel reduction in input amplitude, they can be removed by correcting the 7-b systematic INL error. In contrast, the DAC errors arising from random capacitor mismatch presents a fundamental limitation to the SFDR unless they are dynamically scrambled [55]–[60]. Distortion in the S/Hs produces a dominant third-order harmonic, which does not appear until the input frequency goes beyond 75 MHz.

Fig. 15 shows that the ADC works to 3.05-V supply.

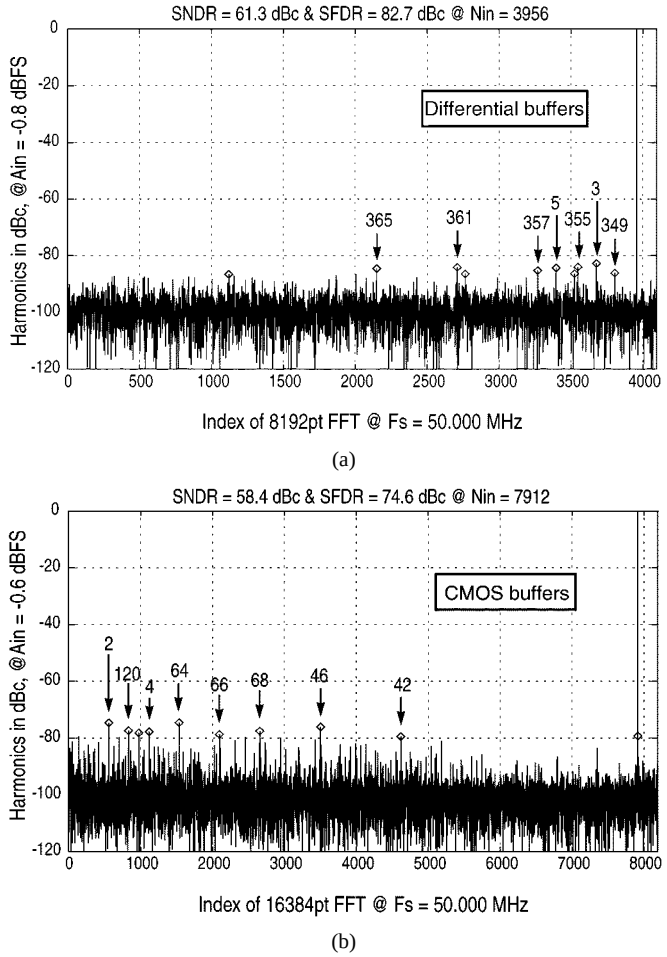


Fig. 14. Measured ADC output spectra with differential and CMOS output drivers at $f_{in} = 74.146$ MHz and $f_s = 50$ MHz. (a) Differential buffers. (b) CMOS buffers.

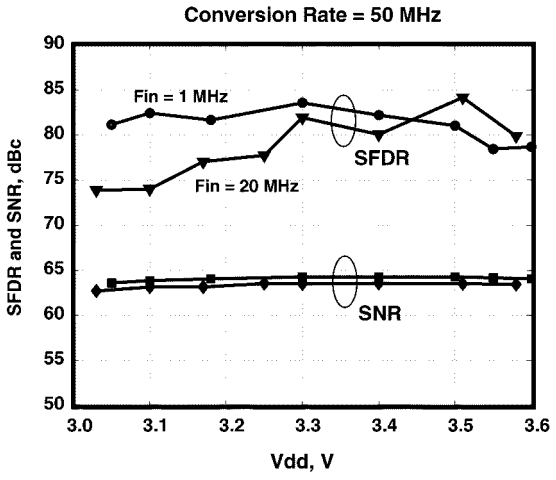


Fig. 15. V_{dd} tolerance test.

The MATLAB numerical model of the ADC is also useful in understanding the measured data. The FFT of a sinewave digitized by a 12-b ADC in MATLAB whose quantization thresholds are perturbed by the measured INL data is similar to the measured spectrum, confirming that INL dominates SFDR. In terms of SNDR, the reconstructed spectrum is 3.5 dB better than the measured (67.5 versus 64.0 dB), suggesting a random noise about 1.24 times the INL distortion. The random noise is also directly measured by grounded input tests, from which a noise (rms) of 0.66 LSB (i.e., 257 μV) is extracted. The MATLAB ADC shows that the reconstructed spectrum degrades in SNR by 3.5 dB when this noise is added at the input, and further by 4 dB at 200-MHz input frequency when the time index of the input sinewave function is perturbed with 0.61-ps jitter (rms)—consistent with the measured SNR rolloff shown in Fig. 13(a). The results are summarized in Table II.

TABLE II
PERFORMANCE SUMMARY

Resolution	12 bits
INL / DNL @f_{in} = 10 MHz	+/- 1.3 LSB / 0.8 LSB
Analog Input	1.6 Vp-p differential
Input Capacitance (S/H)	2 pF
Latency	4
Clock Jitter	< 0.61 ps
Error Rate [49] @f_s = 80 MHz	< 10^{-13} (in errors/sample)
Conversion Rate	50 MS/s
SFDR @f_{in} < 75 MHz	> 80 dB
SNR @f_{in} = 1 MHz / 200 MHz	64 dB / 60 dB
Power Dissipation	850 mW
Min. Power Supply Voltage	3.05 V
Technology	3.3-V, 0.6-μm CMOS
Active/Total Die Area	4x4 mm^2 / 5.5x4.8 mm^2

VII. CONCLUSION

A pipeline ADC with large number of bits in the first stage is inherently superior in SFDR, because the first-stage multibit quantization spreads the spur energy arising from the interstage gain error, random DAC nonlinearity, and INL in the second stage sub-ADC. This is demonstrated with the ADC prototype of a 6–7-b partition, which achieves over 80-dB SFDR for signal frequencies up to 75 MHz at 50 MSPS without trimming, calibration, or dithering. The required low-latency (flash) multibit (6-b) sub-ADC is made efficient using folding, averaging and interpolation techniques. Offset averaging is optimized based on spatial filtering. The bootstrap circuit, in-loop interstage switch and multi-V_{eff} OTA are instrumental in achieving the required linearity in the front-end S/Hs at low V_{dd} of 3.3 V. The major spurs are identified and related to the imperfections in the ADC. The intuitive and analytical approach used in this work proves effective in designing and evaluating ADCs intended for IF sampling.

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T. Brooks suggested the in-loop switch action as presented in Section V-A.

REFERENCES

[1] T. Gratzek, B. Brannon, J. Camp, and F. Murden, "A new paradigm for base station receivers: High IF sampling + digital filtering," in *1997 IEEE Radio Frequency Integrated Circuits Symp.*, June 1997, pp. 143–146.

[2] ——, "ADCs for digital receivers: The whole world tunes in," in *1996 IEEE MTT-S Dig.*, pp. 1335–1338.

[3] D. B. Chester, D. H. Damerow, and C. Olmstead, "Analog to digital converter requirements and implementations for narrowband channelization applications," in *IEEE Int. Conf. Acoustics, Speech and Signal Processing*, vol. 4, Mar. 1992, pp. 325–328.

[4] F. Murden and R. Gosser, "12-b 50-Msample/s two-stage A/D converter," in *ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 1995, pp. 278–279.

[5] Analog Devices, AD9042 Data Sheet, 1996.

[6] P. Vorenkamp and R. Roovers, "A 12-b 60-MSample/s cascaded folding and interpolating ADC," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1876–1886, Dec. 1997.

[7] D. Birdsall and A. Kuckreja, "A 12-bit, 65 MSPS BiCMOS ADC for cellular base-station applications," in *Proc. 1998 Bipolar/BiCMOS Circuits and Technology Meeting*, Sept. 1998, pp. 43–46.

[8] A. G. Clavier, P. F. Panter, and D. D. Grieg, "Distortion in a pulse count modulation system," *AIEE Trans.*, vol. 66, pp. 989–1005, 1947.

[9] D. R. Martin and D. J. Secor, "High-speed analog-to-digital converters in communication systems: Terminology, architecture, theory and performance," TRW Electronics Systems Group, Redondo Beach, CA, Nov. 1981.

[10] W. T. Colleran, "A 10-bit 100-MS/s A/D converter using folding, interpolating, and analog encoding," Ph.D. dissertation, Univ. California, Los Angeles, CA, Dec. 1993.

[11] H. Pan, "A 3.3-V 12-b 50-MS/s A/D converter in 0.6-μm CMOS with over 80-dB SFDR," Ph.D. dissertation, UCLA, Dec. 1999.

[12] W. R. Bennett, "Spectra of quantized signals," *Bell Syst. Tech. J.*, vol. 27, pp. 446–472, July 1948.

[13] A. Gersho, "Principle of quantization," *IEEE Trans. Circuits Syst.*, vol. CAS-25, pp. 427–436, July 1978.

[14] R. M. Gray, "Quantization noise spectra," *IEEE Trans. Inform. Theory*, vol. 36, pp. 1220–1244, Nov. 1990.

[15] R. M. Gray and D. L. Neuhoff, "Quantization," *IEEE Trans. Inform. Theory*, vol. 44, pp. 1–63, Oct. 1998.

[16] S. H. Lewis and P. R. Gray, "A pipelined 5-Msample/s 9-bit analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 22, pp. 954–961, Dec. 1987.

[17] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1440, Oct. 1989.

[18] M. J. M. Pelgrom and M. Vertregt, "CMOS technology for mixed signal ICs," *Solid-State Electron.*, vol. 41, pp. 967–974, July 1997.

[19] S. H. Lewis *et al.*, "A 20-b 20-Msample/s analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 27, pp. 351–358, Mar. 1992.

[20] H.-S. Lee, D. A. Hodges, and P. R. Gray, "A self-calibrating 12-b CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 813–819, Dec. 1984.

[21] Y. M. Lin, B. Kim, and P. R. Gray, "A 13-b 2.5-MHz self-calibrated pipelined A/D converter in 3-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 26, pp. 628–636, Dec. 1991.

[22] S.-H. Lee and B.-S. Song, "Digital-domain calibration of multistep analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1679–1688, Dec. 1992.

[23] M. de Wit, K.-S. Tan, and R. K. Hester, "A low-power 12-b analog-to-digital converter with on-chip precision trimming," *IEEE J. Solid-State Circuits*, vol. 28, pp. 455–461, Dec. 1993.

[24] E. G. Soenen and R. L. Geiger, "An architecture and an algorithm for fully digital correction of monolithic pipelined ADCs," *IEEE Trans. Circuits Syst. II*, vol. 42, pp. 143–153, Dec. 1995.

[25] I. E. Opris, L. D. Lewicki, and B. C. Wong, "A single-ended 12-bit 10 Msample/s self-calibrating piepline A/D converter," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1898–1903, Dec. 1998.

[26] R. E. J. van de Grift, I. W. J. M. Rutten, and M. van der Veen, "An 8-bit video ADC incorporating folding and interpolation techniques," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 944–953, Dec. 1987.

[27] R. J. van de Plassche and P. Baltus, "An 8-bit 100-MHz full-Nyquist analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1334–1344, Dec. 1988.

[28] W. T. Colleran and A. A. Abidi, "A 10-b 75-MHz two-stage pipelined bipolar A/D converter," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1187–1199, Dec. 1993.

[29] R. Roovers and M. Steyaert, "Design of CMOS A/D converters with folding and/or interpolating techniques," in *Advanced A-D and D-A Conversion Techniques and Their Applications*, July 6–8, 1994, pp. 76–81.

[30] B. Nauta and A. G. W. Venes, "A 70-MS/s 110-mW 8-b CMOS folding and interpolating A/D converter," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1302–1308, Dec. 1995.

[31] A. G. W. Venes and R. J. van de Plassche, "An 80-MHz, 80-mW, 8-b CMOS folding A/D converter with distributed track-and-hold preprocessing," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1846–1853, Dec. 1996.

[32] M. Flynn and B. Sheahan, "A 400MSample/s 6-b CMOS folding and interpolating ADC," in *ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 1998, pp. 150–151.

[33] K. Bult and A. Buchwald, "An embedded 240-mW 10-b 50MS/S CMOS ADC in 1-mm^2," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1887–1895, Dec. 1997.

[34] K. Kattmann and J. Barrow, "A technique for reducing differential nonlinearity errors in flash A/D converters," in *ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 1991, pp. 170–171.

[35] J. L. White and A. A. Abidi, "Active resistor networks as 2D sampled data filters," *IEEE Trans. Circuits Syst. I: Fundamental Theory and Applications*, vol. 39, pp. 724–733, Sept. 1992.

[36] B. D. Smith, "An unusual analog-digital conversion method," *IRE Trans. Instrum. Meas.*, pp. 155–160, June 1956.

[37] J. D. Edson and H. H. Henning, "Broadband codecs for an experimental 224 Mb/s PCM terminal," *Bell Syst. Tech. J.*, pp. 1887–1940, Nov. 1965.

[38] A. Arbel and R. Kurz, "Fast ADC," *IEEE Trans. Nucl. Sci.*, vol. NS-22, pp. 446–451, Feb. 1975.

[39] U. Fieldler and D. Seitzer, "A high-speed 8-bit A/D converter based on a gray-code multiple folding circuit," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 547–551, June 1979.

[40] R. J. van de Plassche and R. E. J. van de Grift, "A high-speed 7 bit A/D converter," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 938–943, Dec. 1979.

[41] R. E. J. van de Grift and R. J. van de Plassche, "A monolithic 8-bit video A/D converter," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 374–378, June 1984.

[42] T. Ando, A. B. Fowler, and F. Stern, "Electronic properties of two-dimensional systems," *Rev. Mod. Phys.*, vol. 54, pp. 437–672, 1982.

[43] G. S. Gildenblat and C.-L. Huang, "Engineering model of inversion channel mobility for 60–300 K temperature range," *Electron. Lett.*, vol. 25, pp. 634–636, May 1989.

[44] M. de Wit, "Sample and hold circuitry and methods," U.S. Patent 5170075, Texas Instruments Inc., Dec. 8, 1992.

[45] A. M. Abo and P. R. Gray, "A 1.5-V 10-bit 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, pp. 599–606, May 1999.

[46] K. Bult and G. J. G. M. Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB dc gain," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1379–1384, Dec. 1990.

[47] T. B. Cho and P. R. Gray, "A 10-b 20-Msample/s 35-mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, pp. 166–172, Mar. 1995.

[48] T.-I. Liou and C.-S. Teng, "n$^+$-poly-to-n$^+$-silicon capacitor structures for single-poly analog CMOS and BiCMOS processes," *IEEE Trans. Electron Dev.*, vol. 36, pp. 1620–1628, Sept. 1989.

[49] C. W. Mangelsdorf, "A 400-MHz input flash converter with error correction," *IEEE J. Solid-State Circuits*, vol. 25, pp. 184–191, Feb. 1990.

[50] K. Y. Kim, N. Kusayanagi, and A. A. Abidi, "A 10-b 100-MS/s CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. 32, pp. 302–311, Mar. 1997.

[51] C. S. G. Conroy, W. A. Lane, and M. A. Moran, "Statistical design techniques for D/A converters," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1118–1128, Aug. 1989.

[52] M. J. McNutt, S. LeMarquis, and J. L. Dunkley, "Systematic capacitance matching errors and corrective layout procedures," *IEEE J. Solid-State Circuits*, vol. 29, pp. 611–616, May 1994.

[53] H. P. Tuinhout, H. Elzinga, J. T. Brugman, and F. Postma, "The floating gate measurement technique for characterization of capacitor matching," *IEEE Trans. Semicond. Manufact.*, vol. 9, pp. 2–8, Feb. 1996.

[54] P. Carbone and D. Petri, "Effective frequency-domain ADC testing," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 660–663, July 2000.

[55] L. R. Carley, "A noise shaping coder topology for 15+ -bit converters," *IEEE J. Solid-State Circuits*, vol. 24, pp. 267–273, Apr. 1989.
[56] B. H. Leung and S. Sutarja, "Multibit D S A/D converter incorporating a novel class of dynamic element matching techniques," *IEEE Trans. Circuits Syst. II*, vol. 39, pp. 35–51, Jan. 1992.
[57] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit $\Delta\Sigma$ A/D and D/A converters using data-weighted averaging," *IEEE Trans. Circuits Syst. II*, vol. 42, pp. 753–762, Dec. 1995.
[58] R. Radke, A. Eshraghi, and T. S. Fiez, "A spurious-free delta–sigma DAC using rotated data weighted averaging," in *Proc. IEEE 1999 Custom Integrated Circuits Conf.*, May 1999, pp. 125–128.
[59] R. Adams, K. Q. Nguyen, and K. Sweetland, "A 113-dB SNR oversampling DAC with segmented noise-shaped scrambling," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1871–1878, Dec. 1998.
[60] I. Galton, "Digital cancellation of D/A converter noise in pipelined A/D converters," IEEE Trans. Circuits Syst. II, to be published.

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