A Fully Integrated 0.13-μm CMOS Mixed-Signal SoC for DVD Player Applications

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***Abstract*—This paper describes a fully integrated single-chip CMOS mixed-signal system on a chip (SoC) for DVD player applications. It integrates one digital signal processor (DSP), two 32-bit CPUs, three dedicated processing units, a partial response maximum likelihood (PRML) read channel with an analog front end (AFE), and many other subsystems on the same die. The AFE includes a fifth-order G_m-C filter and attains over 66 dB C/N overall. PR(3,4,4,3) structure is employed in the PRML read channel. Owing to the PRML signal processing and the mixed-signal system level optimization in the PRML read channel, less than 10^{-6} of bit-error rate (BER) is obtained for the focus offset margins over ± 0.5 μm. This SoC is fabricated in 0.13-μm one-poly six-Cu CMOS technology. It contains 24 million transistors in a 63.87 mm^2 die and consumes 1.5 W at 40 MSample/s data rate, which corresponds to DVD 1.5 times playback operation mode.**

***Index Terms*—Analog front end (AFE), CMOS, DVD, G_m-C filter, LSI, mixed-signal technology, partial response maximum likelihood (PRML), read channel, system on a chip (SoC).**

I. Introduction

THE DVD player market has been growing rapidly for the past several years. This growth will remain strong in the coming years. The competition for customers in the worldwide DVD player market requires lower prices and higher performance for DVD player systems. Especially, low cost and low power are very important issues for LSIs in these systems. In addition, requirements for development of high-readability systems and realization of high image quality are increasing with the diversity of read/write media such as DVD-RAM media, which have lower signal-to-noise ratio (S/N) than ROM media. System on a chip (SoC) must be the most efficient solution to meet these demands. To meet these demands, there are many sophisticated signal processing techniques on high-performance storage LSIs and related technologies [1]–[6].

Fig. 1 shows the block diagram of the conventional DVD player system. This system has three main blocks: a front-end (FE), a back-end (BE), and a controller. The FE performs readout processing, servo processing, and so on. The BE decodes the data extracted by the FE and converts it into audio/visual (A/V) data. The controller manages whole operations in both the FE and the BE. To realize the functions of the FE, the BE, and the controller, the conventional system requires seven LSIs, an analog front-end (AFE) LSI, an optical disc controller LSI, an audio LSI, a progressive LSI, a decoder LSI, a system controller LSI, and a panel controller LSI, shown in Fig. 1. In particular, the AFE LSI is designed by using BiCMOS technology. This seven-chip structure increases the total power consumption and the production cost.

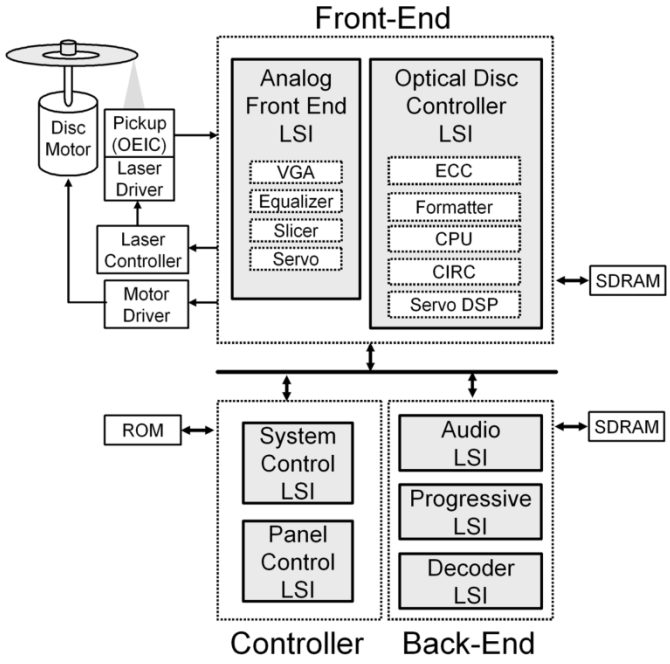

Fig. 1. Conventional DVD player system.

Moreover, in the conventional system, due to simple data detection algorithms implemented in a data slicer, the intersymbol interference (ISI) of the read signal should be low. For high-density DVD signals with large ISI and low S/N ratio, this simple approach makes it difficult to extract accurate data. This has an influence on the readability and the image quality.

This paper describes a fully integrated mixed-signal SoC for DVD player applications. Low power consumption and high readability are achieved by the one-chip solution and a mixed-signal optimization.

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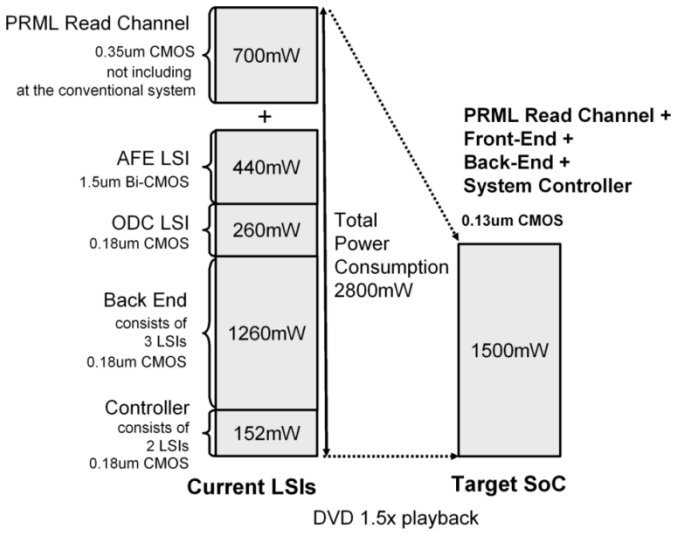

Fig. 2. SoC target.

II. SoC Architecture

A. SoC Target

A low-power and low-cost solution is very important in the design of DVD player systems. High readability is also strongly required for these systems. To address these issues, the following three targets are set. The first target is development of a fully integrated mixed-signal SoC that includes the conventional seven LSIs. This means that the AFE LSI must be integrated on the same die. The second target is employment of the high-performance signal processing method for rewritable media such as DVD-RAM read operation. The last is the development of a low-power system and use of a plastic package.

Fig. 2 shows the power consumption target for the proposed SoC compared with the conventional DVD player system. In the conventional system, seven LSIs are used for signal processing, and they consume in total 2.1 W at 1.5 times DVD playback operation mode. Moreover, the conventional system does not include a read channel employing highly accurate data extraction method such as the partial response maximum likelihood (PRML) technique. If employing the PRML read channel in the conventional system, the total power consumption should be 2.8 W at 1.5 times DVD playback operation mode.

The total power consumption target for the proposed SoC including the PRML read channel is 2.0 W at 54 MSample/s, which corresponds to 2 times DVD playback operation mode. The power consumption target should decrease to 1.5 W in 1.5 times DVD playback operation mode. That means about 50% reduction of total power consumption in the case of employing the PRML read channel with the conventional seven LSIs.

In order to realize these targets, the following two approaches have been taken. The first approach is the use of the 0.13-μm CMOS process to realize highly functional integration and to reduce the total power consumption. The second is the use of the PR(3,4,4,3)ML architecture with the high-performance fifth-order G_m-C filter. In addition, the mixed-signal system-level optimization has been performed instead of the conventional analog method. As a result of these approaches, analog area, the number of external elements, and production cost have been reduced dramatically.

B. Overall Architecture

Fig. 3 shows the block diagram of the proposed SoC. It integrates the FE, the BE, and the controller. The FE includes a 32-bit CPU (CPU2), an optical disc formatter (FMT), a servo digital signal processor (DSP), an error-correction code (ECC) circuit, an AV interface, and the PRML read channel with the AFE including the fifth-order G_m-C filter. The BE for an AV decoding consists of an IO processor, a pixel operation processor, and an AV decode processor. The system controller includes a 32-bit CPU (CPU1).

In the playback mode, the FE receives analog readout signals from an optical pick up (OPU). In order to control a position of the OPU, the servo DSP calculates a focus error and a tracking error with the data preprocessed by the AFE. The PRML read channel with a main stream reading part of the AFE extracts recorded data and synchronized clock. The FMT decodes the data from the PRML read channel and the ECC corrects the error in the decoded data, and delivers to the BE. The CPU2 in the FE controls the operations of the FE.

The BE includes three processors: the AV decode processor, the IO processor, and the pixel operation processor. By controlling these processors cooperatively, multifunctional processing can be realized as follows.

A video decoding processing is realized by using the AV decode processor and four dedicated hardware engines: a variable length decoder (VLD), an inverse quantization unit (IQ), an inverse discrete cosine transform unit (IDCT), and a motion compensation unit (MC). In this processing, the AV decode processor performs the stream analysis which varies according to the video compression standard. Also audio decoding processing is realized by using the AV decode processor. In addition to the audio decoding processing, various sound effect processing is implemented in this SoC, and it is possible to combine it with the audio decoding processing by software control.

In order to realize high picture quality enhancement, various image processing can be realized by using the pixel operation processor. In this SoC, a progressive conversion processing and various noise reduction processing are implemented. An interpolation filter, which is used in the progressive conversion processing, is changed adaptively based on the motion of every pixel detected in correlation of consecutive interlace pictures. In the noise reduction processing, mosquito noise, block noise, and random noise can be removed. Moreover, scaling processing can be realized by time sharing.

The IO processor performs analysis of the bit stream input from the FE and output processing of the decoded A/V data.

In this way, the BE achieves various media processing through applying flexibility of software control.

The system controller consists of an interrupt controller, a timer, a serial I/F, and the 32-bit RISC CPU (CPU1). The CPU1 controls whole functions in this SoC and operates at 67.7 MHz.

Only one SDRAM located outside of the SoC is required in the new system, where two SDRAMs are required in the conventional system.

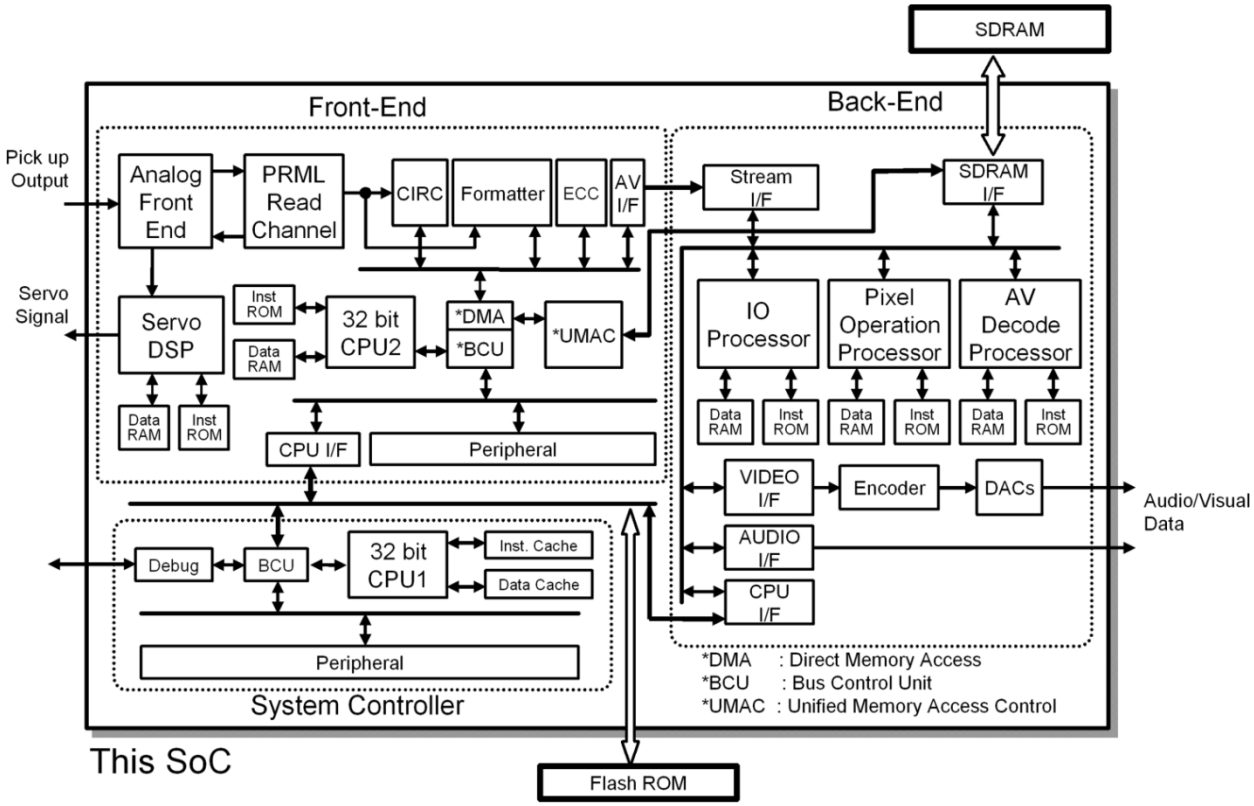

Fig. 3. Block diagram of the proposed SoC.

A unified memory access controller (UMAC) arbitrates the memory access requests between the FE and the BE. Several access requests from the FE to the SDRAM are compared with an access request from the BE and are divided into high-priority access requests and low-priority access requests in the UMAC. According to priority of the access requests, the memory access from the FE and the BE to the SDRAM is done. In addition, the UMAC has the function to change several access requests from the FE into single burst access. By using this function, increase in efficiency of memory access has been attained.

The one-chip solution provides drastic reduction of system cost, and low-voltage power supply using 0.13-μm CMOS technology realizes low power consumption. The PRML signal processing and the AFE including the fifth-order G_m-C filter placed close by the PRML read channel on the die contribute high performance of the data extraction.

III. PRML Read Channel

A. Block Configuration

High-density recording systems have low S/N ratio and large ISI. Thus, the PRML read channel technique has been implemented into the SoC to reduce the BER and to increase the focus offset margin and the tilt margin.

Fig. 4 shows the block diagram of the PRML read channel in the SoC. The PRML read channel consists of a variable gain amplifier (VGA), an offset adjuster, a fifth-order G_m-C filter, a 7-bit analog-to-digital converter (ADC), an adaptive finite-impulse response (FIR) filter employing a least mean square (LMS) algorithm, a Viterbi detector, and a phase-locked loop (PLL).

Due to large variations of a reflection coefficient of the disc and characteristics of the OPU, the amplitude and the center level of the input signals vary widely. Therefore, to compensate these variations and control to fit the dynamic range of the 7-bit ADC, the first step in the read operation spends a gain control and an offset control operation. A digital controller block, which consists of a gain controller, an offset controller, and a defect detector, detect top peaks and bottom peaks from the digitized input data. A gain control signal and an offset control signal, which are calculated by using these peak data, are input to the 8-bit current-mode digital-to-analog converters (DACs) to control the VGA and the offset adjuster, respectively. In a gain control loop, the variable range of the VGA is 26 dB. Furthermore, defects such as black dot out and off track can be detected by this digital control block. In the conventional system, these controls have been realized in analog signal processing. In this system, a digital control method is employed. Large reductions of analog area, external elements, and cost have been attained by this approach. Furthermore, optimization of these feedback loops have been easily realized. After this process, a pre-equalization is performed with a continuous-time filter. The fifth-order G_m-C filter is used as a continuous-time filter. A pre-equalized signal is input to the 7-bit ADC and converted into digital data. This converted data is input to the adaptive FIR filter and equalized digitally. This equalized data is input to the Viterbi detector and data detection process is performed. This detected data is output to other circuit blocks. The digital data converted by the 7-bit ADC is also input to the PLL to extract the synchronous clock.

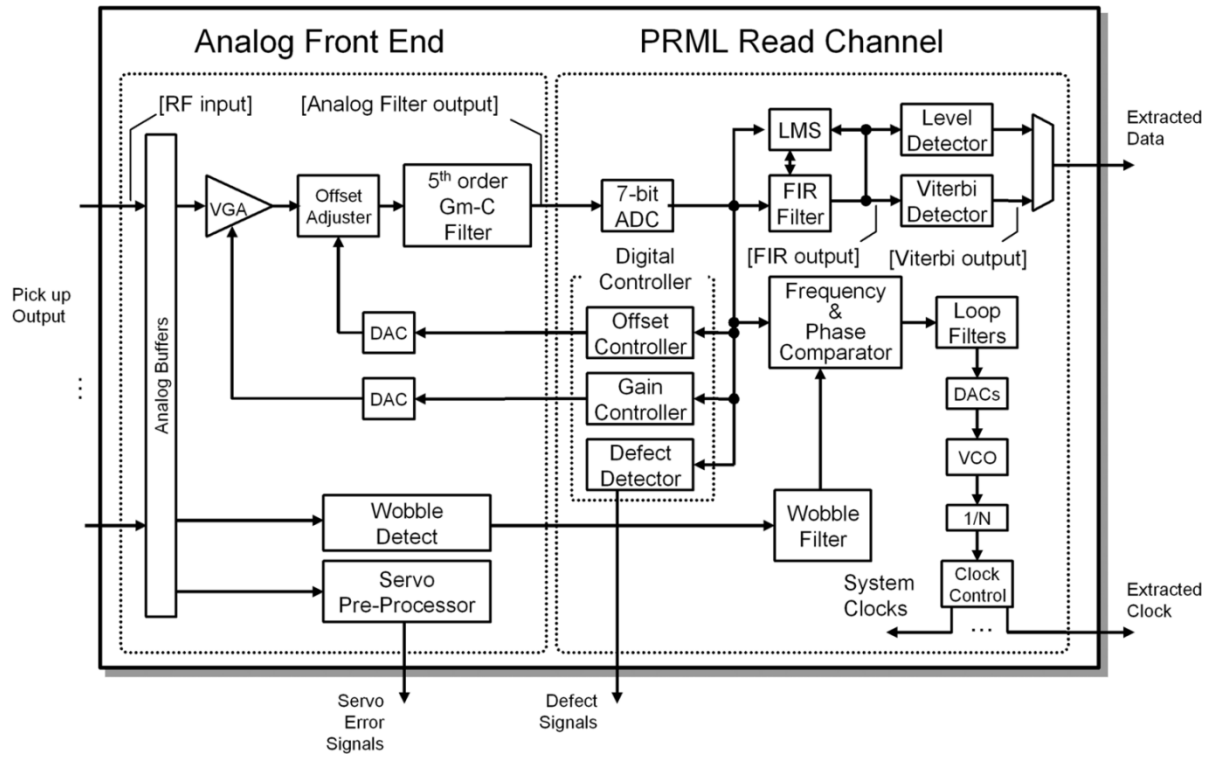

Fig. 4. Block diagram of the PRML read channel with the AFE.

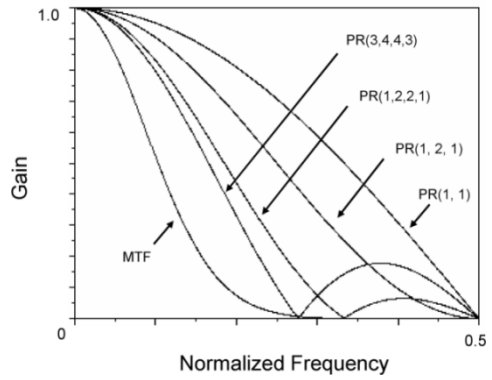

Fig. 5. Frequency responses of PR channels.

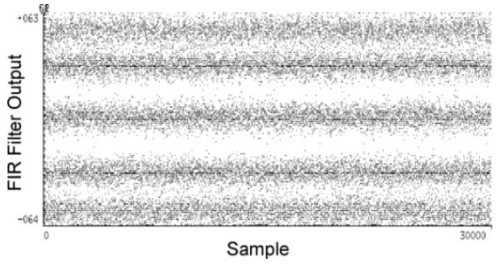

Fig. 6. Synchronized data at the FIR output.

The PLL consists of a frequency/phase comparator, digital loop filters, DACs, and a voltage-controlled oscillator (VCO). In the playback mode for DVD-ROM, the PLL can extract the clock signal by the frequency and phase detection of playback data. In contrast to this mode, in the playback mode for DVD-RAM, the wobble signal is needed for the frequency pull-in.

B. PR(3,4,4,3) Equalization

PR(3,4,4,3) architecture has been employed for this system. The reasons are described in the following. First, its characteristic is similar to modulation transfer function (MTF) characteristics of the readout signal from the OPU. Fig. 5 shows frequency characteristics for several PR architectures. The frequency characteristic of PR(3,4,4,3) is closest to that of the MTF characteristic. Thus, the pick-up data can be equalized without large degradation of frequency characteristics. Second, the equalization characteristic of PR(3,4,4,3) has good equalization balance. Fig. 6 shows measured equalized data in PR(3,4,4,3) architecture at DVD playback operation mode. This figure indicates that the balance of equalization is very good. The waveform is vertically symmetrical from the zero cross point and the intervals of neighboring equalized data are almost equal. The 8–16 modulation DVD guided by the (2,10) RLL rule has three channel bits minimum code length. Therefore, values after PR(3,4,4,3) equalization will split into just five values. This small number of split level is very effective for circuit simplicity and low power consumption.

Fig. 7 shows the architecture of the PR equalization in this SoC. The PR equalization is performed in the analog domain by the fifth-order G_m-C filter and in the digital domain by the adaptive FIR filter. In general, a biquad structure has a flat group delay characteristic when no boost characteristic is required. However, in the DVD system, a boost function is required to compensate the limited optical resolution of the pick up. Thus, a ladder-type structure is used [7]. This filter has wide tunable cutoff frequency range from 0.35 to 13 MHz and wide tunable boost range of 0 to 12 dB to support up to 2 times DVD and 16 times CD playback operation mode. In digital domain, the

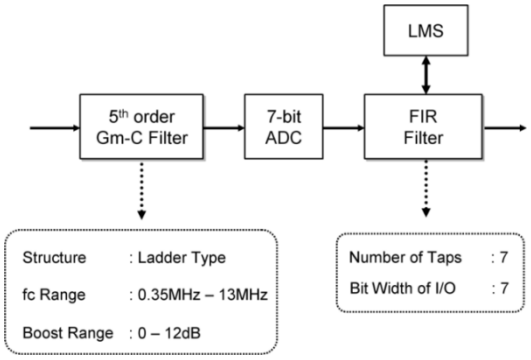

Fig. 7. Architecture of PR equalization in the SoC.

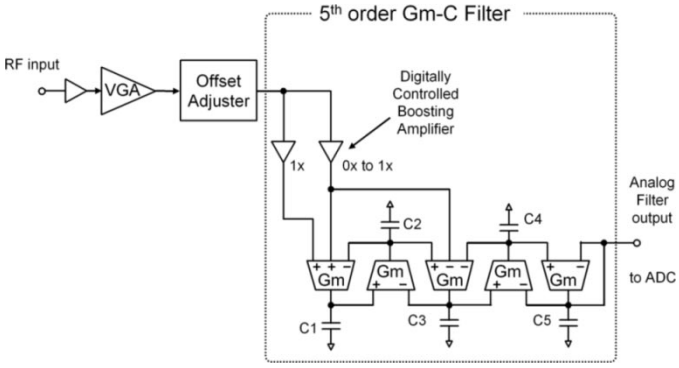

Fig. 8. Block diagram of the fifth-order G_m-C filter.

seven-tap adaptive FIR filter rectifies the residual equalization errors.

IV. Circuit Design in the PRML Read Channel

A. Fifth-Order G_m-C Filter

Fig. 8 shows the block diagram of the fifth-order G_m-C filter. In this system, this filter needs more than 20 times the tunable cutoff frequency range to support various operating modes. The simplest method to realize this is changing the capacitance according to cases. However, this method increases the analog area for the plural of capacitances. So, to support the wide tunable range of the cutoff frequency without increasing area, each G_m amplifier is constructed with four voltage-to-current converters (VICs), shown in Fig. 9. By switching the states of these VICs digitally, the wide tunable cutoff frequency range has been realized. The state of these VICs is programmable via 8-bit registers. Also, more than 12-dB boost control has been obtained by changing the gain of the digitally controlled boosting amplifier via 4-bit registers. The cutoff frequency setting and the boost setting are independently controlled.

B. Seven-Bit ADC

The 7-bit ADC is an important analog core for this SoC as well as the fifth-order G_m-C filter. Fig. 10 shows the block diagram of the 7-bit ADC in this SoC [8]–[10]. To reduce the power and area, a dynamic comparator and an interpolation circuit composed with gate-width-weighted transistors, instead of conventional resistor ladders, are used.

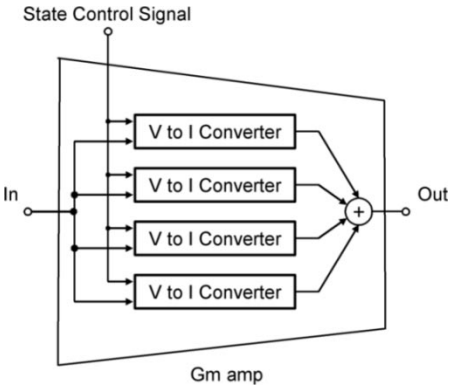

Fig. 9. Structure of G_m amplifier.

C. Viterbi Detector

Fig. 11 shows a block diagram of the Viterbi detector. It consists of branch metric, add–compare–select (ACS), and path memory. In this SoC, the Viterbi detector employs two new methodologies [11]. The first methodology is a new calculation procedure of ACS. In this method, the operation results of one time future are used to simplify the ACS formula. The second methodology is an original path memory architecture called Path Selection Signal Memory Architecture. The conventional path memory needs a huge number of registers to store all the temporally detected bit sequences corresponding to all survivor paths. By using the new path selection memory architecture, the number of registers for the survivor path can be reduced. These two new methodologies reduce power and area for the Viterbi detector by half.

V. SoC

Fig. 12 shows the chip microphotograph of this SoC. This SoC has been fabricated in 0.13-μm one-poly six-Cu CMOS process. The chip size of this SoC is 63.87 mm^2 (10.09 mm $\times$ 6.33 mm) containing 24 million transistors. This SoC integrates one DSP, two 32-bit CPUs, three processors, the PRML read channel with the AFE, and many other subsystems on the same die.

This SoC has been realized by using the mixed-signal technology, where highly sensitive analog circuits and complex digital circuits have been used in cooperation.

VI. Experimental Results

Fig. 13 shows a measured result for the gain characteristics of the AFE of this SoC at 2 times DVD playback operation mode. The lowest cutoff frequency is 2 MHz and the highest is 11.5 MHz at this setting. When the playback process is carried out, the optimal cutoff frequency is set up from this range at the initial learning period. Fig. 14 shows a measured result for the boost characteristic of the AFE when the cutoff frequency is set to 11.5 MHz. More than 12-dB boost range has been obtained by the digitally controlled boosting amplifier. When the playback process is carried out, the optimal boost value is set up from this range at the initial learning period similarly to the cutoff frequency setting. Fig. 15 shows measured group delay characteristics of the AFE when the cutoff frequency is set to

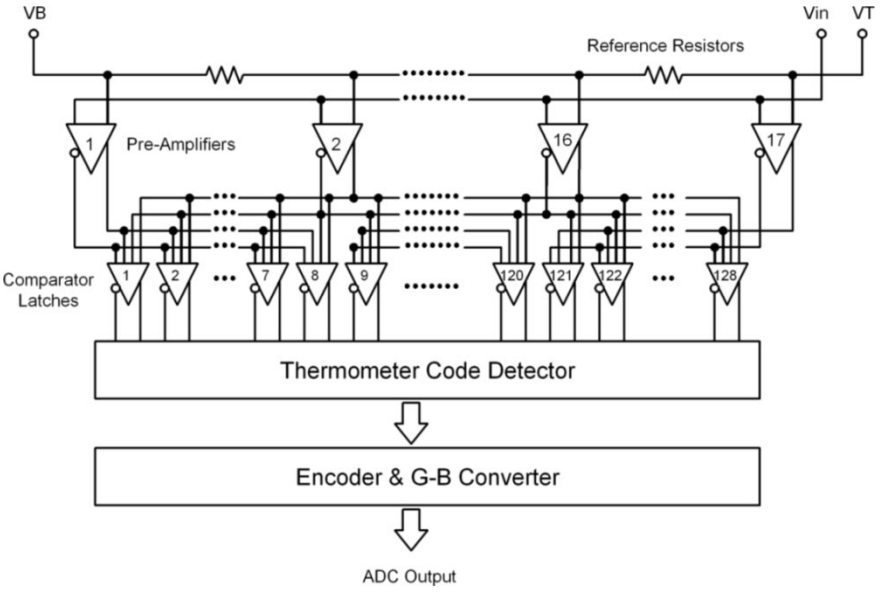

Fig. 10. Block diagram of 7-bit ADC.

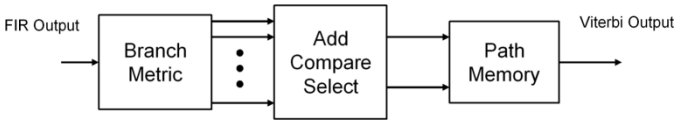

Fig. 11. Block diagram of Viterbi detector.

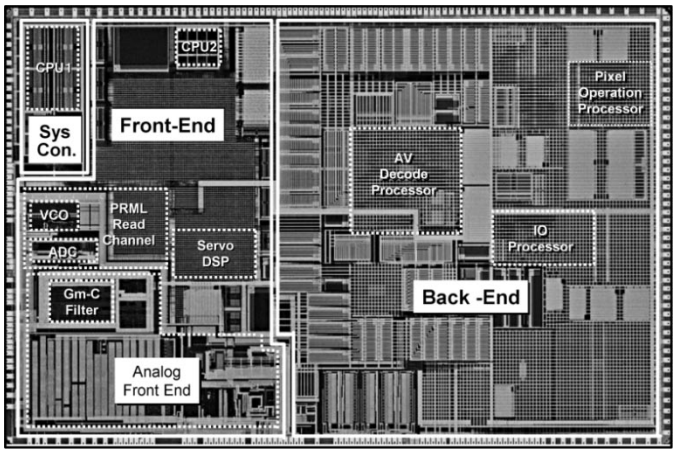

Fig. 12. SoC micrograph.

11.5 MHz. A flat group delay characteristic in the range of the playback signal is strongly needed, since the ripple of the group delay should be greatly concerned with the performance of the PLL for clock extraction.

The proposed SoC was designed so that the total group delay characteristic, from the output of the optical pick up to the input of the 7-bit ADC, would be as flat as possible. Consequently, as shown in Fig. 15, even if the boost value is changed, 2 ns or less of flat group delay ripple has been obtained in the desired frequency range. The value of 2 ns group delay ripple becomes 2% in terms of percentage for the desired frequency range.

Fig. 16 shows the measured carrier-to-noise ratio (C/N) characteristic of the AFE under the condition that a part of the PRML read channel is ON. A C/N value of more than 66 dB is obtained.

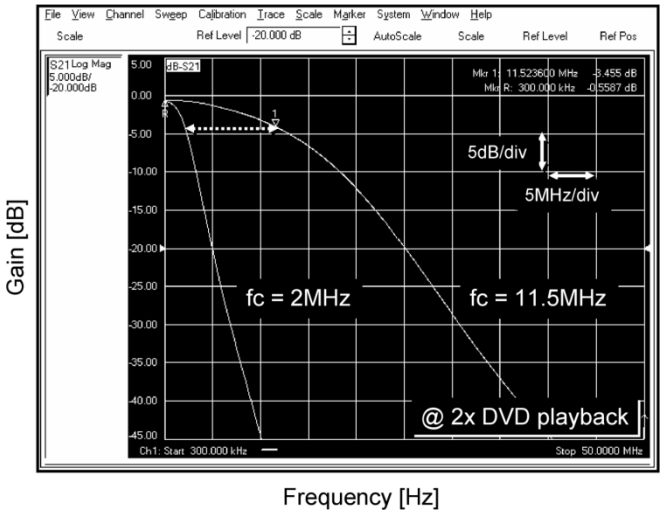

Fig. 13. Measured gain characteristics of the AFE.

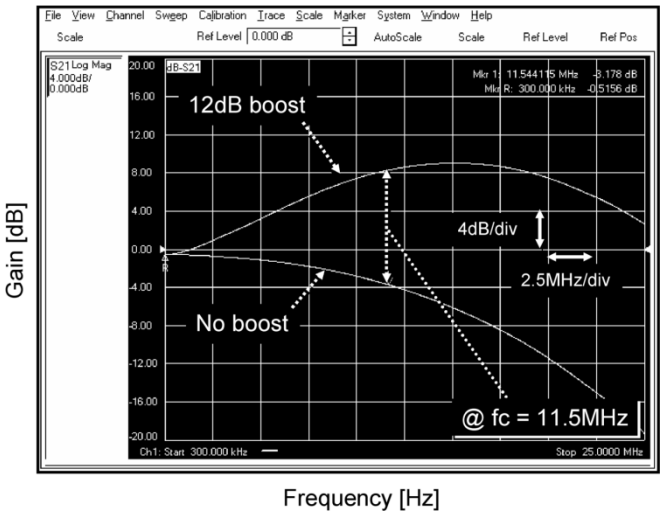

Fig. 14. Measured boost characteristics of the AFE.

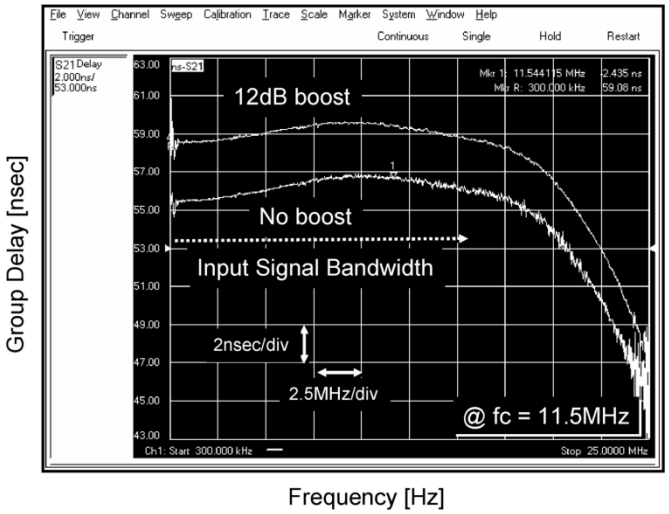

Fig. 15. Measured group delay characteristics of the AFE.

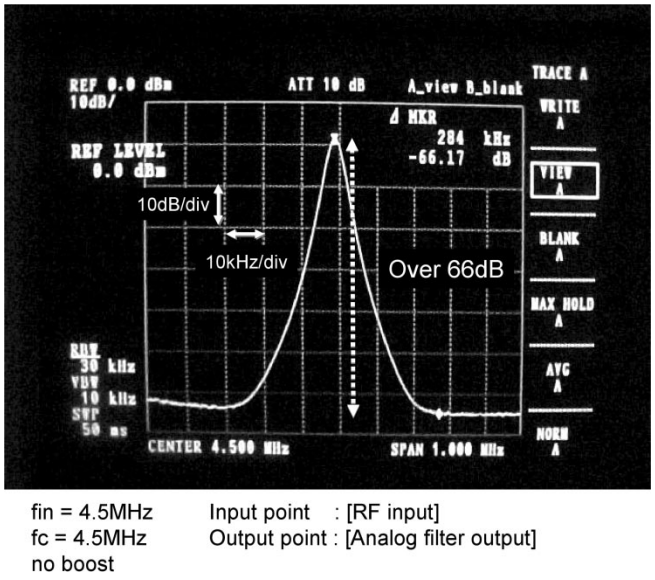

Fig. 16. Measured C/N characteristic of the AFE.

This good result is due to the following reasons. The first is the use of the triple-well structure to isolate the sensitive analog circuits from the noisy digital circuits. The second is the layout optimization considering the separation of power supplies and shield protection of sensitive analog signals, according to the size and use of analog cores. The last is the detailed verification in advance by the mixed-signal system simulator considering the noise and other nonideal factors.

The measured power consumption of the fifth-order G_m-C filter is 30 mW at 1.5 times DVD playback operation mode. The occupied area is 0.55 mm^2. The performance summary of the AFE is shown in Table I.

Table II summarizes the measured results of the 7-bit ADC in the SoC. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are less than 0.6 LSB and 1.0 LSB, respectively, for a 1-kHz input at 1.5 times DVD playback operation mode.

Fig. 17 shows measured equalized data at the adaptive FIR filter output when the defects appeared on the DVD disc. In the

TABLE I
AFE PERFORMANCE

VGA Gain Range	-6dB to 20dB
AFE fc Range	0.35MHz to 13 MHz
AFE Boost Range	0dB to 12dB (@ fc)
AFE GD Variation	< 2% (to 1.5fc)
AFE C/N	> 66dB
Power Supply	3.3V (Analog)
Gm-C Filter Power Consumption	30mW
Gm-C Filter Active Area	0.55mm^2

TABLE II
7-BIT ADC PERFORMANCE

Resolution		7 bit
INL/DNL	1kHz input	1.0LSB/0.6LSB (@1.5x DVD playback)
ENOB	10MHz input	6.1bit (@1.5x DVD playback)
Input Range		0.8Vp-p
Power Supply		3.3V (Analog), 1.5V (Digital)
Power Consumption		36mW (@ 1.5x DVD playback)
Active Area		0.35mm^2 (1.00mm x 0.35mm)

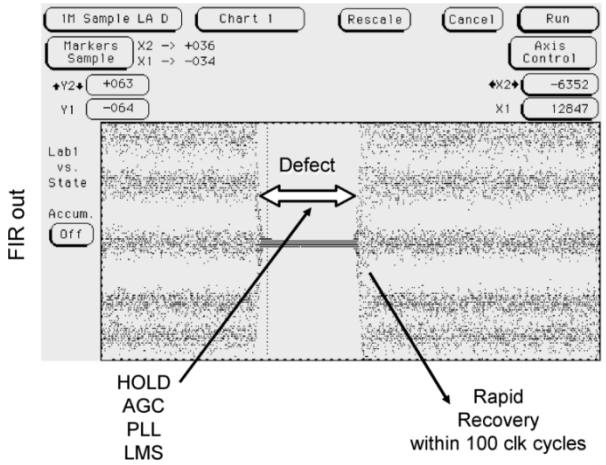

Fig. 17. Measured recovery performance after disc defects.

PR(3,4,4,3) architecture, the playback data is equalized to five values. When the defects were detected by the digital controller, feedback loops such as AGC, PLL, and LMS are in hold state. After the defects on the disc were disappeared, each feedback loop was recovered within 100 channel clock cycles without data slipping. This result shows the fast system recovery.

Fig. 18 shows measured BER as a function of focus offsets in the OPU. The conventional BER characteristic is the same as the state of the PRML OFF. Owing to the PRML read channel,

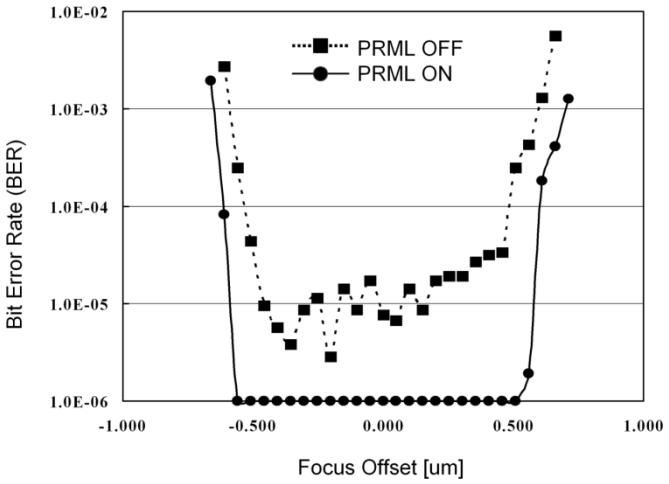

Fig. 18. Measured BER versus focus offsets.

TABLE III
SOC PERFORMANCE

PRML Read Channel Maximum Operating Speed	70M Sample/sec
Process Technology	0.13um 1PS 6Cu CMOS
Power Supply	3.3V (Analog), 1.5V (Digital)
Power Consumption	1.5W (@ 1.5x DVD playback) 2.0W (@ 2x DVD playback)
Die Size	63.87mm^2 (10.09mm x 6.33mm)
Number of Transistors	24 Million Transistors
Package	256 pin LQFP

the focus offset margin over ± 0.5 μm has been obtained with small BER of less than 10^{-6}. The bottom value of the BER is lower than 10^{-6} in the measurement. However, the reliability of the BER depends on the number of input data: 10^8 of input data are used in the measurement, and it is enough to set the bottom of the BER to 10^{-6}. Therefore, the bottom line of the BER is set to 10^{-6} in this figure.

Due to the optimization of clock latency and digitization of feedback loops, the loop characteristic of the PLL for the input signal jitter has been improved over than 2%, compared with the conventional system.

The measured power consumption is 1.5 W at 1.5 times DVD playback operation mode and 2.0 W at 2 times DVD playback operation mode. This allows us to use a low-cost 256–pin plastic package. Table III summarizes the performance of the proposed SoC.

VII. CONCLUSION

A fully integrated mixed-signal SoC for DVD player applications has been developed using 0.13-μm CMOS process. This SoC integrates all necessary analog and digital functions for signal processing in DVD player systems.

In spite of the use of 24 million transistors in a 63.87-mm^2 die, very low power consumption of 1.5 W has been attained at 1.5 times DVD playback operation mode and the value of power consumption is about 50% off compared with the conventional one.

The high-readability system has been constructed by the use of PRML signal processing with the high-performance AFE and mixed-signal optimization in the PRML read channel.

The proposed SoC supports up to 2 times DVD and 16 times CD playback operation mode. Its performance becomes much higher, but power consumption and total cost are reduced dramatically in comparison with conventional multichip solutions.

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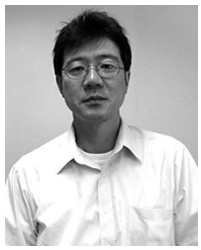

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