Design of A 1″× 1″, 512×512 Poly-Si TFT-LCD with Integrated 8-bit Parallel-Serial Digital Data Drivers

Won-Chul Shin, Seung-Woo Lee, Hoon-Ju Chung and Chul-Hi Han

Abstract

A 1"×1", 512×512 poly-Si TFT-LCD with a new integrated 8-bit parallel-serial digital data driver was proposed and designed. For high resolution, the proposed parallel-serial digital driver used serial video data rather than parallel ones. Thus, digital circuits for driving one column line could be integrated within very small width. The parallel-serial digital data driver comprised of shift registers, latches, and serial digital-to-analog converters (DAC's). We designed a 1"×1", 512×512 poly-Si TFT-LCD with integrated 8-bit parallel-serial digital data drivers by a circuit simulator which has physical-based analytical model of poly-Si TFT's. The fabricated shift register well operated at 2 MHz and V_{DD}=10V and the fabricated poly-Si TFT serial DAC's, which converts serial digital data to an analog signal, could convert one bit within 2.8 μs. The driver circuits for one data line occupied $8100 \times 50\ \mu m^2$ with 4 μm design rule.

Keywords : Parallel-serial digital data driver, poly-Si TFT-LCD, serial DAC

1. Introduction

Polycrystalline silicon thin-film transistor (Poly-Si TFT) technology has a potential to implement driver circuits on a glass substrate because poly-Si has higher carrier mobility than amorphous silicon. Integration of driver circuits reduces cost of the driver IC's and the number of interconnection to less than 10 %. Thus, many researchers have developed small size poly-Si thin-film transistor liquid crystal displays (TFT-LCD's) with analog integrated data driver circuits [1-4]. Recently, integrated data drivers with digital interface have become increasingly needed, but only a few researches have been tried [5-6]. We have developed a new digital data driver for high-density display [7]. The integrated driver, serial digital data driver [7], uses serial digital data to reduce the physical area of a data driver.

In this paper, we propose a small-size poly-Si TFT-LCD with fully integrated 8-bit digital data driver using a modified shift register and the parallel-serial data driver.

2. 1"×1" Poly-Si TFT-LCD

Table 1 shows the specifications of the poly-Si TFT-LCD. The schematic diagram of the display is shown in Fig. 1. Integrated data driver for a small-size display is the parallel-serial digital data driver without analog buffer. Because the data line capacitance is at most 5.5 pF, analog buffer is not necessary. Storage capacitors are formed over previous gate electrodes. To increase the storage capacitance, a capacitor is added under the previous gate line using doped active poly-Si film. For low leakage current, transistors with duel-gate are used as switching devices. The aperture ratio is 35 % and pixel capacitance including storage capacitance is 0.3 pF with the design rule of 4 μm. To suppress the leakage current more, a self-aligned offset structure using photoresist (PR) reflow is adopted [8]. The gate

Manuscript received February 26, 2001 ; accepted for publication April 15, 2001.

Won-Chul Shin is with the Comtec Systems Co., Ltd., 779-10 Daelim3-Dong, Youngdungpo-Ku, Seoul 150-816, Korea.

Seung-Woo Lee is with the Samsung Electronics Co., Ltd., San #24 Nongseo-Ri, Kiheung-Eup, Yongin-City, Kyunggi-Do 449-711, Korea

Hoon-Ju Chung and Chun-Hi Han are with the Department of Electrical Engineering & Computer Science, KAIST, 373-1 Kusong-Dong, Yusong-Ku, Daijon 305-701, Korea

E-mail : island@kaist.ac.kr **Tel** : +42 869-8044 **Fax** : +42 869-8530

material is Mo. The gate load resistance and capacitance are 2.5 kΩ and 200 pF, respectively.

TABLE 1. Display spectifications.

Size	1"×1"
Resolution	512×512
Inversion	Dot
Addressing	Digital line-at-a-time
Gray level	256
Frame frequency	60 Hz

2.1 Integrated parallel-serial digital data driver

To drive data lines, we use double banks of data drivers. As you can see in Fig. 1, the data drivers use parallel digital data rather than serial ones. Parallel digital data are stored in the first latches simultaneously. After storing the parallel data pixel by pixel in the first latches, all pixel data of one line are shifted to the second serially. During storage of parallel digital data of the next line in the first latches, the shifted digital data are converted to analog signals by serial DAC's. Thus, we refer to the driver as an integrated parallel-serial digital data driver.

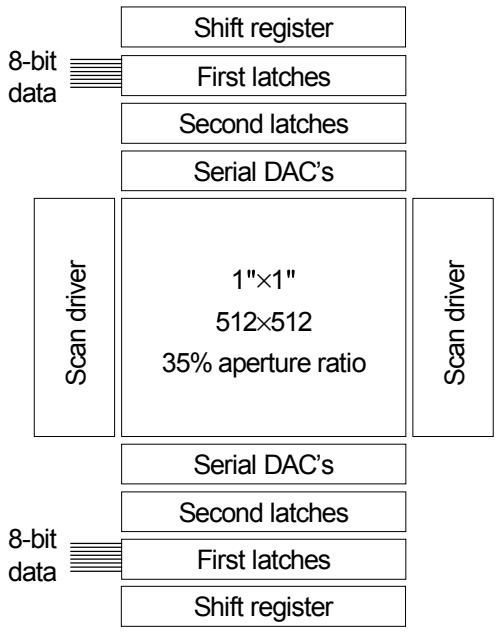


Fig. 1. Schematic diagram of the poly-Si TFT-LCD with fully integrated 8-bit parallel-serial digital drivers.

Shift register and data latches: We have devised a modified shift register and parallel-serial data driver to reduce time for data storage and conversion. The schematic diagram of the latches is shown in Fig. 2. Let us explain why the data driver should use parallel data and a modified shift register. Because parallel data are more available than serial data for video signal in digital systems, we use parallel data rather than serial data.

A shift register and a data latch have the same circuit structure. Thus, they have the same operation speed. The shift register outputs are used as switch control signal for data storage. Fig. 3 shows a modified shift register. The pulse width of the conventional shift register output is the same as the one period of the clock used in the shift register. In contrast with the conventional shift register, the pulse width of the modified shift register output has half the period of the clock. Let the clock speed be 1 MHz, 8 μs is needed for storing one 8-bit pixel data in the serial data driver [7]. If a serial data driver using serial data has 8 data bus lines, the first latches store 8 pixel data in 8 μs. However, it does not need such a long time of as much as 1 μs for storing when data are stored simultaneously. The modified shift register can generate shorter shift register outputs. There is no problem in storing data within 0.5 μs in the parallel-serial data driver with the modified shift-register. Thus, the first data latches with 8-bit parallel input can store 16 pixel data in 8 μs.

Serial BAC and Driving method: LCD requires polarity reversal driving. Thus, DAC's should convert digital data to a positive or a negative analog signal. We, however, divided DAC's into two DAC groups for positive and negative polarities, as shown in Fig. 4. When the driver-I drives odd data line for positive polarity, the driver-II addresses even data line for negative ones. During the next line time, polarity signal switches the connection of the driver-I to the even data line and that of the driver-II to the odd one. Dividing DAC's into two polarity groups gives two advantages; area efficiency and power consumption. DAC's for the same polarity shares common control signals and reference voltage lines. That's why we divide DAC's into two groups. Power consumption in DAC's can decrease because dynamic range of DAC's is reduced to half compared with the conventional method. After converting digital data into an analog signal, switch DAC2 and Write are closed. Then, the charges on C_1 and C_2 are shared with data line capacitance.

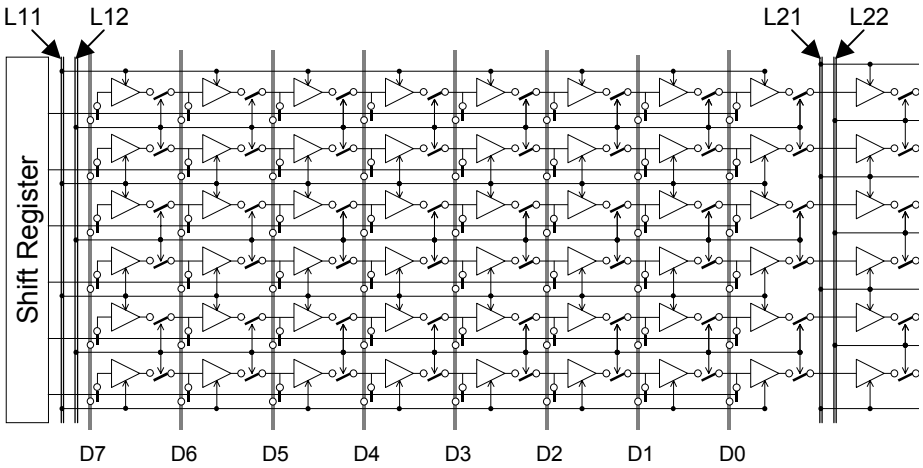


Fig. 2. Circuits diagram of the first latches and second latches. 8-bit digital data are stored in the first latches simultaneously according to the modified shift register.

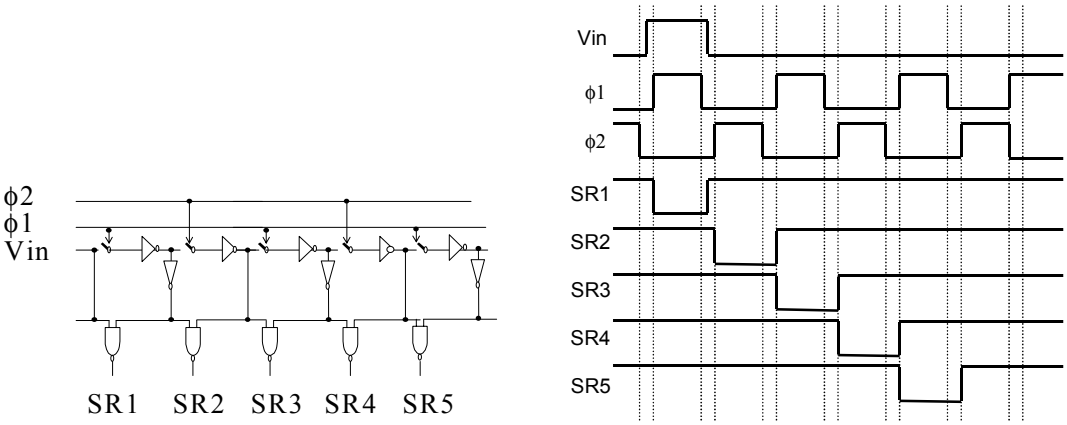


Fig. 3. Circuit diagram of a modified shift register.

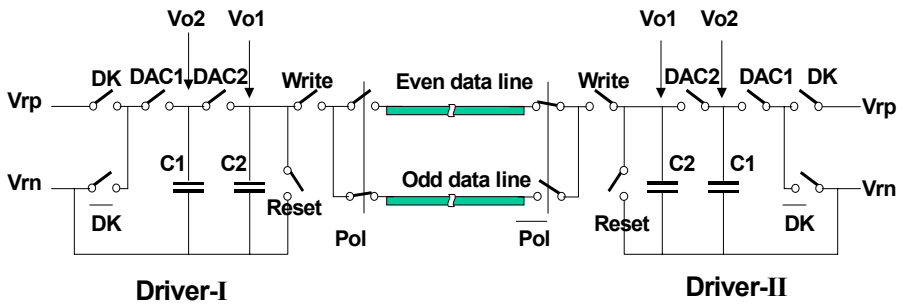


Fig. 4. Circuit diagram of data line driving circuits.

Fig. 5 shows timing diagram of control signals of the parallel-serial digital data driver. The total operation period is composed of a shifting period and a converting period. At the shifting period, the first latches send the data to the second latches with a fast clock speed. At the converting period, the first latches store new data while the serial DAC's convert digital data coming from the second latches to analog signals.

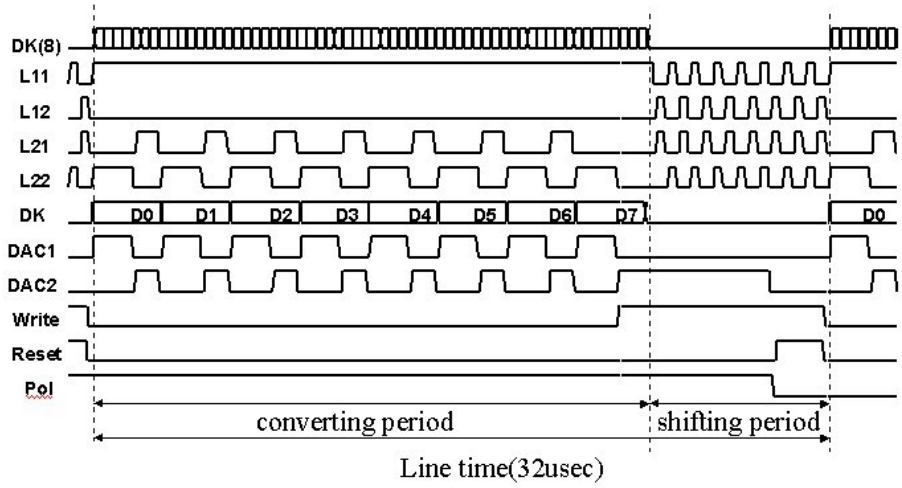


Fig. 5. Timing diagram of the parallel-serial digital data driver.

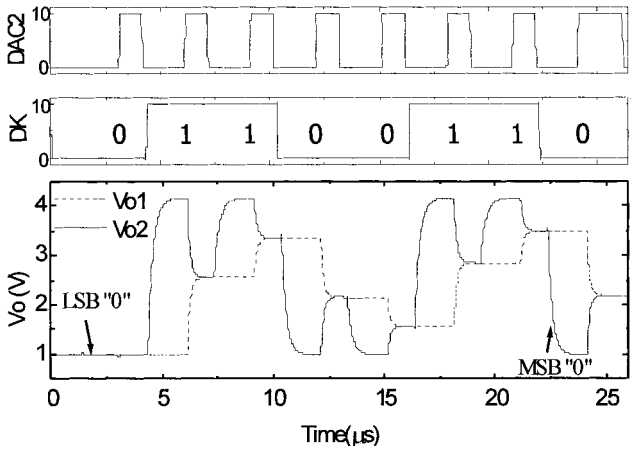


Fig. 6. Simulation results of serial DAC connected to data line.

We simulated the circuits with a circuit simulator, Aim-Spice, based on a physical-based analytical model proposed by Dr. Yang [9]. The parameters are extracted from the devices manufactured in our laboratory. The threshold voltages of n- and p-channel poly-Si TFT's were 0.9 and –2.1 V, respectively. The mobilities of n- and p-channel poly-Si TFT's were 60 and 55 cm^2/V, respectively. Simulation results show that the maximum operating frequency of a modified shift register is 2.2 MHz at V_{DD} = 10 V. On the assumption that operating frequency of shift register is 2 MHz, the data driver for the 1″×1″ LCD panel needs 10 blocks.

Fig. 6 shows the simulation results of data line driving circuit. The reference voltage Vrp is 4.14 V and Vrn is 1 V. The input digital value is '01100110'. The final output of the serial DAC is 2.189 V and the error is 3 mV, which is lower than 1 LSB. From the simulation results, it is found that 3 μs is sufficient to convert one bit into the designed serial DAC.

2.2 Fabrication and results

Starting wafer was quartz wafer. A 300 nm thick buffer oxide was deposited using atmospheric pressure chemical vapor deposition (APCVD). Then, a 50 nm-thick a-Si:H was deposited using plasma enhanced CVD (PECVD), followed by furnace annealing at 430 °C for de-hydrogenation. Crystallization of the a-Si:H film was performed using XeCl eximer laser annealing (ELA). Poly-Si film was patterned to form device islands and capacitor electrodes using reactive ion etching (RIE).

After capacitor electrode was formed by n^+ ion doping, 10 nm-thick gate oxide was grown in an ECR N_2O-plasma at a substrate temperature of 400 °C for 1 hour with a microwave power of 600 W. And then, a 40 nm thick gate oxide was deposited by low-pressure chemical vapor deposition (LPCVD). We used N_2O-plasma oxide for high device reliability and LPCVD oxide for high supply voltage. Mo gate material was sputtered, followed by pixel gate definition. By photoresist (PR) reflow and ion doping, self-aligned offset was formed. Circuit gate was defined and then, n- and p-channel sources/drains were doped by ion shower with 6 kV. The dopant were activated by furnace annealing at 900 °C in N_2 ambiennt. Deposited 500 nm thick interlayer CVD oxide was opened and then, Al-metallization was performed. After patterning the Al, ITO was sputtered, followed by ITO defining.

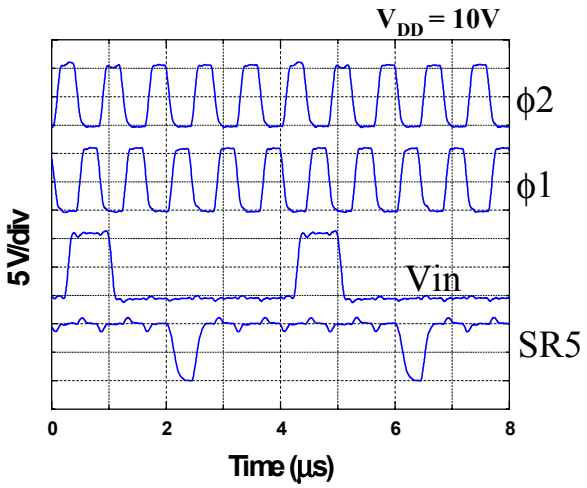


Fig. 7. Measured output of a modified shift register of data driver.

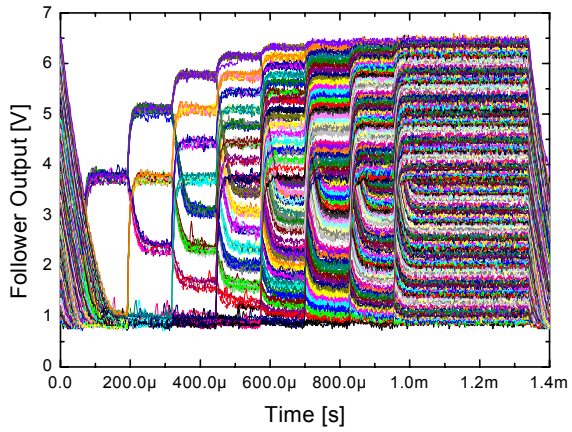
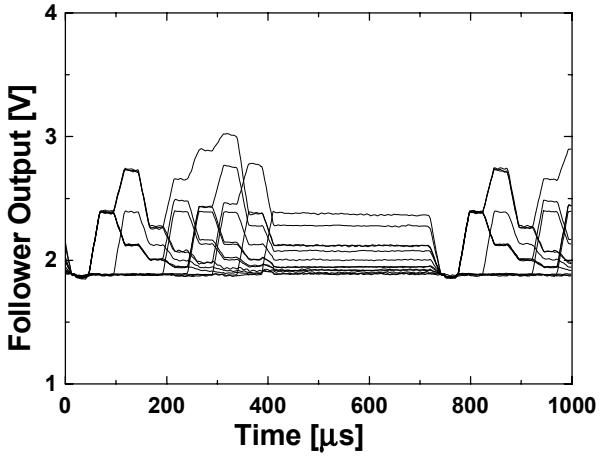
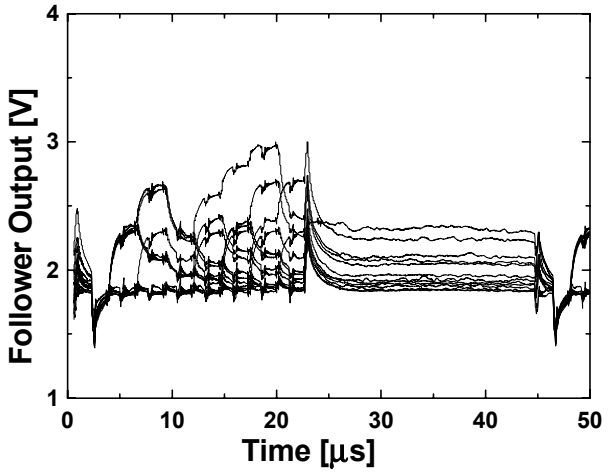


Fig. 8. Measured source follower outputs of 8-bit serial DAC without data line capacitance.

The threshold voltages of the fabricated n- and p-channel poly-Si TFT's were 3.1 and –2.7 V, respectively. The mobilities of n- and p-channel poly-Si TFT's were 73.4 and 57.8 cm^2/V, respectively. Fig. 7 shows output waveforms of a modified shift register of data driver. We confirmed that shift register well operated at 2 MHz and V_{DD}=10 V.



(a)



(b)

Fig. 9. Measured source follower outputs of 8-bit serial DAC with data line capacitance. (a) One bit conversion tiem = 50 μs, (b) One bit conversion time = 2.8 μs.

We measured the serial DAC without data line capacitance. The output voltage was measured through a simple source follower. The follower outputs for 8-bit converter were shown in Fig. 8. The nonlinearity was ±1 LSB. As can be seen in the figure, the conversion time is very long because of large capacitance load of the probe.

Figs. 9 (a) and (b) show output waveforms of 8-bit serial DAC with data line capacitance at one bit conversion time=50 μs and 2.8 μs, respectively. After converting digital data to analog data, the difference between analog voltages is 2.6 mV. Because 2.6 mV is lower than 1 LSB, 2.8 μs is sufficient for one bit conversion time. 2.8 μs was almost equal to our designed value of 3 μs. Fig. 10 shows normalized output of 8-bit serial DAC with data line capacitance. From fabrication results, differential nonlinearity error was about ±2 LSB. We used conventional single-gate poly-Si TFT's with high leakage current as switch devices. Nonlinearity of fabricated serial DAC's was mainly caused by charge loss of serial DAC's capacitors through the analog switches. If we use poly-Si TFT's with low leakage current, linearity of serial DAC's can be improved.

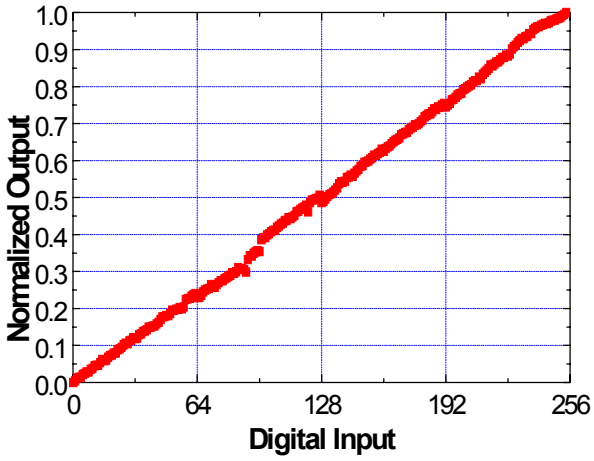


Fig. 10. Measured linearity of 8-bit serial DAC with data line capacitance.

3. Conclusions

We have proposed a new integrated 8-bit parallel-serial digital data driver and applied it to 1″×1″ TFT-LCD with 262,000 pixels. Parallel-serial digital data drivers use parallel digital data and data processing for high resolution. The manufactured shift register was well operating at 2 MHz and V_{DD}=10 V and 3 μs was sufficient for one bit conversion time of designed serial DAC's. Differential nonlinearity of serial DAC was about ± 2 LSB. But, linearity of serial DAC could be improved by reducing leakage current of switch devices. One data driver occupied 8100 × 50 μm^2 with 4 μm design rule. If the design rule decreased, the physical area of the driver could easily shrink. The development of small-size display utilizing the digital parallel-serial data driver will help us to develop a large-size display with high-information-contents with 150 ppi or higher.

References

[1] F. Okumura, H. Asada, K. Sera, K. Hirata, K. Kurakagi, Y. Hirai, S. Kaneko, K. Hamada, N. Kodama, A. Mineji, S. Saito, K. Ikeda, K. Miyakoshi, and M. Imajo, "A 76-mm (3-in.) driver-integrated poly-Si TFT-LCD light valve," SID 94, p. 79, 1994.

[2] H. Nakamura, Y. Masuda, H. Sato, K. Mori, M. Kobayashi, T. Nakazono, T. Kanaya, M. Nakagawa, and N. harada, "3.3-inch, 1.9 Mpixel integrated driver poly-Si TFT-LCD for HDTV projector," ISSCC 94, p. 154, 1994.

[3] K. Kaise, H. Ichikawa, T. Fukuda, H. Kitai, F. Abe, N. Furuto, H. Komatsu, Y. Tsubota, Y. Saito, and H. Yamanaka, "A 1.43-in 768K dots TFT LCD for a single panel projection TF with buried micro lens array," AMLCD 96, p. 205, 1996.

[4] H. Sekine, H. Asada, Y. Ogawa, K. Ozawa, K. Mochinzuki, F. Okumura, and S. Kaneko, "Amplifier compensation method for a poly-Si TFT LCLV with an integrated data-driver," IDW 97, p. 45, 1997.

[5] Y. Matsueda, S. Inoue, S. Takenaka, T. Ozawa, S. Fujikawa, T. Nakazawa, and H. Ohshima, "Low-temperature poly-Si TFT-LCD with integrated 6-bit digital data drivers," SID 96, p. 21, 1996.

[6] M. Osame, M. Azami, J. Koyama, Y. Ogata, H. Ohtani, and S. Yamazaki, "A 2.6-in. poly-Si TFT-LCD HDTV display with monolithic integrated 8-bit digital data drivers," SID 98, p. 1059, 1998.

[7] Seung-Woo Lee, Hoon-Ju Chung and Chul-Hi Han, "A novel integrated serial digital data driver for poly-Si TFT-LCD's," 19th IDRC (Euro Display 99), p. 465, 1999.

[8] Jung-In Han and Chul-Hi Han, "A self-aligned offset polysilicon thin-film transistor using photoresist reflow," IEEE EDL, vol. 20, p. 476, 1999.

[9] Gi-Young Yang, Sung-hoi Hur, and Chul-Hi Han, "A physical-based analytical turn-on model polysilicon thin film transistor for circuit simulation," IEEE Trans. on Electron Devices, vol. 46, no. 1, p. 165, 1999.