40-Gb/s 2:1 Multiplexer and 1:2 Demultiplexer in 120-nm Standard CMOS

Daniel Kehrer, Hans-Dieter Wohlmuth, Herbert Knapp, Martin Wurzer, and Arpad L. Scholtz

***Abstract*—We present an integrated 2:1 multiplexer and a companion 1:2 demultiplexer in CMOS. Both integrated circuits (ICs) operate up to a bit rate of 40 Gb/s. The 2:1 multiplexer features two in-phase data inputs which are achieved by a master–slave flip-flop and a master–slave–master flip-flop. Current-mode logic is used because of the higher speed compared to static CMOS and the robustness against common-mode disturbances. The multiplexer uses no output buffer and directly drives the 50-Ω environment. An inductance connected in series to the output in combination with shunt peaking is used to enhance the bandwidth of the multiplexer. Fully symmetric on-chip inductors are used for peaking. The inductors are mutually coupled to save chip area. Lumped equivalent models of both peaking inductors allow optimization of the circuit. The ICs are fabricated in a 120-nm standard CMOS technology and use 1.5-V supply voltage. Measured eye diagrams of both ICs demonstrate their performance.**

***Index Terms*—Demultiplexer, CMOS, current-mode logic, inductive peaking, multiplexer.**

I. Introduction

TODAY'S serial data communication systems operate at throughputs between 10 and 40 Gb/s. Up to now, communications integrated circuits (ICs) operating at such high speeds were engineered using GaAs, InP, or SiGe bipolar technologies. Heavy emphasis was placed on finding the right match between circuit techniques and fabrication technology.

This work demonstrates CMOS to be a viable alternative for broad-band circuit design at 10+ Gb/s. The approach is very economical because of the lower production costs, higher yield, and integration density. Recent achievements in CMOS multiplexer and demultiplexer designs which fully exploit the speed potential of a 120-nm standard CMOS technology are presented. Advanced circuit techniques and a state-of-the-art fabrication process are combined to extend speed limits.

Data multiplexer (MUX) and data demultiplexer (DEMUX) are key blocks in high-speed data communication systems. Current 2:1 MUX already achieve operating speeds of 20+ Gb/s in CMOS [1], [2]. A 30-Gb/s DEMUX in CMOS has been reported [3] and a complete 10-Gb/s transmitter/receiver with an integrated 16:1 MUX/DEMUX in CMOS has been published [4], [5].

We have designed a 40-Gb/s 2:1 MUX and 1:2 DEMUX using a 120-nm standard CMOS process with six-layer copper metallization. The manufactured nMOS transistors have an f_t of 100 GHz and an $f_{\max}$ of 50 GHz [6]. All subcircuits of the MUX and DEMUX ICs use current-mode logic (CML) with differential signals. Compared to conventional static CMOS logic, CML allows a reduction of the internal voltage swing. The lower internal voltage swing is essential for high switching speeds. To reach this speed, the 2:1 multiplexer uses shunt and series inductive peaking, which nearly doubles the bandwidth.

Manuscript received April 16, 2003; revised June 23, 2003.

The authors are with Infineon Technologies AG, D-81739 Munich, Germany (e-mail: daniel.kehrer@infineon.com).

Digital Object Identifier 10.1109/JSSC.2003.818297

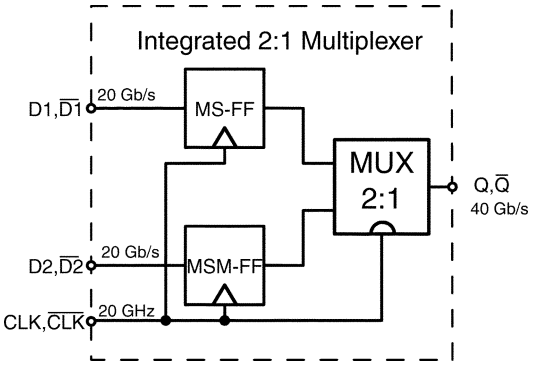


Fig. 1. Block diagram of the 2:1 MUX IC.

II. 2:1 MUX Circuit

The 2:1 MUX IC (Fig. 1) consists of a master–slave flip-flop (MS-FF), a master–slave–master flip-flop (MSM-FF), and a multiplexer stage (MUX 2:1). The 2:1 MUX IC features two in-phase differential 20-Gb/s input signals, D1 and D2. The in-phase data input is necessary for higher integration levels like a 4:1 multiplexer. The 90° phase shift between the MUX stage inputs is achieved by adding an extra latch to one path (MSM-FF). Each latch adds a delay of 90° to the data. The latches apply a high voltage swing of 600 mV to the MUX stage inputs, which is necessary due to the low gain of the transistors at such high frequencies. Finally, the data streams D1 and D2 are multiplexed by the 2:1 MUX stage to a 40-Gb/s output data stream. The 2:1 MUX IC uses no output buffer.

Fig. 2 shows the schematic diagram of the MUX circuit. Like all CML gates, the MUX works as a current switch. All transistors of the MUX circuit are nMOS devices because of their higher speed compared to pMOS transistors. Except for the current-source transistors, low-V_t devices with gate lengths of 120 nm are used.

The current source consists of two stacked nMOS transistors with a gate length of 0.18 μm. A regular-V_t device ($V_t \approx 400$ mV) and a low-V_t device ($V_t \approx 300$ mV) are connected in series. This configuration increases the output resistance of the

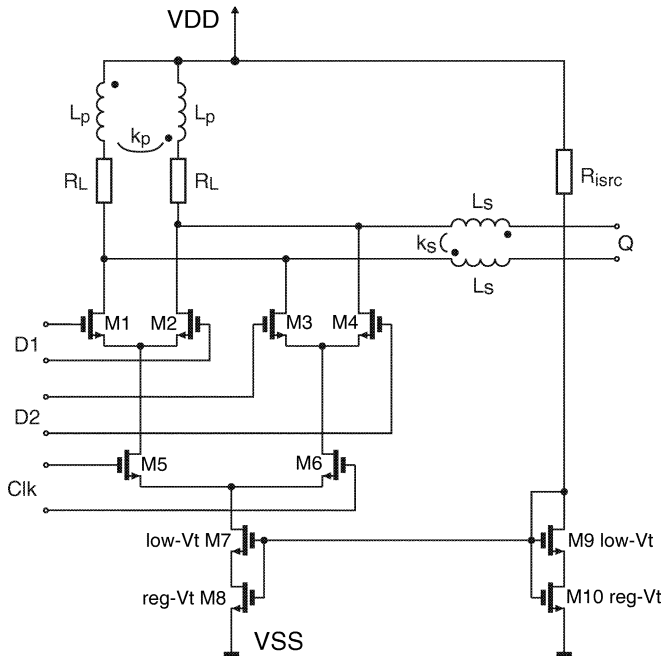


Fig. 2. Schematic diagram of the 2:1 multiplexer stage.

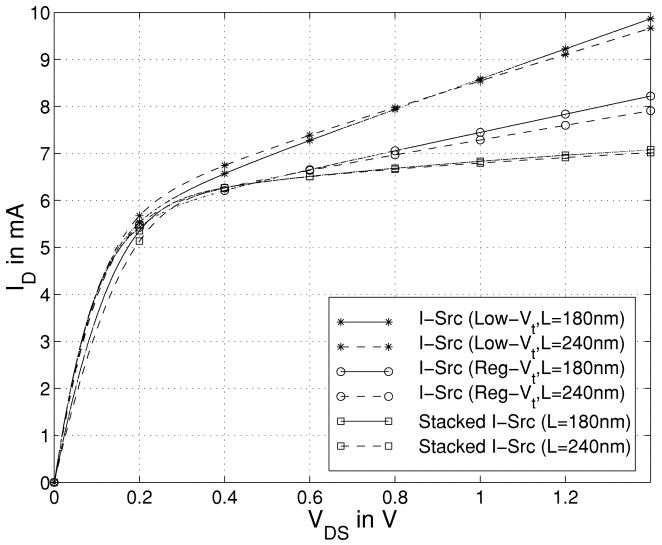


Fig. 3. Current-source characteristic of conventional current mirror with low-V_T and regular-V_T devices and the stacked current source.

current source. Neglecting the body effect, the output resistance of the stacked current source can be written as

$$R_{\rm o} = r_{\rm o} + r_{\rm o}(1 + g_m r_{\rm o}) = 2r_{\rm o} + g_m r_{\rm o}^2 \approx g_m r_{\rm o}^2 \qquad (1)$$

where $r_{\rm o}$ is the output resistance of M7 and M8, assuming that they have the same output resistance.

Fig. 3 shows the drain current $I_{\rm D}$ versus drain–source voltage $V_{\rm DS}$ (load voltage) of the current source. The stacked current source has flat current-source behavior. The main disadvantage of stacked current sources is the higher operating voltage to keep the devices in saturation. However, the minimum operating voltage is very close to the minimum operating voltage of the conventional current mirror.

In the design of the multiplexer stage, the stacked current source with device gate length of 180 nm has been chosen. The current source works above 350-mV load voltage.

The MUX stage uses series gating between clock and data inputs. All transistors in the MUX stage data path are of the same size and are 3/5 the width of the clock transistors. The lower width of the data path devices reduces the parasitic capacitance on the output. The MUX uses 70-Ω polysilicon load resistors as low-capacitance loads. The tail current is set to 7 mA. The dc level of the sinusoidal clock signal is $V_{\rm DD}/2$.

III. Inductive Network

Inductive networks can be used to increase the bandwidth of CML circuits. The most common technique using inductive networks is shunt peaking. An inductance is connected in series to the load resistor of the CML circuit. This technique can increase the bandwidth of the circuit by approximately 80% if an overshoot of 8% is acceptable and ideal inductors are used. The inductor can be realized as bond inductances or as on-chip inductors. Quality factors (Q factors) of on-chip inductors are lower than bond inductances, therefore, the latter are often used for peaking [7], but also, on-chip inductors are proposed for use as shunt peaking inductors [8], [9].

However, additional pads for bond inductors or on-chip inductors require large chip area. Inductors cannot be used in every stage to enhance the bandwidth because this is hardly acceptable for the required chip area. In the case of multiplexers, it makes sense to use inductive networks only at the fastest multiplexer of the system. On-chip inductors have low Q factors due to the limited conductivity of the metal, substrate loss, and parasitic capacitance. Shunt peaking can improve the bandwidth by approximately 50%, assuming the use of on-chip inductors.

Another technique to enhance the bandwidth of CML circuits is series peaking. An inductance is connected in series to the output of the CML circuit. The output network acts as a filter which consists of various parasitic capacitances, load resistors, bond inductances, and on-chip inductors. Series peaking can additionally improve the bandwidth by approximately 45% when combined with shunt peaking. Series peaking makes sense if it is used in combination with shunt peaking. If only series peaking is used, then the enhancement in bandwidth is low. Using series peaking and shunt peaking can nearly double the bandwidth of a CML circuit. The 2:1 MUX IC uses both peaking techniques to achieve high operating speeds.

A. Shunt and Series Peaking

Fig. 4 shows the equivalent circuit of the output network of a CML circuit with shunt and series peaking. The output network is a fifth-order system consisting of various parasitics, load resistors, a shunt, and a series peaking inductor. The shunt peaking inductor L_p is connected in series to the load resistor R_L while the series peaking inductor L_s is connected between the circuit and the pads. The differential signals allow mutual coupling of the inductors denoted by the coupling coefficients k_p and k_s.

The load resistors R_L of the CML circuit are realized as polysilicon resistors. The load resistors R_L are 70 Ω, which is a compromise between high voltage swing and reasonable output

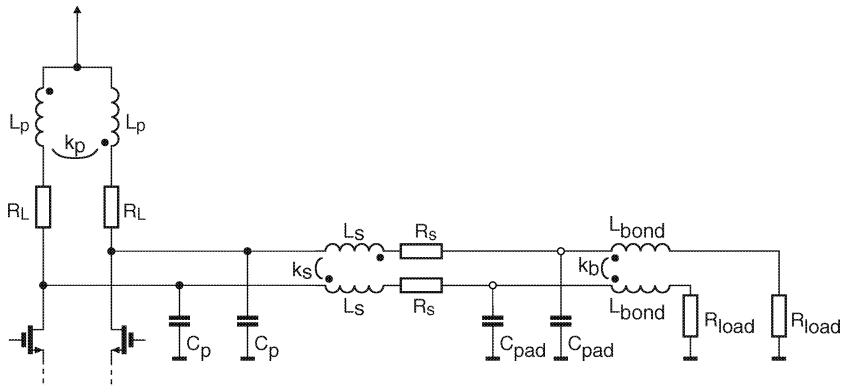


Fig. 4. Equivalent circuit of the inductive output network.

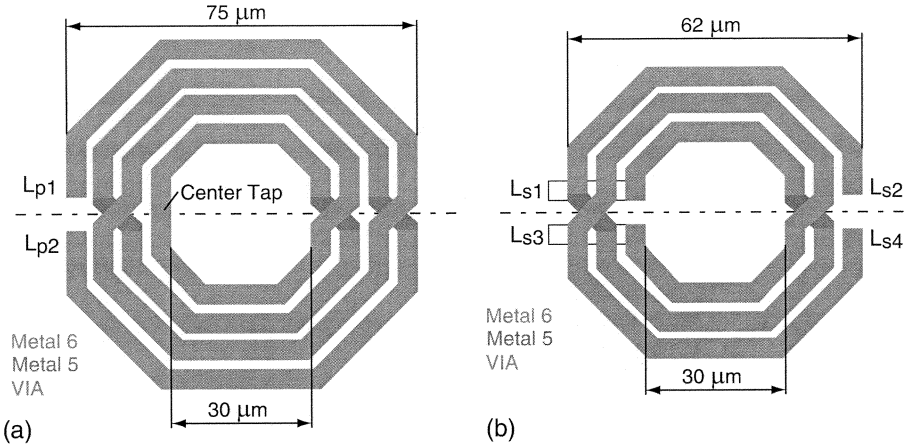


Fig. 5. Layouts of the symmetric peaking coils. (a) Shunt peaking inductor. (b) Series peaking inductor.

matching. The external load is $R_{\rm load} = 50\,\Omega$. The series resistance of the nonideal inductor L_p is added to the load resistor R_L.

Parasitic capacitances are denoted in Fig. 4 by C_p and are the sum of

$$C_p = C_{\rm tran} + C_{\rm R} + C_{\rm metal} \tag{2}$$

where $C_{\rm tran}$ are the transistor parasitics, $C_{\rm R}$ are the parasitics of the poly resistor R_L, and $C_{\rm metal}$ are the interconnect parasitics. The pad capacitance $C_{\rm pad}$ is separated by the series inductor from C_p. The nonideal series inductor L_S has a series resistance R_S due to the limited conductivity of the metal.

The bonding wires are denoted in Fig. 4 by $L_{\rm bond}$. The wires are mutually coupled as denoted by $k_{\rm b}$. The effective bond inductance seen on each side is

$$L_{\rm bond,eff} = L_{\rm bond}(1 - k_{\rm b}). \tag{3}$$

The coupling coefficient of the bonding wires in our setup is in the range of $k_{\rm b} = 0.2$. The parasitic capacitances C_p, the pad capacitance $C_{\rm pad}$, and the bond inductance $L_{\rm bond}$ are kept as small as possible. We can optimize the shunt peaking inductor L_p and the series peaking inductor L_s to improve the bandwidth.

IV. Peaking Inductors

The design issues concerning inductive peaking treat an ideal inductor with an inductor series resistance. This model illustrates how to optimize the inductance values of the shunt and series peaking inductors. An on-chip inductor has a complex model and behaves differently then an ideal inductor. Many investigations have been done to make a precise high-frequency characterization of inductors [10], [11]. In each application, different behaviors of the inductors have been observed.

The multiplexer shown in Fig. 2 is a fully differential design with fully symmetric peaking inductors. Fig. 5 shows the layouts of the shunt peaking inductor and the series peaking inductor used in the design of the 2:1 MUX IC.

The shunt peaking inductor shown in Fig. 5(a) has a center tap where the supply voltage is applied. The two ports $L_{\rm p1}$ and $L_{\rm p2}$ are connected to the load resistors R_L of the circuit diagram shown in Fig. 2. The turns of the inductor consist only of Metal 6. The crossover sections use Metal 5. The conductor material of Metal 5 and Metal 6 is copper with a thickness $t = 0.55\,\mu$m. The inner diameter is 30 μm and the outer diameter is 75 μm. The spacing between the turns is kept wide to reduce turn-to-turn parasitic capacitance. The turns have a spacing of 2 μm and a width of 4 μm.

Fig. 6 shows the equivalent circuit of the symmetric shunt peaking inductor which is used for the simulations. The symmetric inductor has a coupling coefficient of $k_p = 0.67$. The inductance is $L_p = 0.26$ nH. The effective inductance seen on each side can be calculated as $L_{\rm shunt} = L_p(1+k_p) = 0.44$ nH. The series resistance of the coil, denoted by R_p, is calculated for $f = 20$ GHz. The parasitic capacitance from the inductor to

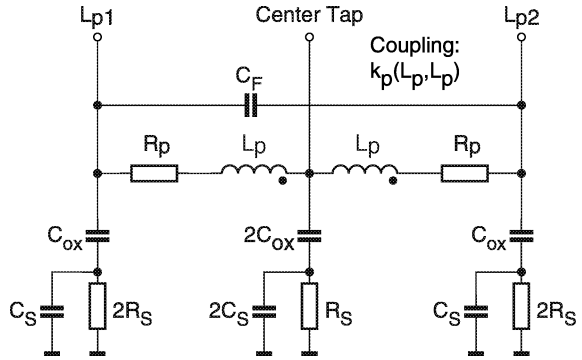


Fig. 6. Equivalent circuit of the symmetric shunt peaking coil for SPICE simulations.

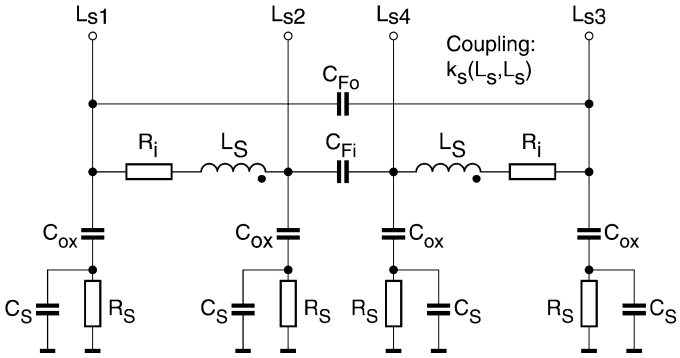


Fig. 7. Equivalent circuit of the symmetric series peaking coil for SPICE simulations.

the substrate is represented by $C_{\rm ox}$. The substrate parasitics and losses are denoted by C_S and R_S. The interwinding capacitance is modeled by C_F.

The extraction of the parameters is done with an in-house tool [11] which uses two cores [12], [13] to extract the inductance and the parasitic capacitances.

The series peaking inductor is shown in Fig. 5(b). The ports $L_{\rm s1}$ and $L_{\rm s3}$ are connected to the drains of transistors M1–M4 of the multiplexer circuit shown in Fig. 2. The coil has three turns and consists of Metal 6 and Metal 5 connected in parallel. The inner diameter is 30 μm and the outer diameter is 62 μm.

Fig. 7 shows the equivalent circuit of the symmetric series peaking inductor which is used for the simulation. The symmetric inductor has a coupling coefficient of $k_s = 0.53$. The inductance is $L_s = 0.15$ nH. The effective inductance seen on each side is $L_{\rm series} = L_s(1 + k_s) = 0.24$ nH.

The series peaking coil is connected in series to the output. Therefore, it is highly desirable to get a series inductor with a high Q factor. The series resistance R_i causes additional losses at the output transfer function of the multiplexer and should, therefore, be kept as small as possible. The oxide capacitance $C_{\rm ox}$ can be added to the parasitics C_p and $C_{\rm pad}$ of Fig. 4. A high substrate resistance R_S minimizes the loss due to substrate coupling.

On the other hand, the series resistance R_p of the shunt peaking inductor is in series to the load resistor R_L of the multiplexer and is, therefore, not critical. The quality factor $Q = {\rm Im}\{Z\}/{\rm Re}\{Z\}$ of the shunt peaking inductor is mainly determined by $Q = \omega L_{\rm shunt}/R_L$. It is not necessary to optimize the shunt peaking inductor for a high Q factor.

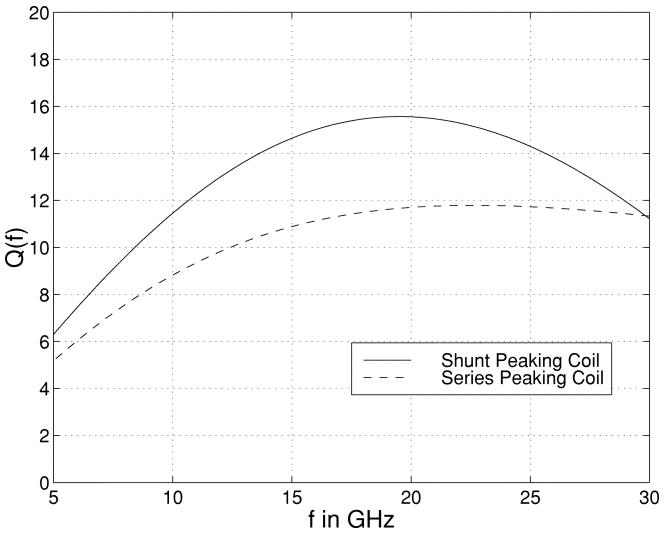


Fig. 8. Simulated quality factor Q versus frequency of the shunt peaking coil and series peaking coil.

Fig. 8 shows the simulated Q factor of the shunt peaking coil and the series peaking coil versus frequency using the models of Fig. 6 and Fig. 7. In the operating mode of the shunt peaking inductor, the parasitics of the center tap (Fig. 6) are shortened to the supply voltage. Therefore, the shunt peaking inductor has a high Q factor of $Q \approx 15$ at 20 GHz.

In contrast, all parasitics of the series peaking inductor lower the Q factor. The series peaking inductor has a simulated Q factor of $Q \approx 12$ at a frequency of 20 GHz.

A. Simulations Using Inductor Models for Shunt and Series Peaking

The models for the shunt peaking coil and the series peaking coil extracted from the inductor geometries can be used in SPICE simulations. The models allow optimization of the circuit. Fig. 9 shows the simulation of the small-signal transfer function of the output network when the inductor models of Fig. 6 and Fig. 7 are used. The simulations are produced with $C_p = 60$ fF, $L_{\rm bond} = 0.1$ nH, $R_L = 70\,\Omega$, and $R_{\rm load} = 50\,\Omega$.

The logarithmic frequency axis in Fig. 9 is normalized to $f_0 = 22.2$ GHz which is the -3-dB cutoff frequency when no inductive peaking is used. A bandwidth improvement of 50% can be achieved when shunt peaking is used. The simulations show that a bandwidth of $f_{-3{\rm dB}} = 1.97 f_0 = 43.7$ GHz can be achieved by using shunt and series peaking.

However, the bandwidth of the output network is not all that must be observed. It can be shown that a constant group delay is highly desirable for digital communications [8], [14]. In the output network, only the peaking inductors are varied and, therefore, a Bessel characteristic, which would be optimum, is not possible.

Fig. 10 shows the simulated group delay τ_G of the output network when the extended inductor models are used. A flat group delay is highly desirable in order to omit intersymbol interference. However, the group delay is not flat in any case at frequencies above f_0. If shunt and series peaking is used the group delay has a simulated delta of $\Delta\tau_G = 20$ ps up to $\approx 2f_0$.

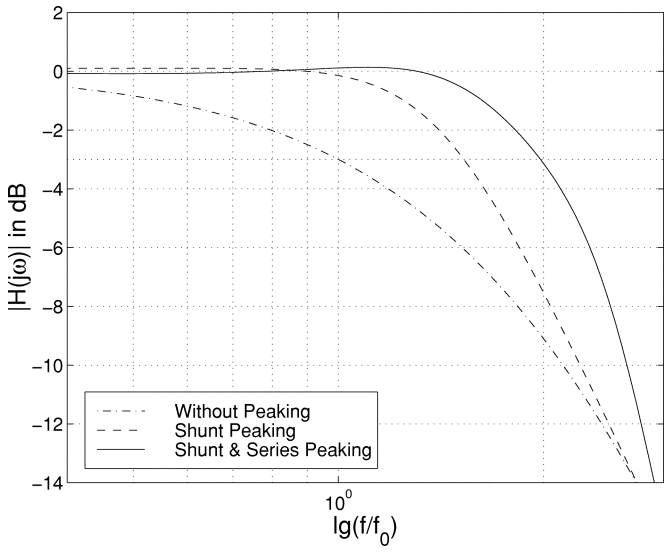


Fig. 9. Simulated transfer function of the output network using the inductor models of Fig. 6 and Fig. 7 ($f_0 = 22.2$ GHz).

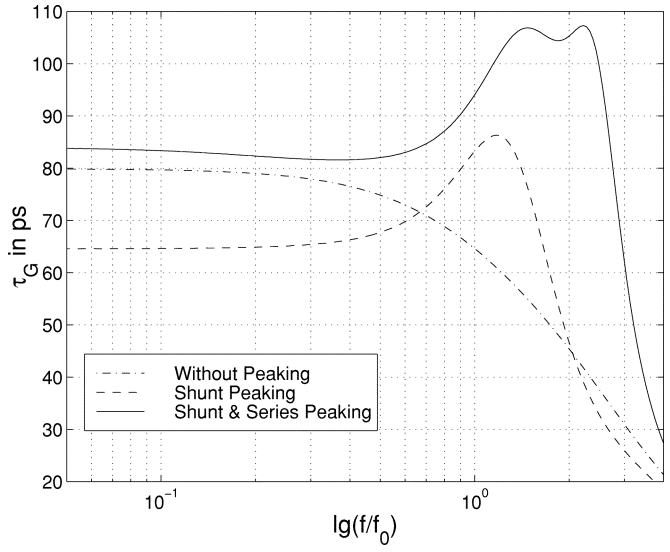


Fig. 10. Simulated group delay τ_G of the output network with the inductor models ($f_0 = 22.2$ GHz).

The affect of shunt and series peaking in combination can be seen in the step response of the multiplexer circuit. While the transfer function only shows the small-signal behavior, the step response shows the large-signal behavior of the multiplexer circuit. On the clock input of the MUX circuit, a step signal with 2×400 mV is applied. Fig. 11 shows the step response of the MUX circuit (single-ended signal). The simulated rise time (20%–80%) when no inductive peaking is used is $t_r = 12.3$ ps. When shunt peaking is used, the rise time is $t_r = 9.2$ ps, which is 26% lower. When series and shunt peaking is used, the rise time is $t_r = 8.6$ ps, which is 31% lower compared with no-peaking.

Series and shunt peaking in combination causes an overshoot of about 6% in the step response. In reality, a rectangular clock never occurs when the circuit operates at high data rates. Clock and data signals are sinusoidal waveforms.

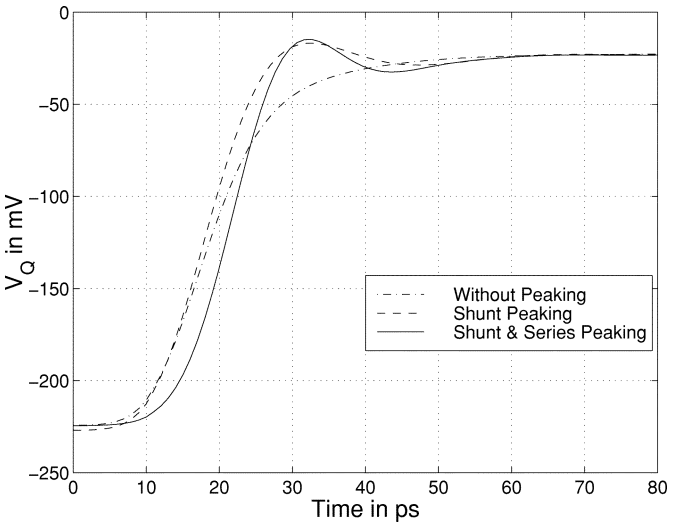


Fig. 11. Simulated step response of the multiplexer with the inductor models (single ended signal).

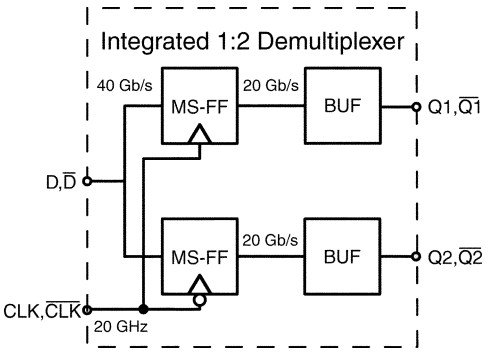


Fig. 12. Block diagram of the 1:2 DEMUX IC.

V. 1:2 DEMUX Circuit

The 1:2 DEMUX IC (Fig. 12) consists of two MS-FFs and output buffers (BUF). When a 40-Gb/s data stream is applied, the MS-FFs are clocked at 20 GHz. To sample every bit of the 40-Gb/s input data, the clock of one MS-FF is in phase while the other one is inverted. A separate buffer for each output decouples the MS-FFs from the 50-Ω environment.

The MS-FF (Fig. 13) consists of two latches connected in series. The latches are realized in the well proven CML design. As in the MUX, all transistors in the core are low-V_t 120-nm nMOS devices. The latches use series gating between clock and data inputs. All data path transistors are of the same size and are 3/5 the width of the clock transistors. Polysilicon resistors are used as loads. No inductive peaking is used because of the large number of latches and, therefore, large chip area needed for the inductors. Nevertheless, latches can make use of all advantages discussed in Section IV. One latch consumes 7 mA. The clock input is realized with 100-Ω on-chip resistors, which are connected to a dc level shifter ($V_{\rm DD}/2$).

To get the demultiplexed data off the chip, a line driver is used. It consists of a pair of differential amplifier stages. Fig. 14 shows the schematic diagram of the line driver.

In each stage, the tail current is three times the current of the previous stage. The first stage offers a high-voltage swing of

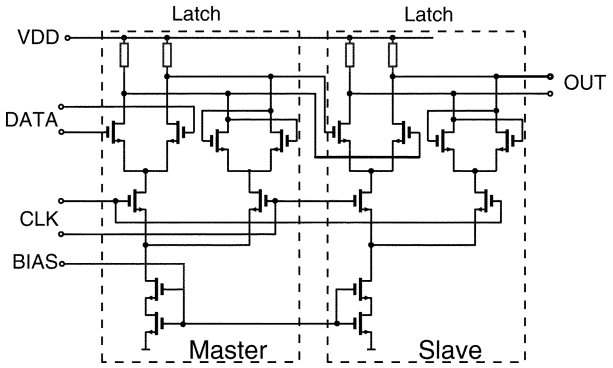


Fig. 13. Schematic diagram of the MS-FF.

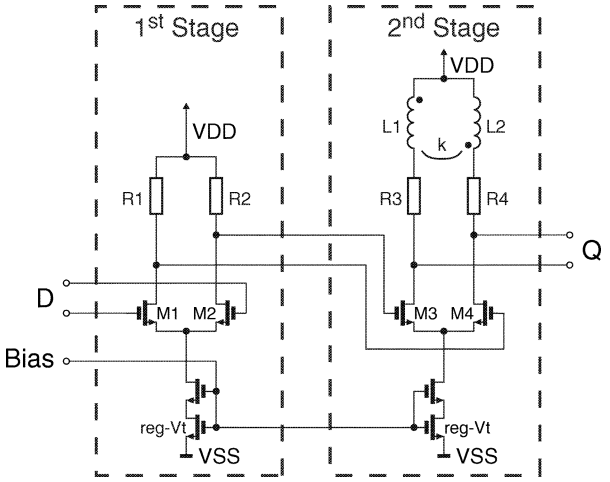


Fig. 14. Schematic diagram of the two-stage buffer used as line driver.

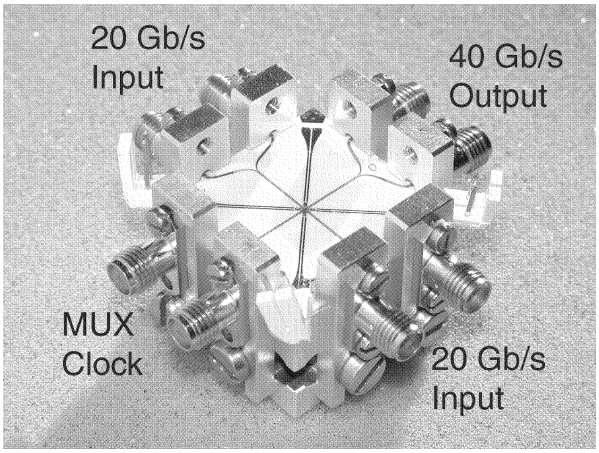


Fig. 15. 2:1 multiplexer high-frequency test fixture (30×30 mm^2).

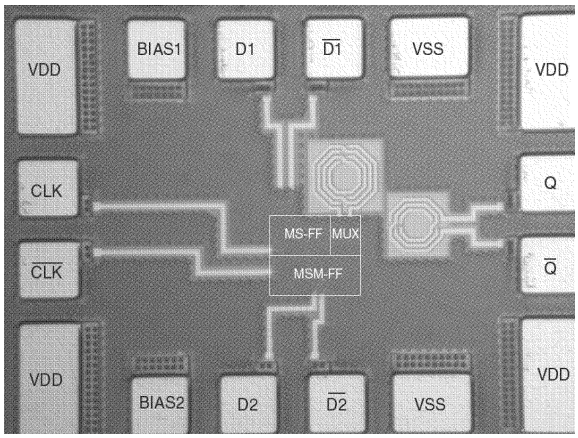


Fig. 16. Chip micrograph of the 2:1 MUX IC.

660 mV. This high-voltage swing drives the second stage, which works as a limiting amplifier. The last differential amplifier is designed to provide enough voltage swing with a 50-Ω load. To achieve full voltage swing, at least 10-GHz bandwidth is needed for the output buffers. To enhance the bandwidth of the output stage, shunt peaking is used. The advantages of shunt peaking are considered in Section III. The shunt peaking inductor is of the same kind used in the 2:1 MUX IC. A drawing of the inductor layout is shown in Fig. 5(a).

VI. Technology

The circuit is fabricated in a 120-nm CMOS technology with six-layer copper metallization and silicon-oxide dielectric ($\varepsilon_r = 3.9$). The chip has a size of 0.93×0.71 mm^2 and is determined by the pad frame. The active area is only a fraction of the total chip area. Due to fill structures, the chip micrograph shows only the topmost metal layer. The manufactured nMOS transistors have a cutoff frequency f_t of 100 GHz and a maximum oscillation frequency $f_{\max}$ of 50 GHz [6].

VII. Experimental Results

Fig. 15 shows the high-frequency test fixture of the 2:1 multiplexer IC. The 2:1 MUX IC is mounted on a 30×30 mm^2 microwave ceramic. We use SMA connectors and coupled microstrip lines on the substrate. The chip is bonded with a wetch-wetch bonder to the ceramic substrate. The chip is mounted in a cavity so that the surface of the chip is plane to the surface of the ceramic substrate. This allows very short bond wires, which increases the bandwidth of the MUX. The MUX has a chip size of 0.63×0.47 mm^2. Fig. 16 shows a chip micrograph of the MUX.

The multiplexer is tested with two pseudorandom bit sequences (PRBS of $2^7 - 1$). The input voltage swing is 2×400 mV$_{\rm pp}$. The sinusoidal clock signal has a voltage swing of 2×450 mV$_{\rm pp}$. Fig. 17 shows the measured eye diagram of the differential output signal at a data rate of 40 Gb/s. The measured eye opening is 2×100mV on an external 50-Ω load. The bounce at the top and the bottom of the eye shows that the circuit is at the limit and full current switching is not achieved. The transistor models are too optimistic at such high speeds. The 2:1 MUX draws 66 mA at 1.5-V supply voltage.

For measurements, the 1:2 DEMUX IC is mounted on a 30×30 mm^2 0.51-mm RO4003 microwave substrate with SMA connectors. The demultiplexer is tested with two PRBS, running at 20 Gb/s, which are then multiplexed by a SiGe 2:1 MUX [15] to get a 40-Gb/s data stream with sufficient voltage swing. The input signal voltage swing is 2×250 mV$_{\rm pp}$. The sinusoidal clock signal has a voltage swing of 2×450 mV$_{\rm pp}$.

The DEMUX has a chip size of 0.63×0.47 mm^2. Fig. 18 shows a chip micrograph of the DEMUX.

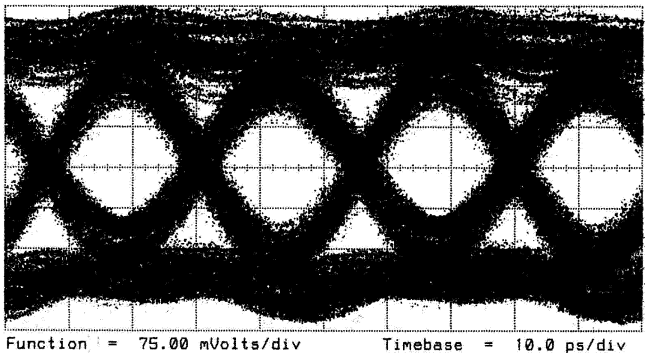


Fig. 17. Measured eye diagram of multiplexer output (40 Gb/s, differential signal).

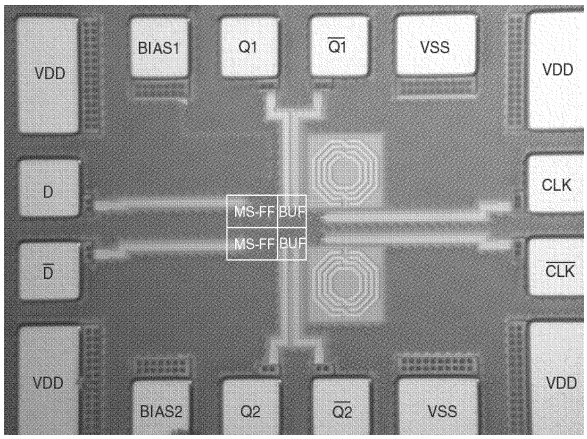


Fig. 18. Chip micrograph of the 1:2 DEMUX IC.

Fig. 19 (bottom) shows the measured eye diagram of the differential output Q1 at an input data rate of 40 Gb/s. The measured eye opening is 2×150 mV. The double traces in the eye are due to the limited bandwidth of the peaked output buffer. The peaking coils cause a rapid change in the group delay at the cutoff frequency, which results in intersymbol interference. Fig. 19 (top) shows the 40-Gb/s input eye diagram applied to the differential DEMUX input. The 1:2 DEMUX draws 72 mA at 1.5-V supply voltage. Table I summarizes the features of the chips.

VIII. Conclusion

CMOS has been demonstrated to be a viable technology for high-bit-rate broad-band circuit design at 10+ Gb/s. CMOS offers low production costs, high yield, and integration density.

A 40-Gb/s 2:1 MUX IC which fully exploits the high-speed potential of a 120-nm standard CMOS technology has been presented. The multiplexer is a fully differential design realized in CML. The MUX draws 66 mA from a 1.5-V supply and consumes 100 mW. To enhance the bandwidth, the 2:1 MUX IC uses inductive peaking extensively. The advantages of series peaking in combination with shunt peaking were demonstrated.

Inductive peaking can significantly increase the speed of the multiplexer. Simulations of the rise time show a speed increase of 26% compared with the nonpeaked multiplexer when shunt peaking is used. A speed enhancement of 31% can be achieved when shunt and series peaking is used.

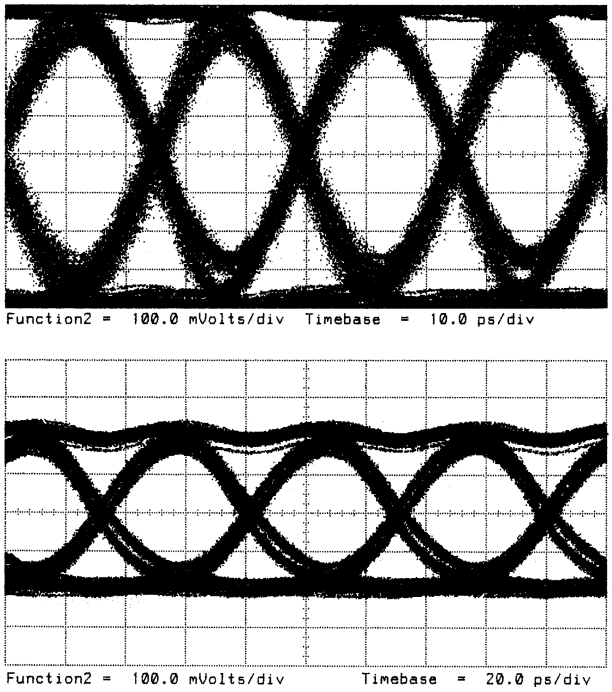


Fig. 19. Measured 40 Gb/s input eye diagram (top) and measured 20 Gb/s output eye diagram (bottom) of the DEMUX differential signal).

TABLE I
SUMMARY OF THE 2:1 MUX AND 1:2 DEMUX IC

Technology	0.13 μm CMOS, f_t=100 GHz
Chip size of each IC	0.63x0.47 mm^2
Supply voltage of ICs	1.5 V
Function	2:1 MUX
Max. output bit rate	40 Gb/s
Current consumption	66 mA
Power dissipation	100 mW
Function	1:2 DEMUX
Max. input bit rate	40 Gb/s
Current consumption	72 mA
Power dissipation	108 mW

Fully symmetric on-chip inductors with high Q factors were used as peaking coils. Precise extraction of the inductor parasitics is necessary to get reliable models for the circuit simulation.

A companion 40-Gb/s 1:2 DEMUX IC was presented. The data latch used in the DEMUX IC uses no inductive peaking and is realized in CML. Output buffers drive the demultiplexed data off the chip. The DEMUX draws 72 mA from a 1.5-V supply and consumes 108 mW.

REFERENCES

[1] H. Knapp, H. D. Wohlmuth, M. Wurzer, and M. Rest, "25 GHz static frequency divider and 25 Gb/s multiplexer in 0.12 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2002, pp. 302–303.

[2] M. Vadipour and J. Savoj, "A low-power 20-Gb/s 2:1 multiplexer/driver," in *Proc. Eur. Solid-State Circuit Conf.*, Firenze, Italy, Sept. 2002, pp. 231–234.

[3] A. Rylyakov, S. Rylov, H. Ainspan, and S. Gowda, "A 30 Gb/s 1:4 demultiplexer in 0.12 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 2003.

[4] M. M. Green, A. Momtaz, K. Vakilian, X. Wang, K. C. Jen, D. Chung, J. Cao, M. Caresosa, A. Hairapetian, I. Fujimori, and Y. Cai, "OC-192 transmitter in standard 0.18 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2002, pp. 248–249.

[5] J. Cao, A. Momtaz, K. Vakilian, M. M. Green, D. Chung, K. C. Jen, M. Caresosa, B. Tan, I. Fujimori, and A. Hairapetian, "OC-192 receiver in standard 0.18 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2002, pp. 250–251.

[6] T. Schiml, "A 0.13 μm CMOS platform with Cu/low-k interconnect for system on chip applications," in *Symp. VLSI Technology Dig. Tech. Papers*, 2001, pp. 101–102.

[7] H.-M. Rein and M. Möller, "Design considerations for very-high-speed Si-bipolar ICs operating up to 50 Gb/s," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1076–1090, Aug. 1996.

[8] T. H. Lee, H. W Li, and D. E. Boyce, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998.

[9] B. Razavi, "Prospects of CMOS technology for high-speed optical communication circuits," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1135–1145, Sept. 2002.

[10] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1368–1382, Sept. 2000.

[11] D. Kehrer, W. Simbürger, H. D. Wolmuth, and A. L. Scholtz, "Modeling of monolithic lumped planar transformers up to 20 GHz," in *Proc. IEEE Custom Integrated Circuits Conf.*, San Diego, CA, May 2001, pp. 401–404.

[12] *FastHenry user's guide, Version 3.0*, Massachusetts Inst. Technol., Cambridge, MA, 1996.

[13] *FastCap user's guide*, Massachusetts Inst. Technol., Cambridge, MA, 1992.

[14] G. C. Temes and J. W. LaPatra, *Circuit Synthesis and Design*. New York: McGraw-Hill, 1977.

[15] M. Möller, H.-M. Rein, A. Felder, and T. F. Meister, "60 Gbit/s time-division multiplexer in SiGe-bipolar technology with special regard to mounting and measuring technique," *Electron. Lett.*, vol. 33, no. 8, pp. 679–680, 1997.

Daniel Kehrer was born in Austria in 1976. He received the Dipl.-Ing. degree in communications engineering and the Ph.D. degree in electronics from Vienna University of Technology, Vienna, Austria, in 2001 and 2003, respectively.

He is currently with Infineon Technologies AG, Corporate Research, Munich, Germany, where his research focuses on gigabit CMOS circuit design.

Hans-Dieter Wohlmuth was born in Eisenstadt, Austria, in 1969. He received the Dipl.-Ing. degree in electrical engineering and the Ph.D. degree in electronics from the Technical University of Vienna, Vienna, Austria, in 1994 and 2000, respectively.

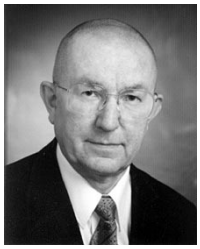
He joined Siemens AG, Corporate Research and Development, Munich, Germany, in 1994. He is now with Infineon Technologies AG, Corporate Research, Munich, where he has been engaged in the development of RF silicon integrated circuits for future wireless and wireline communication systems in the gigahertz range.

Herbert Knapp was born in Salzburg, Austria, in 1964. He received the Dipl. Ing. and Ph.D. degrees in electrical engineering from the Technical University Vienna, Vienna, Austria, in 1997 and 2000, respectively.

He joined Siemens AG, Corporate Research and Development, Munich, Germany, in 1993, where he was engaged in the design of integrated circuits for wireless communications. He is now with Infineon Technologies Corporate Research, Munich, Germany. His research interests include the design of high-speed analog and digital circuits.

Martin Wurzer was born in Innsbruck, Austria, in 1966. He received the Dipl. Ing. degree in electrical engineering from the Technical University of Vienna, Vienna, Austria, in 1994, where he is currently working toward the Ph.D. degree.

He joined Siemens AG, Corporate Research and Development, Munich, Germany, in 1994, where he has been engaged in the development of digital high-speed silicon bipolar ICs for future optical communication systems in the gigabit per second range. He is currently with Infineon Technologies Corporate Research, Munich, working on the design of integrated circuits for high-speed data communication.



Arpad L. Scholtz was born in Kecskemet, Hungary, on January 19, 1947. He studied telecommunications at the Technical University of Vienna, Vienna, Austria, where he earned the Master's degree in 1972 and the Ph.D. degree in 1976, both with distinction.

From 1972 to 1982, he was an Assistant Professor of radio frequency technology at the Institute of Communications and Radio Frequency Engineering, Vienna, where he became an Associate Professor in 1992.