A 40-μA/Channel Compensated 18-Channel Strain Gauge Measurement System for Stress Monitoring in Dental Implants

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***Abstract*—This paper presents an autonomous monitoring system ASIC, which is capable of measuring and compensating 18 strain gauges simultaneously. This sensor interface is implemented in a 0.7-μm CMOS technology and includes a proportional to absolute temperature (PTAT)-current reference, an 8-bit digital-to-analog converter together with a digital interface for multigauge nulling, a switched-capacitor (SC) instrumentation amplifier, an SC sample-and-hold (S/H), and a 9-bit successive approximation analog-to-digital converter. The total chip consumes a mere 40 μA/channel (at 3.1 V) and allows for sampling of each individual strain gauge channel at a sampling rate of 111 Hz with a 20-μstrain accuracy. The measurement system presented is a part of an autonomous data logger, which is integrated in a dental prosthesis.**

***Index Terms*—Dental prosthesis, low-power sensor interface, mixed analog–digital integrated circuit, strain gauge.**

I. Introduction

A DENTAL prosthesis (Fig. 1) is fixated by a bridge, which is supported by Titanium implants and cylindrical abutments ($h = 5.5$ mm, $\phi = 4.5$ mm). The number of implants and abutments can vary between two and six for a given patient. To reduce the number of implant losses and to gain more insight into the bone regrowth process (due to the introduction of Titanium implants into the bone), every abutment is equipped with three strain gauges. In this way, the axial forces and bending moments on the different abutments can be measured. Finite element analysis is applied to predict the bone regrowth process, using the measured axial forces and bending moments as input parameters.

II. Existing External System

At present, an external nonportable measuring unit is employed to quantify the forces on the abutments. This unit is connected to the different strain gauges by wires, which come out of the patient's mouth. The major drawback of this system is the restriction of the measurements to the hospital environment, since the external unit is necessary to perform the measurements. Another drawback is the possible introduction of artificial chewing behavior, since the wires to the strain gauges disturb the normal chewing behavior of a patient. Moreover, this measurement methodology does not allow measurement of unconscious nocturnal activities like bruxing and clenching, which are seen as a missing link for the validation of existing bone remodeling models. These drawbacks clearly indicate the need for a miniaturized measurement system which is part of the prosthesis and is capable of measuring continuously over a longer period, independent of the hospital environment.

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III. New Miniaturized System Specifications

The new system must be able to monitor 18 different strain gauge channels (six abutments) during a two-day period. Because the monitoring has to go on continuously, independent of the hospital environment, the system is equipped with two (1.55-V 45-mA·h) batteries (Panasonic SR41W), requiring a low-power design. The bandwidth of the dental force signals is 50 Hz and the desired measuring accuracy of the new system is 20 μstrain, which corresponds to an axial force accuracy of 19.4 N and a bending moment accuracy of 1.6 N·cm [1]. The maximum/minimum strains due to excessive biting are estimated to be $\pm$2000 μstrain. Since the tolerance on the nominal resistance of the strain gauges is as high as 1.5 times the resistance change due to maximum/minimum strains, compensation of every strain gauge channel is a requisite. Moreover, when the abutments and the prosthesis are placed orally, it was found that an excessive prestrain of up to $\pm$3300 μstrain can occur due to possible mechanical misalignments between the individual abutments and the bridging structure. This prestrain is thus also higher than the maximum/minimum occurring strains. This clearly shows that the new measurement system must be capable of compensating for this excessive prestrain *after* placement of the prosthesis, equipped with the data logger.

The prosthesis is fixated with screws through the abutments into the bone implants. It is made of a synthetic material, which has the advantages of low shrinkage during molding and subsequent hardening and a very low permeability for liquids. This allows one to mold the electronics, placed on a thick film substrate, in the prosthesis after treatment with an epoxy. The batteries are placed in a separate Teflon holder, which is sealed with a Teflon cover during molding and hardening of the synthetic prosthesis material. The batteries may not be in contact with the prosthesis material during hardening, since the high temperature needed for the polymerization of this material causes a capacity loss of the batteries. Teflon is utilized because of its high chemical inertness, such that no reaction with the synthetic prosthesis

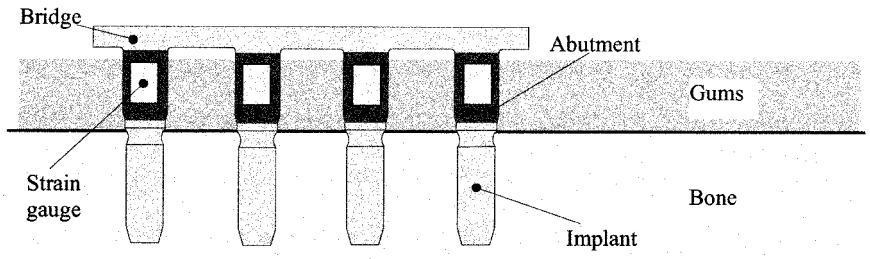

Fig. 1. Schematic of a dental prosthesis bridge, supported by abutments and implants.

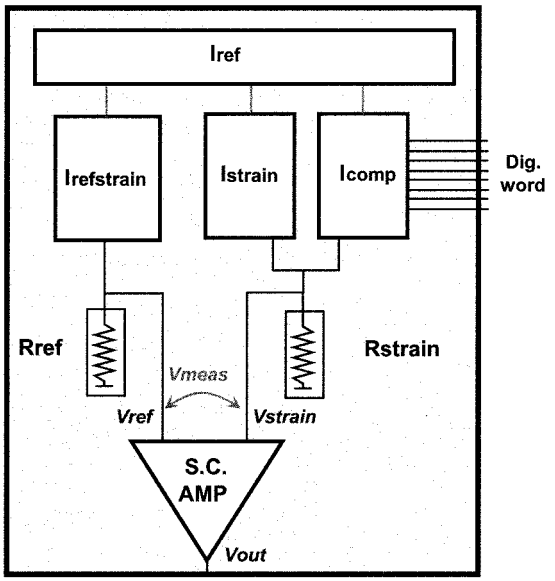

Fig. 2. Current-driven Wheatstone configuration with compensation.

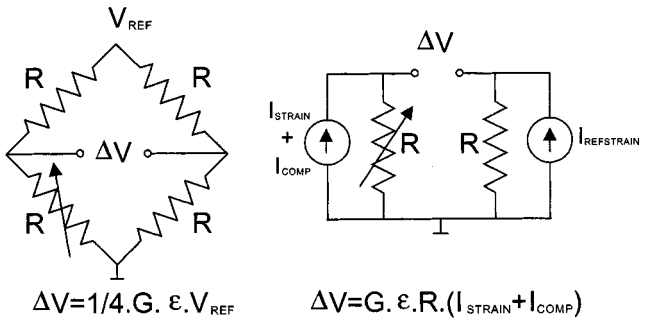

Fig. 3. Comparison of current-driven and voltage-driven Wheatstone configuration.

material occurs. After hardening, the two 1.55-V 45-mAh batteries are placed in the holder, which is sealed with a Teflon cover.

As explained below, a bidirectional link will be integrated in the complete data logger. This link permits activation of the above described compensation wirelessly after placement of the prosthesis and, in addition, it allows tailoring of the system toward each individual patient (e.g., number of channels, data processing algorithm). This is achieved by incorporating flexibility into the operation of the device during the design phase and the possibility of reprogramming the device settings by the telemetric link after oral placement.

IV. Multigauge Measurements With Nulling

To measure the different strain gauges, a current-driven Wheatstone configuration is applied (Fig. 2). This configuration consists of a reference resistor $R_{\rm ref}$, a strain gauge under measurement $R_{\rm strain}$ and two current sources $I_{\rm refstrain}$ and $I_{\rm strain} + I_{\rm comp}$. This current-driven configuration yields a doubled sensitivity-per-total-current ratio compared to the voltage-driven one[1] (Fig. 3) of

$$\Delta V/I_{\rm total} = 1/2.G.\varepsilon.R \tag{1}$$

[1]BLH, Catalog 305, Canton, MA, USA.

where

G gauge factor ($\Delta R/R = G.\varepsilon$);

ε applied strain;

R strain gauge resistance;

and yields thus a lower power consumption.

A system capable of compensating the earlier described occurring high prestrains and the strain gauges resistance tolerance is also shown in Fig. 2. $I_{\rm ref}$ is a mother reference current source from which the currents $I_{\rm refstrain}$, $I_{\rm strain}$, and a digitally controlled current $I_{\rm comp}$ are derived. This compensation current $I_{\rm comp}$ is summed together with the $R_{\rm strain}$-current $I_{\rm strain}$. By applying the appropriate digital word at the input of the digitally controlled current $I_{\rm comp}$, which is implemented as a binary weighted current steering digital-to-analog converter (DAC), the current through the strain gauge $R_{\rm strain}$ can be adjusted so that $V_{\rm strain}$ equals $V_{\rm ref}$ (limited by the resolution level of the DAC) and nulling (or compensation) is achieved.

The upper part of Fig. 4 illustrates the system expanded for 18 strain gauges. It shows the introduction of multiplexers to switch between the 18 different strain gauges. At startup, the appropriate nulling is performed for every single strain gauge. The digital word (i.e., input DAC) is put into an on-chip nulling memory. In the measurement mode, when a particular strain gauge is selected by the multiplexer, the digital word belonging to that particular strain gauge is fetched from the nulling memory and offered to the DAC such that offset-compensated measurements are performed. The overall sampling rate of the measurement system is 2 kHz, such that the channel sampling frequency of the individual strain gauge channels is 2 kHz/18 $=$ 111 Hz.

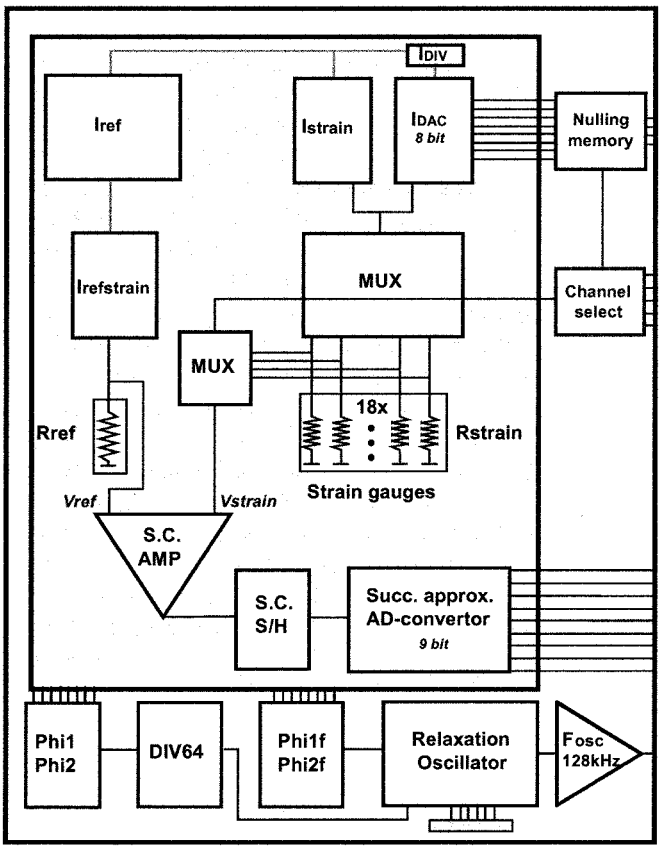

Fig. 4. Overview of the complete sensor interface chip.

V. New Sensor Interface Chip

A. System Overview

An overview of the total sensor interface chip, which was optimized with MAPLE for low-power consumption, is given in Fig. 4. It consists of the earlier described multigauge nulling block with an 8-bit DAC, followed by a switched-capacitor amplifier and sample-and-hold, proceeded by a 9-bit successive approximation analog-to-digital converter (ADC). It also has a 5-bit programmable 128-kHz relaxation oscillator on board to cope with possible technology variations and a digital interface and nulling registers to program/store the digital words needed for compensation. This chip has been implemented in a 0.7-μm CMOS technology.

B. Strain Gauge Sensors

To cope with possible temperature variations in the mouth (due to, for example, hot drinks or ice cream), self-temperature compensated (STC) strain gauges are employed. In this design, the BLH FSM-A6306S-500 [2] STC metal film strain gauge ($R = 5$ kΩ, $G = 2.1$) is chosen. This strain gauge is ideal for low-power battery-operated systems, because of its high nominal resistance and yet relatively small dimensions (3.8 mm $\times$ 2.5 mm). Moreover, system optimization proved that the introduced larger white noise due to the high-resistance strain gauges is not the limiting noise contribution to the total system.

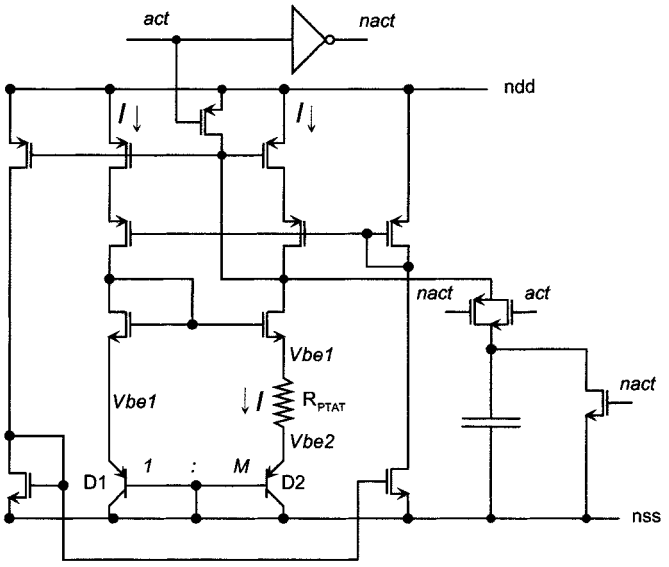

Fig. 5. Thermal voltage referenced current reference source with a wide-swing cascode current mirror and startup circuit.

C. Current Reference

The mother reference current $I_{\rm ref}$ is implemented as a self-biased thermal voltage referenced current source, shown in Fig. 5 [3]. The resistor $R_{\rm PTAT}$ is an externally screen-printed resistor that can be trimmed to attain an absolute mother reference current $I_{\rm ref}$ of 22 μA. $D1$ and $D2$ are vertical PNP bipolar transistors, available in the 0.7-μm CMOS process. The proportional to absolute temperature (PTAT) current I through $R_{\rm PTAT}$ equals

$$I = \Delta V_{be}/R_{\rm PTAT} = n.V_T.\ln(M)/R_{\rm PTAT} \qquad (2)$$

where

n emission coefficient;
V_T thermal voltage;
M ratio of vertical PNP bipolar transistors;

and this PTAT current has a temperature dependence given by

$$TC_I = \frac{1}{I}\frac{dI}{dT} = \frac{1}{V_T}\frac{\partial V_T}{\partial T} - \frac{1}{R_{\rm PTAT}}\frac{\partial R_{\rm PTAT}}{\partial T} \qquad (3)$$

which is minimized by using a Pt resistor paste [4] ($TCR = 2750 \pm 250$ ppm/°C) for the screen-printed resistor $R_{\rm PTAT}$, so that the two terms in (3) partially cancel each other. The wide-swing cascode current mirror is added to decrease the influence of power supply variations. In this way, the total inaccuracy due to power supply (between 2.7 and 3.3 V) and temperature variations (between 32 °C and 42 °C) is kept below 1.5%.

D. Binary Weighted Current Steering DAC

The DAC is a binary weighted current-steering DAC [5]. The required *range* of this DAC is imposed by the strain gauges resistance tolerance, the gauge factor tolerance, and the inaccuracy of the employed current mirrors that derive the different currents from $I_{\rm ref}$ (Fig. 4). To calculate the inaccuracy of these

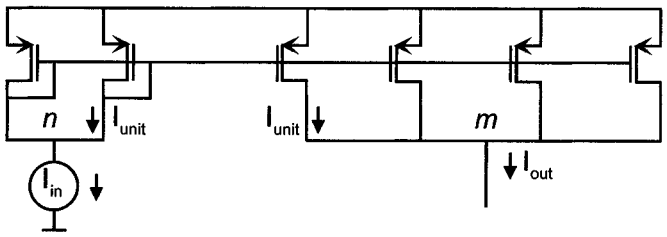

Fig. 6. Accuracy derivation of a current mirror with a m/n current ratio and a unit current source mismatch $\sigma(I_{\rm unit})/I_{\rm unit}$.

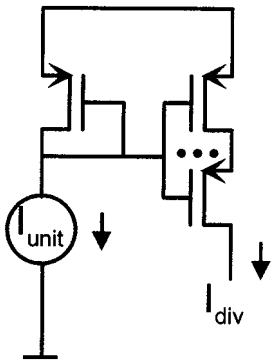

Fig. 7. Implementation of current divisions with series-connected transistors.

current mirrors due to mismatch, the following equation, which has been verified by Monte Carlo simulation, has been derived (Fig. 6):

$$(\sigma(I_{\rm out})/I_{\rm out})^2 = \left(\frac{1}{n}+\frac{1}{m}\right)\cdot(\sigma(I_{\rm unit})/I_{\rm unit})^2 + (\sigma(I_{\rm in})/I_{\rm in})^2. \quad (4)$$

Because of the discrete nulling by the DAC, a small "prestrain" remains after compensation. This remaining "prestrain" in combination with the maximum/minimum occurring strain must not saturate the following amplifier. The needed *resolution* and *accuracy* of the DAC are determined by the requirement that the remaining offset strain level after compensation must be smaller than 1/11 of the total measurement range of the system. This ensures that maximum compression (-2000 μstrain) and/or tension ($+2000$ μstrain) measurements, which occupy each about 5/11 of the total available measurement range, cannot cause saturation of the system. To achieve this, it was calculated that the needed resolution of the DAC is 8 bit (1 LSB $\approx$ 172 nA) and that the maximum step size between two consequent compensation levels of the DAC must always be smaller than 1.54 LSB. This requires thus a differential nonlinearity (DNL) of the DAC smaller than $+0.54$ LSB.

The binary weighted current steering DAC is implemented with unit current sources, equivalent with 8 LSB (i.e., 1375 nA). The 3-LSB current sources of the DAC are realized with series-connected (Fig. 7) unit current sources (to achieve current divisions), while the 4-MSB current sources are realized with parallel-connected unit current sources (Fig. 6). The total number of required transistors is strongly reduced in this way: only 45 transistors are needed instead of 255 (parallel-connected) with more or less the same area (due to the connections). On the other hand, the implemented current divisions are not completely perfect and introduce systematic errors in the DAC. However, these errors do not impact the functionality of the DAC as shown by simulation. Fig. 8 shows the simulated systematic DNL error due to the nonperfect current divisions. This error is smaller than $+0.1$ LSB, such that the total DNL error due to mismatch ($<\pm 0.2$ LSB) and the systematic errors ($<+0.1$ LSB) is smaller than $+0.54$ LSB over the total DAC range, satisfying the accuracy requirement.

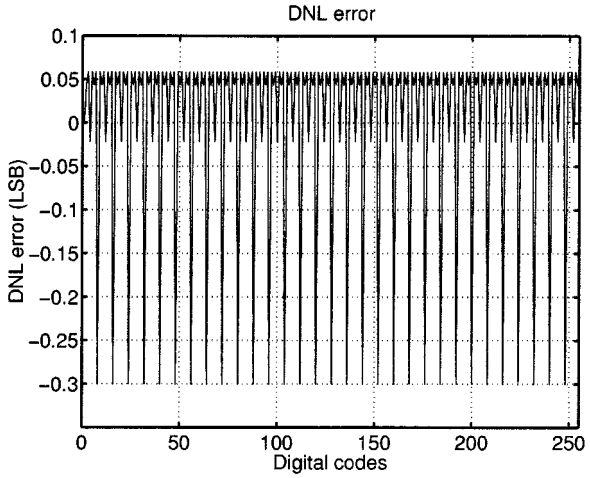

Fig. 8. Simulated systematic DNL error due to the nonperfect current divisions.

E. Resettable SC Gain Amplifier

Due to the small sensor signal levels, the temperature-dependent offset of the amplifier (in particular), and the drift of this offset become a problem. To cope with this, the amplifier and the other building blocks include offset-cancellation. The amplifier is an SC resettable gain amplifier (Fig. 9), where the offset is sampled during the reset phase ϕ_2, such that compensation for this offset is achieved during the (next) amplification phase ϕ_1 [6]. Also, (low-frequent) $1/f$ amplifier noise is cancelled in this way. The gain of the amplifier is 70 and the sample frequency $f_{\rm sample}$ equals 2 kHz, i.e., the 18 different channels are each individually sampled at 111 Hz.

To derive the total integrated input noise of the amplifier and the presented multigauge nulling block, the two different phases of the SC amplifier must be considered separately (Fig. 10) [7]. First the contributions of the different noise sources in the reset phase ϕ_2 to the different capacitances $V_{\rm noise1}$, $V_{\rm noise2}$, $V_{\rm noise3}$ and $V_{\rm noise4}$ are calculated by small-signal analysis. At the end of the reset phase, these noise contributions are sampled on the different capacitances and have to be taken into account during the next amplification phase ϕ_1. By applying the law of charge conservation, an equivalent noise source $V_{\rm noise\,sampled\,equiv}$. can be calculated that has to be added to the other noise sources during the second phase ϕ_1. This results in a total integrated input referred noise of 8.8 μV of the multigauge nulling block, the SC amplifier, and the following SC S/H.

To deal with the SC problem of charge injection, the clocks of the switches at the inputs of the amplifier (i.e., nMOS transistors) are advanced in time compared to the clocks of the

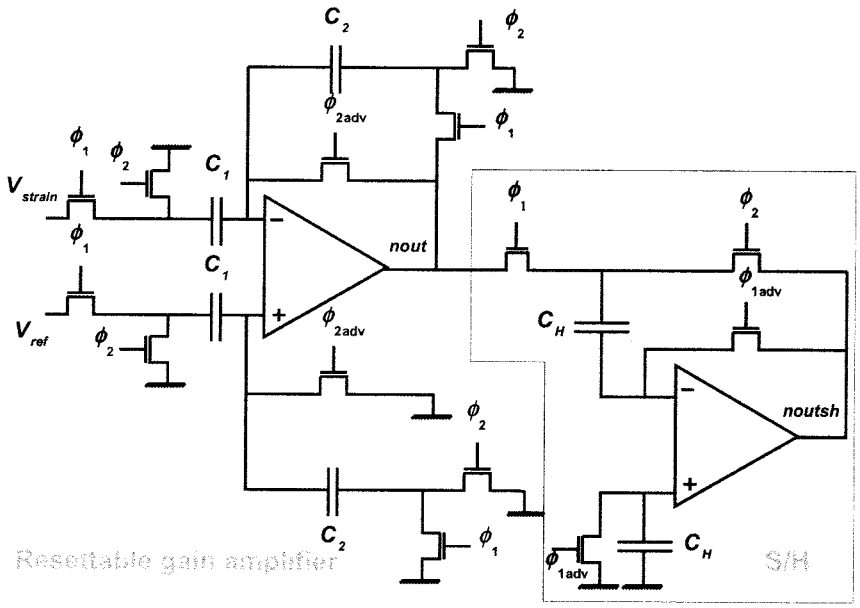

Fig. 9. SC resettable gain amplifier and S/H with offset-cancellation.

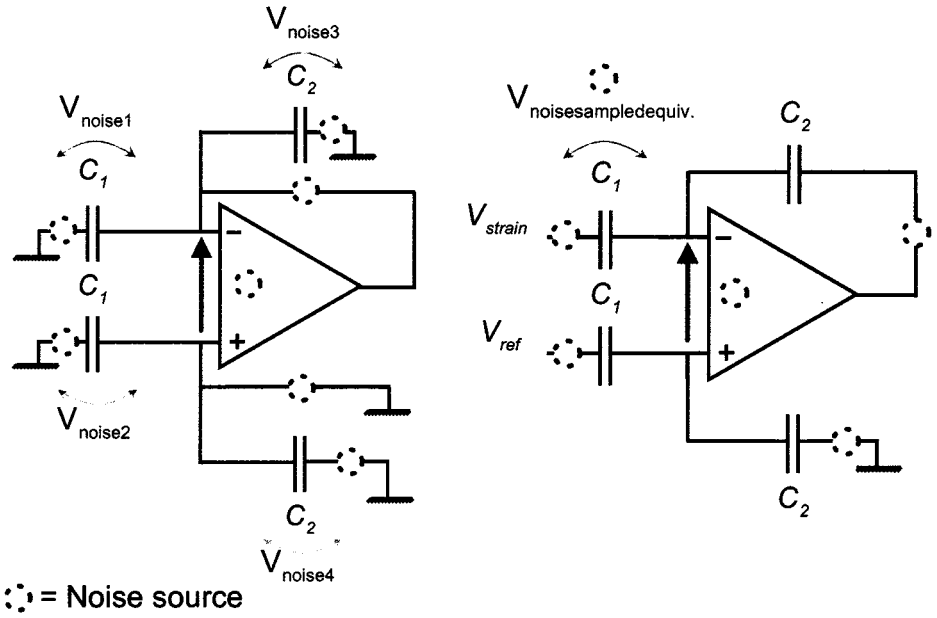

Fig. 10. Noise calculation of the SC resettable gain amplifier in the two phases. Left: reset phase. Right: amplification phase.

other switches (i.e., transmission gates) [6], such that the charge injection is constant for every cycle and independent of the input voltage V_{strain}. Moreover, extra switches and capacitors are placed at the positive input of the opamp (see also S/H). In this way, the impedances seen by the different switches equal each other and the injected charges will distribute equally on both sides. The resulting offset of the amplifier is strongly reduced in this way and only depends on capacitor and transistor mismatch [8].

F. S/H and Successive Approximation ADC

The amplifier is followed by an offset-cancelled SC S/H (Fig. 9) and a 9-bit successive approximation ADC based on a charge-redistribution DAC [9]. The pre-amplifier of the comparator [10] of this successive approximation ADC is also offset-cancelled. To reduce the power consumption of the ADC, the timeslots of the successive approximation sequence are not equally divided over the conversion period, i.e., $1/(2.f_{\text{sample}})$. The timeslots of the 3 MSB bits, where the largest voltage steps occur during the conversion, are made longer. In this way, a lower total power consumption over the whole conversion period can be obtained without causing a settling problem of the reference voltages during the first timeslots.

G. Layout

Fig. 11 shows a photograph of the 0.7-μm CMOS-sensor interface chip, which measures 4.6 mm by 5.2 mm. To minimize the interference of the digital part on the analog part, both are

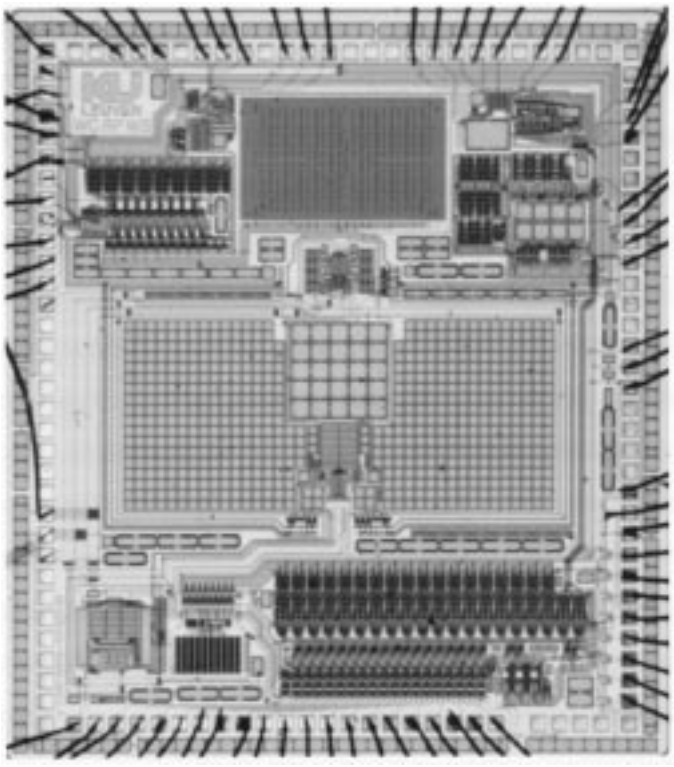

Fig. 11. Photograph of the total chip.

separated by grounded wells. The different power supplies of the various building blocks (analog, digital, and switches) are also decoupled separately (see outline of the chip). Moreover, the substrate of the chip is conductively glued to the negative power supply on the chip carrier to reduce possible noise injection of the digital circuitry into the analog parts through the low-resistance substrate of the technology.

VI. Experimental Results

A. Power Consumption

Table I shows the current consumption of the different analog building blocks. To reduce the total mean current consumption, the currents of the multigauge nulling block are turned off during most (=14/32) of the amplifier's reset phase ϕ_2. In this way, the resulting mean current consumption of the analog building blocks is reduced to a mere 38.3 μA ($\Rightarrow$119 μW at 3.1 V) per strain gauge channel.

The mean current consumption of the total chip, including the digital circuitry, is less than 40 μA per strain gauge channel, which is lower than that reported earlier in similar work [11]–[13]. Moreover, the presented system has the additional capability to compensate the different strain gauges and also has offset-cancellation of the different building blocks.

B. DAC

Fig. 12 depicts the measured DNL error of the implemented DAC. The systematic errors due to the current divisions are higher than simulated, resulting in a DNL error smaller than -1 LSB for certain digital codes. This, however, does not impose a problem to attain accurate nulling, since the DNL error

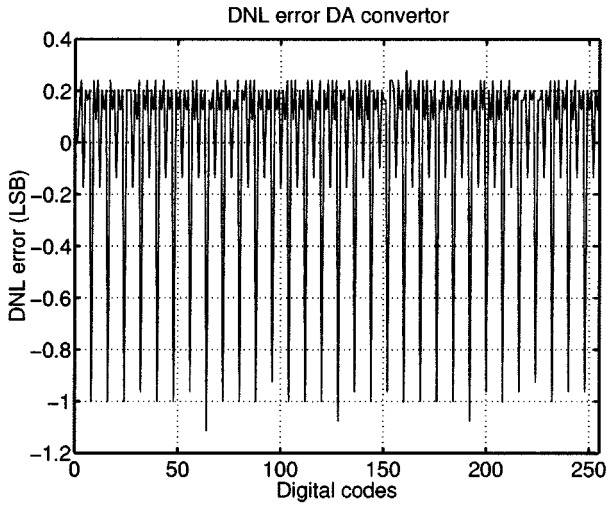

Fig. 12. Measured DNL error.

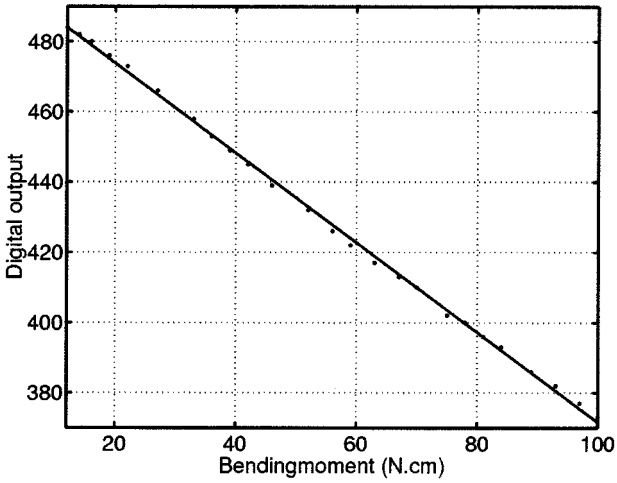

Fig. 13. Static load measurement with pneumatically controlled test setup.

is smaller than $+0.54$ LSB over the total range, satisfying the DAC accuracy requirement. The introduced nonmonotonicity for certain codes can cause a possible error in the digital successive approximation algorithm (applied in the full data logger) for automatic nulling, but this is easily solved by applying some extra "fine" nulling steps after "course" nulling by successive approximation.

C. Static Load Measurement

To determine the system's behavior to static loads, a calibration setup with a load cell has been developed. This pneumatically controlled test setup is able to impose axial forces and bending moments to an abutment under test. The applied force is measured with a load cell, having an accuracy better than ± 0.5 N. The digital output of the chip for an increasing bending moment (i.e., a force applied at 1 cm from the center of the abutment) is shown in Fig. 13. The slope of the least-squares fit of the measured data is 0.78 N·cm/bit. The σ of the error (due to the system's inaccuracy and the restricted test setup accuracy) is 1.43 N·cm, which proves that the system satisfies the requested accuracy specification of 1.6 N·cm (i.e., 20 μstrain).

TABLE I
CURRENT CONSUMPTION OF THE DIFFERENT ANALOG BUILDING BLOCKS

Analog building blocks	***Current (μA)***
I_{mother}	46
I_{ref} (18/32 of time)	176
I_{strain} (18/32 of time)	308
I_{DAC} (18/32 of time)	22
I_{DIV}	48
Current-driven Wheatstone with multi-gauge nulling (total)	*600*
S.C. Res. Gain Amplifier	103
S.C. Res. S/H	29
Successive Approximation ADC including voltage references	140
Relaxation oscillator (128 kHz) and clock generators (2 kHz and Φ_1,Φ_2)	39
Maximum current (18/32 of time)	*911*
Minimum current (14/32 of time)	*405*
Mean current	*690*
Mean current/channel (@ 3.1V supply voltage)	***38.3***

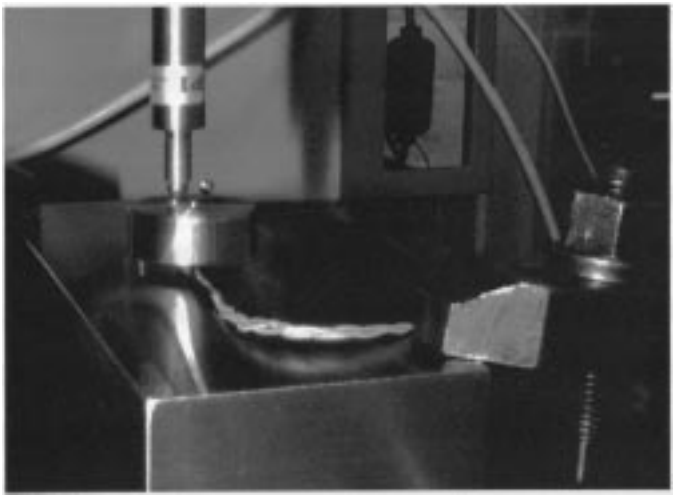

Fig. 14. Dynamic measurement setup with voltage-controlled piezo stack.

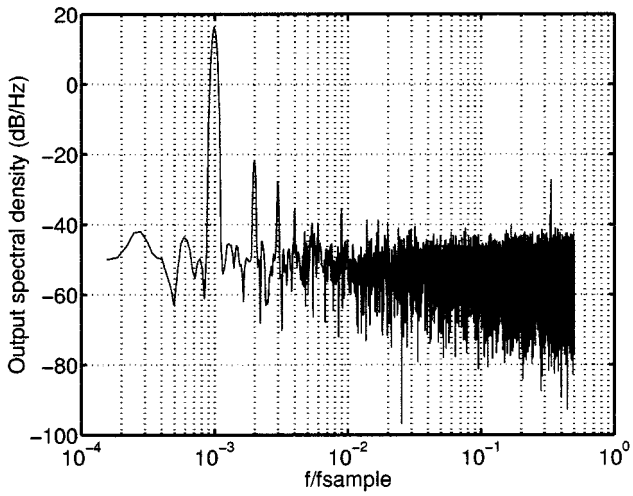

Fig. 15. Dynamic bending moment measurement with piezo stack (2 Hz, 32 N·cm peak-to-peak sinewave, SNDR = 27.7 dB).

D. Dynamic Load Measurement

Another test setup with a voltage-controlled piezo stack has been developed to perform dynamic measurements. Fig. 14 shows the piezo stack which can apply a displacement to a steel disc which is fixated to the abutment under test with a screw. It can apply a sinusoidal displacement with a maximum displacement of 60 μm. The maximum frequency of the sinusoidal displacement without the introduction of nonlinearities due to the test setup is limited due to the nonfixed connection of the piezo stack and the steel disc, i.e., approximately 20 Hz. Also, the maximum bending moment that can be imposed to the abutment is limited, because of the bending of the steel disc itself. However, despite these two drawbacks, this test setup permits to perform measurements with real abutments equipped with real strain gauges. In this way, measurements can be performed which are very similar to the actual measurements of the loads on the abutments of the dental prosthesis.

Because of the limited bending moment that can be applied with the described test setup, the total ADC range is split up in 19 overlapping intervals to perform dynamic measurements. The different intervals can be selected by changing the digital input of the DAC. For all the different intervals, the power spectral density of the digital output of the sensor interface chip for a 2-Hz sinusoidal input (32 N·cm peak-to-peak) bending moment

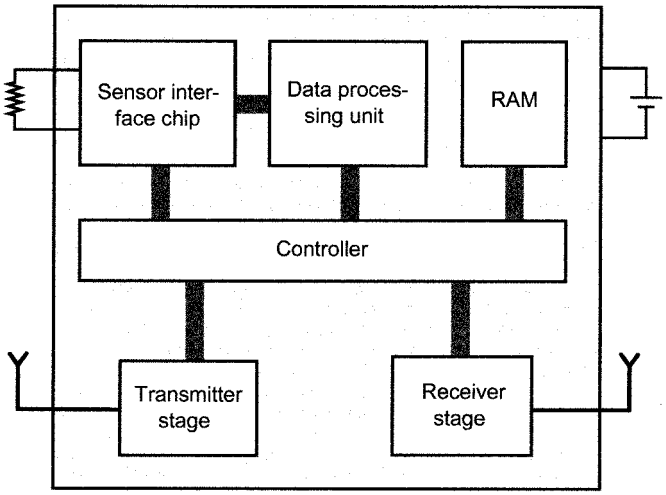

Fig. 16. Overview of the complete autonomous data logger.

was measured (Fig. 15) and the SNDR was derived to determine the dynamic performance. This yields a mean σ of the error over all the intervals of the system (together with the mechanical test setup) of 6.2 μstrain. The maximum measured σ of the error is 6.5 μstrain and the minimum 5.8 μstrain. These measurements prove a system accuracy better than 20 μstrain and prove that the ADC is not limiting the system performance, since the accuracy of the complete system is measured, including the multigauge nulling block, the SC amplifier, the SC S/H, and the ADC. An accuracy better than 20 μstrain was also measured with a sinusoidal voltage source at the input of the sensor interface over the total measurement range of the ADC, but the authors choose to present a measurement with a real abutment in this paper.

VII. Complete Data Logger

The presented sensor interface will be part of an autonomous data logger, shown in Fig. 16. This device consists of the described multichannel sensor interface, a bidirectional RF link, a 2-MB RAM, and a digital data processing unit and controller unit. The system's purpose is to continuously monitor the loads on dental implants over a 48 h-period and to store the processed data in the onboard RAM. The bidirectional RF link allows interaction with the outside world to program the operational mode of the device and to transmit the collected data after oral placement. The integration of all these different building blocks, except the RAM, into one chip is currently in progress.

VIII. Conclusion

We have realized and verified a sensor interface chip in a 0.7-μm CMOS technology, which is capable of measuring 18 different strain gauge channels simultaneously with a 20-μstrain accuracy. The total mean current consumption per channel is a mere 40 μA (@3.1 V) at a 111-Hz sampling frequency. The system is able to compensate the different strain gauge channels for offsets introduced by the strain gauges resistance tolerance and potential prestrains. Moreover, the different building blocks include offset-cancellation to cope with possible circuit offsets. The presented system will be implemented into an autonomous data logger, which will be integrated in a dental prosthesis.

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