

Systematic Analysis and Modeling of Integrated Inductors and Transformers in RF IC Design

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Abstract—An efficient modeling technique and a novel CAD tool for the accurate prediction of the performance of integrated inductors and transformers is presented. This generic and process-independent approach generates lumped-element models that easily plug into the RF IC design flow. Their accuracy is established through comparisons with measurements of numerous fabricated inductor structures. This paper intends to provide answers to vital questions in regard to existing limits and future expectations of the performance of on-chip inductors using comprehensive nomographs and quantitative analysis of spiral inductor families. A LNA design paradigm depicts how first-time-working silicon can be achieved when on-chip inductors' coupling is taken into account during the layout design process, minimizing risk, time, and cost.

Index Terms—Inductor modeling, integrated spiral inductors, integrated transformers, RF IC design.

I. INTRODUCTION

ON-CHIP inductors generally enhance the reliability and efficiency of silicon-integrated RF cells; they can offer circuit solutions with superior performance and contribute to a higher level of integration.

In low-noise amplifiers (LNA's), integrated inductors can be used to achieve input-impedance matching without deteriorating the noise performance of the cell [1]. They can also be used as loads intending either to improve the gain capability of the amplifier or to reduce its power consumption [2]. The usage of an on-chip transformer in an LNA circuit has also been reported [3]. In this case, the transformer is used to provide an inductive feedback path aiming to improve the linearity and stability of the circuit.

During the past few years, design efforts have been focused on integrating voltage-controlled oscillator (VCO) cells, including the passive LC tank, in a single chip while achieving low phase-noise performance ([4] and elsewhere). To ensure a very low phase-noise signal, the existence of a high-quality LC resonator for the VCO is demanded. The quality of the resonator circuit is dominated by the quality factor of the on-chip inductor; hence, the design of such passive devices remains of major importance.

The advent of SiGe technology has pushed the limits of wireless telecommunication applications that are implemented in integrated form beyond 2.5 GHz. In these cases, low-value high-precision inductances are demanded in order to meet the stringent circuit specifications. The existence of reliable integrated inductor models to be used in simulations is very crucial in such designs [2].

The industry has already appreciated the benefits of high-quality integrated inductors and is willing to adapt the existing processes in order to achieve improved inductive elements. The inclusion of Au or Cu metal layers, the increase of the thickness of metal alloys and dielectric materials, the decrease of the dielectric constant of the dielectric materials, and the increase of the substrate resistivity are among the changes that will help to accomplish quality-factor values of above 15. High- Q on-chip inductors can give the opportunity to implement reliable on-chip passive RF filters on silicon substrates, in the near future. Significant efforts have already been reported [30]–[49] in literature that aim to provide high- Q inductive structures for critical RF applications. All these results might lead to the replacement of some of today's off-chip components, while removing the burden of input/output impedance matching wherever this applies. Silicon-area optimization probably remains the last serious obstacle toward the extensive usage of integrated inductors in industrial applications.

First-time working silicon is the ultimate target in every IC design. This goal becomes more difficult to achieve as the frequency of operation increases. Moreover, the inclusion of a poorly characterized element as the integrated inductor in a design turns the whole process to an extremely risky matter. The aim of this work is to minimize the risk, the time, and cost of the inclusion of integrated inductor structures in silicon RF IC designs. This is achieved through the systematic presentation of the properties and nature of integrated inductors, as well as the numerous design cases, parametric evaluation, and nomographs that will allow the engineer to gain insight in Si inductors.

In this paper, a generic and process-independent model for simulating the performance of arbitrarily shaped and multi-layer inductors and transformers on silicon substrates is presented [5]. A multitude of inductor and transformer structures has been fabricated to support the research on the modeling of on-chip inductor structures. Based on the modeling technique that is proposed, a custom CAD tool has been developed, aiming to provide a comprehensive and complete guide for the analysis, synthesis, and optimization of all the popular integrated spiral structures that are commonly used in silicon-based RF IC's. Extensive measurement results of the numerous fabricated structures have proved the accuracy of the simulated models, as it will be

Manuscript received July 1999; revised March 2000. This work was supported in part by the Esprit Project 24123—OCMP. This paper was recommended by Associate Editor M. Ismail.

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Publisher Item Identifier S 1057-7130(00)06581-2.

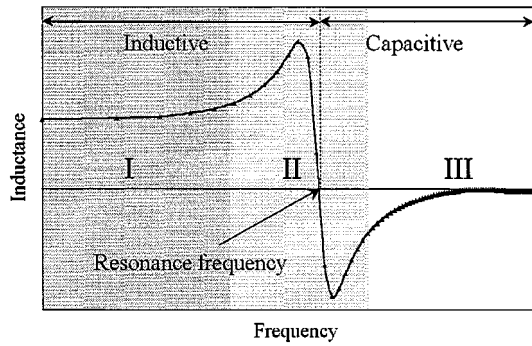


Fig. 1. Distinct operational regions of a typical integrated inductor over a low-resistive substrate in terms of its inductance.

presented later. The principal objective of this paper is to provide to the designer answers to vital questions, such as what to expect from contemporary and future silicon-based technologies regarding all the characteristics of spiral inductors. The proposed model succeeds in accurately predicting the performance of on-chip inductive elements in a wide frequency band that exceeds 10 GHz. Since the low resistivity of the substrate in silicon processes lowers the first self-resonance frequency of the integrated inductors, this area of operation cannot be overlooked any more. For the first time, the behavior of the integrated inductors in the vicinity of their self-resonance frequency and beyond is investigated.

To resolve the confusion that exists regarding the performance of typical integrated spiral inductors, a generic description will clarify their operating regions, before and after resonance frequency. Among the principal quantities that measure performance of an inductor is its inductance value (L). While an ideal inductive element exhibits a constant inductance value for all frequencies, every nonideal integrated inductor exhibits an inductance value that would resemble to the function of frequency depicted in Fig. 1. In terms of the inductance value, Fig. 1 displays qualitatively the three distinct regions of operation that most integrated inductors, over low-resistive silicon substrates, usually reveal. Region I in Fig. 1 comprises the useful band of operation of an integrated inductor. Inside this region, the inductance value remains relatively constant and the passive element can be securely used. Region II is the transition region in which inductance value becomes negative with a zero crossing, which is the first self-resonance frequency of the inductor. Beyond this critical frequency point, the passive element starts performing as a capacitor, and operation should be avoided. The inability to predict the limits of Region II and the exact resonance frequency has forced designers to be very reluctant with the usage of on-chip inductors. By applying the modeling method presented in this paper, resonance frequency can be accurately predicted and the spiral inductor can even be used as an LC -tank, eliminating the need of an area-spending integrated capacitor. In Region III, the integrated element exhibits capacitive behavior and, on top of all, a quality-factor value that is almost zero, making it practically useless.

Section II of the present paper describes in detail the proposed modeling technique of on-chip inductors and Section III gives a brief presentation of the developed CAD tool. In Section IV,

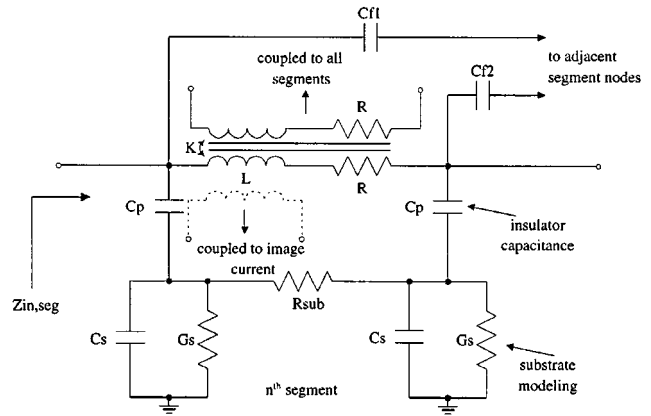


Fig. 2. Equivalent two-port for one segment of the spiral inductor.

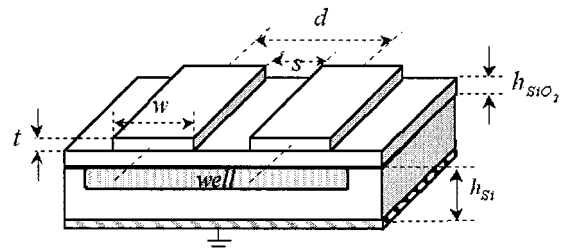


Fig. 3. Parallel coupled spiral segments over Si substrate.

the experimental results of a subset of the fabricated inductors and transformers are compared to simulated models, proving their accuracy, while Section V gives the design optimization hints and guidelines. Finally, it also presents a comprehensive paradigm of the design of a LNA used as a demonstrator of the precautions taken when implementing a multi-inductor layout design.

II. ANALYTICAL MODELING OF INTEGRATED INDUCTORS

A. Electrical Model

For accurate and fast modeling of integrated inductors, an electric-equivalent circuit compatible with SPICE-like simulators has been developed. Remarkable efforts have already been reported in literature toward the modeling of integrated inductors. Most of these have proposed lumped element models for simplicity and speed, such as those presented in [6]–[15]. In our approach, each segment of the inductor is modeled with a two-port network consisting of lumped elements, as shown in Fig. 2. Two coupled microstrips in a typical silicon process are drawn in Fig. 3. The geometry characteristics of interest are the track width w of the spiral, the distance between two adjacent parallel tracks s , and the height of the metal track t . The height of the Si substrate and the SiO₂ insulator are h_{Si} and h_{SiO_2} , respectively. The main elements of the two-port are the series inductance L , the resistance R of the segment, and the capacitors C_p formed by the insulating SiO₂ between the inductor and the Si substrate. All equations referred to hereinafter are listed in Table I. L is calculated by (1), while R is given by (2); R_{sh} is the sheet resistance of the metal track. All lengths are in centimeters, while inductance is given in nanohenrys. C_p is given by (3).

TABLE I
EQUATIONS OF THE PROPOSED GENERIC MODEL

	Equation	Reference
$L = 2l \{ \ln[2l / (w+t)] + 0.50049 + (w+t) / 3l \}$	(1)	[16]
$R = R_{sh} l / w$	(2)	
$C_p = \varepsilon_0 \varepsilon_r w / h$	(3)	
$M = 2IU$	(4)	[16]
$K_m = M_{1,2} / \sqrt{L_1 L_2}$	(5)	
$2M = (M_{l+m \pm \delta} + M_\delta) - (M_{l \pm \delta} + M_{m \pm \delta})$	(6)	[16]
$2M = (M_{m+p} + M_{m+q}) - (M_p + M_q)$	(7)	[16]
$M_{lm} = 2 \cos \phi \left[l \tanh^{-1} \left(\frac{m}{l+y} \right) + m \tanh^{-1} \left(\frac{l}{m+y} \right) \right]$	(8)	[16]
$M_{lm} = 2 \cos \phi \left[(M_{\mu+1, \nu+m} + M_{\mu\nu}) - (M_{\mu+1, \nu} + M_{\nu+m, \mu}) \right] - \Omega d_z / \sin \phi$	(9)	[16]
$\Omega = \frac{\pi}{2} + \tan^{-1} \left[\frac{d_z^2 \cos \phi + lm \sin^2 \phi}{d_z R_l \sin \phi} \right] - \tan^{-1} \left(\frac{d_z \cos \phi}{l \sin \phi} \right) - \tan^{-1} \left(\frac{d_z \cos \phi}{m \sin \phi} \right)$	(10)	[16]
$R_{sub} = \rho_{si} l / (wh_{si})$	(11)	
$C_s = \frac{(w + \Delta w')}{h} \varepsilon_0 \varepsilon_{r,si}, \Delta w' = \left(l + \frac{l}{\varepsilon_{r,si}} \right) \frac{\Delta w}{2}, \Delta w = \frac{t}{\pi} \ln \left[4e / \sqrt{\left(\frac{t}{h} \right)^2 + \left(\frac{l/\pi}{w/t + l.l} \right)^2} \right]$	(12)	[17]
$G_s = \hat{\sigma} \frac{w}{h}, \hat{\sigma} = \sigma \left(\frac{l}{2} + \frac{l}{2\sqrt{1+10h/w}} \right), \hat{h} = \frac{w}{2\pi} \log \left(\frac{8h}{w} + \frac{4w}{h} \right)$	(13)	[18]

The mutual inductance among the segments of the spiral plays an important role to the computation of the total inductance. The mutual inductance M between two segments of the inductor is modeled with a transformer. The complete circuit of the spiral inductor contains a transformer for every possible couple of segments. The magnetic coupling coefficient K of these transformers is given by (5), where L_1 and L_2 are the inductance values of the two segments that form the transformer.

In order to provide a generic model for all spiral geometries, the classical Grover approach [16] is extended to cover all possible relative position cases between two segments. Considering segments as simple filaments, the possible configurations in space are illustrated in Fig. 4. Two different cases are distinguished here: 1) the segments are parallel [Fig. 4(a) and (b)] and 2) the segments are at an angle of φ radians [Fig. 4(c)–(f)]. The mutual inductance of two parallel segments of equal length l , forming an orthogonal rectangle, is given by (4). All other configurations of parallel segments are based on this equation. Attention should be paid to the U factor in (4). U is calculated using closed-form expressions provided by Grover in [16], and concerns the various cases of the geometric mean distance (GMD) between two conductors of width w and height t , separated by d cm. If the segments are parallel, two distinct cases may appear. The first is shown in Fig. 4(a) and the mutual inductance is calculated by (6), where δ is positive for nonoverlapping segments and negative for overlapping ones. In the second [Fig. 4(b)], the mutual inductance M_{lm} between the two conductors with lengths l and m is calculated by (7).

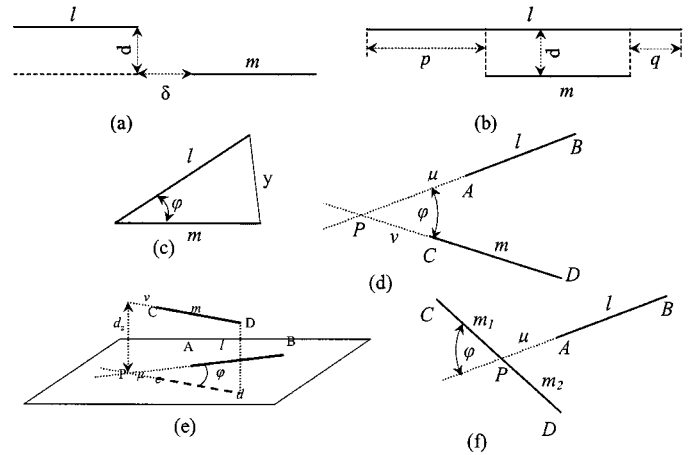


Fig. 4. Magnetically coupled segments in special configurations.

If the two segments are at an angle [Fig. 4(c)], their mutual inductance is calculated by (8). This general form is employed in the calculation of M in Fig. 4(d)–(f). In Fig. 4(d) the intersection point P is lying outside the two filaments and M is computed by (9). Ω applies only in the case of nonplanar segments [Fig. 4(e)] and is given by (10). The most complex case is the one depicted in Fig. 4(f), where the intersection point P lies upon one segment. This case is examined by partition as follows: segment CD is divided into CP and PD . Total M is calculated as the sum of M_1 and M_2 . M_1 is the mutual inductance of segments CP and AB , while M_2 is that of PD and AB . Both M_1 and M_2 are calculated as for Fig. 4(d). Mutual-inductance computation

between inductor segments and image currents on the ground plane under the semiconductor is also incorporated in a similar manner.

The coupling capacitances between parallel adjacent segments are calculated as proposed in [19], with closed-form expressions. The computation of the two elements modeling the substrate layers under the insulator is based on (12) for C_s , and on (13) for G_s . A comprehensive study presented in [18] addresses the calculation of the conductivity per unit length G_s and leads to (13), where σ is the conductivity of the substrate that behaves as a lossy semiconducting material. If a layer exists under the inductor, i.e., n-well in a CMOS process, it is modeled with an extra C'_s, G'_s branch computed also by (12) and (13), and connected in series with the C_s, G_s branch. Finally, the substrate resistance R_{sub} is computed by (11). The skin-effect formulation for both L and R employed in our algorithm is based on the closed-form expressions presented in [19].

B. Full 3-D Capacitance-Coupling Improvement

Multi-turn inductor structures sometimes exhibit more than one resonance frequency in the operating band of the device. To enhance the accuracy of the modeling method presented in the previous paragraph above the first resonance frequency, a technique that is analytically presented in [20] has been employed. According to this technique, an analytical model for calculating the full capacitance matrix of a system of multi-layer conductors is developed. The capacitance matrix contains capacitance values, not only for adjacent spiral inductor segments, but also for every possible pair of conductor segments that belong to all of the on-chip inductors. Inductor-model enhancements are more evident after the second resonance frequency of the device.

III. A NOVEL CAD TOOL FOR THE EVALUATION AND DESIGN OF INTEGRATED INDUCTORS

The **Spiral Inductor Simulation Program** [22] is a custom CAD tool developed to model planar and multi-layer inductive elements on silicon, based on the modeling technique given in the previous section. SISP, presented in detail in [5] and [21], is generic in terms of geometry and technology, efficiently gives fast answers within seconds to complex integrated inductor-modeling questions, and adds a new perspective to their use in Si-based RF IC's. Providing technology parameters and layout design through an ergonomic graphical-user interface, it can accurately model polygonal (i.e., square, octagonal) spiral inductors, both planar and 3-D, transformers, and center-tapped spirals, splitters, and baluns. In addition to the accurate prediction of inductance (L) and quality factor (Q), within a range of 2%, SISP can model the coupling among all on-chip inductive elements, solving the problem of the cell design with more than two spirals. The reliability of the algorithm has already been established through comparisons with experimental results in numerous silicon-based processes, from bipolar and BiCMOS to digital CMOS, as presented in the next paragraph. Finally, emphasis should be put on the prediction of the resonance fre-

TABLE II
TECHNOLOGIES AND TESTED STRUCTURES

Foundry	Technology	Structure
ST-Microelectronics	High-speed Bipolar	Square planar
		Octagonal planar
		Multi-layer Transformers
		Balun
		Splitter
SIEMENS	High-speed Bipolar	Square planar
ATMEL-ES2	Digital CMOS 0.5 μm	Digital planar
		Multi-layer
		Coupled inductors
AMS	BiCMOS 0.8 μm	Square planar
		Multi-layer
ALCATEL-MIETEC	Analog CMOS 0.5 μm	Square planar
		Multi-layer
IBM [23]	SiGe	Square planar
GEC-Marconi	GaAs	Square planar

quency of inductors which is one the very critical characteristics that SISP succeeds to model.

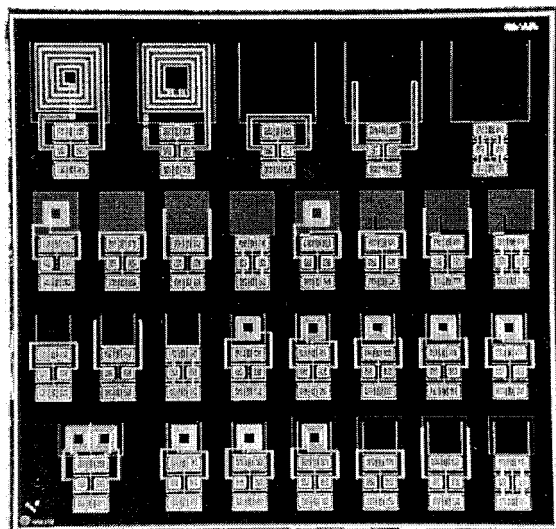
The layout editor of SISP can generate spiral inductor structures or, alternatively, export layout designs in CIF format. The designer should enter the CMOS, BiCMOS, or bipolar process parameters before creating a layout. A fast segment-by-segment extraction of the equivalent SPICE subcircuit is executed within seconds, while a similar model extraction with any EM software would take hours. The kernel extracts a two-port network consisting of eleven lumped elements for every segment of the on-chip inductors, as presented in Section II. Three distinct versions of the model are produced to accommodate "typical," "fast," and "slow" technology variations. Passive elements may be frequency dependent to incorporate the conductor skin-effect, if supported by the simulator being used. Simulations can be initiated through the user interface. The software displays simulation results in rectangular, polar, or Smith chart plots, against measurement results (from S -parameter sets), if any.

IV. ON-CHIP INDUCTOR PERFORMANCE

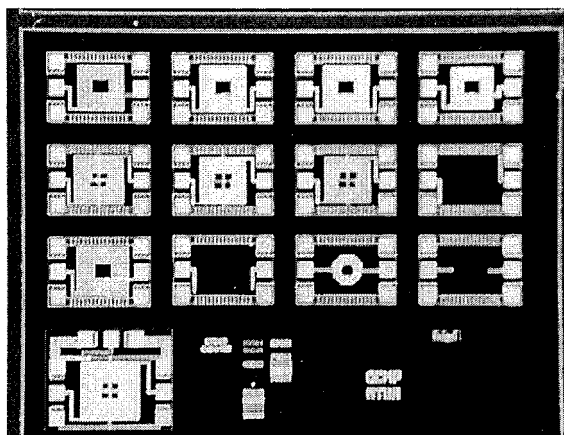
A. Simulation and Experimental Results: Processes and Structures

The reliability and accuracy of the proposed model and CAD tool has been extensively tested against measurements from fabricated integrated structures. A wide span of technologies and geometries is covered, as shown in Table II.

Numerous arrays of integrated inductors have been fabricated in different silicon processes. Two of them are displayed in Fig. 5(a) and (b). The first is an array of square planar and two-layer inductors with varying technology layer schemes fabricated in ATMEL-ES2's ECAT05 digital CMOS process. The second array contains 3-D inductors and transformers fabricated in STM's HSB2 high-speed bipolar process. The experimental results and their comparison with SISP simulations are presented in detail in the following paragraphs. For clarity, the presentation is categorized in standalone and multi-inductor elements.



(a)



(b)

Fig. 5. Micrographs of the test structures. (a) Array of planar and multi-layer square inductors in ATMEL-ES2's ECAT05 digital CMOS process. (b) Array of planar and 3-D, square, and octagonal inductors in STM's HSB2 high-speed bipolar process.

B. Measurement Setup

Measurements have been carried out with a probe station test bed that mainly consists of a HP8753D network analyzer and a Karl Suss probe station with Picoprobe's GSG pattern probetips. An open-circuit pad structure, identical to the one that the inductor is connected to, including all the metal paths that are needed to reach the spiral, is placed near the inductor under test. The measured Y -parameters of the open circuit are subtracted from those of the inductor structure in order to de-embed the parasitics inserted by the probes, in a certain degree.

C. Inductance and Quality-Factor Definitions

Inductance (L) and quality factor (Q), that are typically used to characterize the performance of inductors are given by (14) and (15), respectively

$$L = \text{Im}(1/Y_{11})/2\pi f \quad (14)$$

$$Q = \text{Im}(1/Y_{11})/\text{Re}(1/Y_{11}). \quad (15)$$

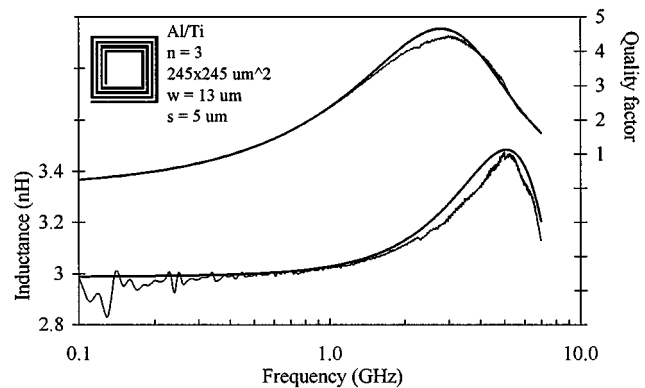


Fig. 6. Comparison between measured and modeled L and Q with SISP of a planar square spiral inductor fabricated in SIEMENS' B6HF.

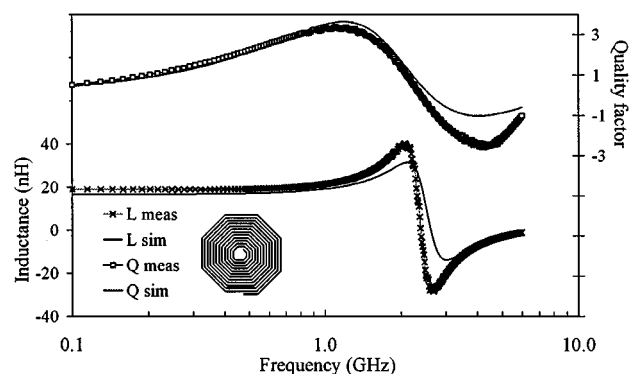


Fig. 7. Comparison between measured and modeled L and Q with SISP of a planar octagonal spiral inductor fabricated in STM's HSB.

Other definitions of the quality factor are provided in [24] and a more explicit study is presented in [25]. However, the classical definition of Q given by (15) is sufficient for the comparisons between measurement and simulation, as well as the performance analysis of the next section.

D. Stand-Alone Inductor Structures

This paragraph presents comparisons between measurement and simulation in terms of inductance (L) and quality factor (Q) as defined by (14) and (15). Four spiral inductor structures are analyzed: a planar square, planar octagonal, two-, and three-layer one. All figures contain both L and Q values comparing measurement and simulation of models extracted by SISP. Fig. 6 displays the results of a three-turn square spiral inductor of $245 \times 245 \mu\text{m}^2$ outer dimensions, track width of $13 \mu\text{m}$ and track spacing of $5 \mu\text{m}$. Fig. 7 displays the performance of a 12-turns octagonal spiral with diameter of $680 \mu\text{m}$, track width of $16 \mu\text{m}$ and track spacing of $8 \mu\text{m}$. Inductor performance prediction with SISP models is successful and accurate for both inductance and quality-factor values, as well as the critical resonance frequency. In particular, the relative error for both L and Q values is below 2% at the useful frequency band, which is far below resonance frequency, but it can reach 40% at frequencies where L and Q exhibit their maximum values. On the other hand, the relative error in the prediction of the first self-resonance frequency is usually below 5%. Multi-layer inductor structures consist of planar spiral inductors laid out

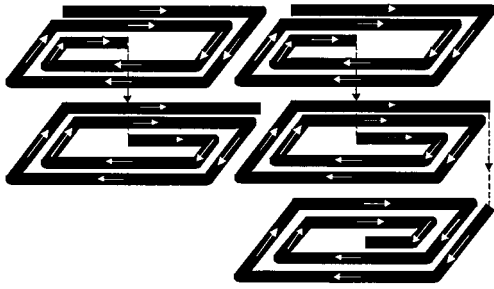


Fig. 8. Current flow in two- and three-layer spiral inductors.

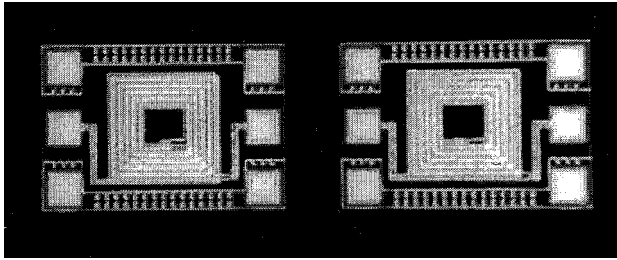


Fig. 9. Micrograph of two-layer spiral inductors.

on different metal layers in a multi-level interconnect technology, one overlapping the other. The relative current flow of the spirals is displayed in Fig. 8. The main benefit of this configuration is the considerable increase of the overall inductance value, sometimes by more than 600%! From another point of view, keeping the inductance value constant, there is an area reduction by the same high percentage, contributing to an overall area reduction for the whole RF IC.

Spiral inductor segments in different layers, which are close to each other, according to Fig. 8, have positive mutual inductance between them because current flows to the same direction. On the other hand, segments that have negative mutual-inductive coupling are relatively far. Therefore, this negative coupling does not affect the total inductance significantly. Overall, the positive mutual inductance between the two spirals is much higher than the negative one, resulting in the significant increase of the total inductance value of the multi-layer structure.

In Fig. 9, two kinds of two-layer inductors are displayed. Both inductors consist of two spirals: one on the first metal layer and one on the third. Both layers are of Al/Ti alloy. The geometrical characteristics of the inductor on the left are: area of $281 \times 281 \mu\text{m}^2$, track width and track spacing of $9 \mu\text{m}$. The spiral that is laid out on the third layer is slightly shifted diagonally and partially overlaps the spiral that is underneath. The characteristics of the inductor on the right are: area of $286 \times 286 \mu\text{m}^2$, track width of $14 \mu\text{m}$, and track spacing of $4 \mu\text{m}$. In this case, the top layer spiral exactly overlaps the lowest layer spiral. Although the total capacitance between the two layers is smaller for the inductor on the left, the fact that the track is narrower leads to a lower quality-factor value. On the opposite, the wider track of the inductor on the right introduces a higher Q value and approximately the same L value.

Fig. 10 displays the performance of the two-layer inductor on the right of Fig. 9 in terms of L and Q (measurement and simulation). Simulation results come from the distributed model extracted from SISF. The inductance of the single layer spiral

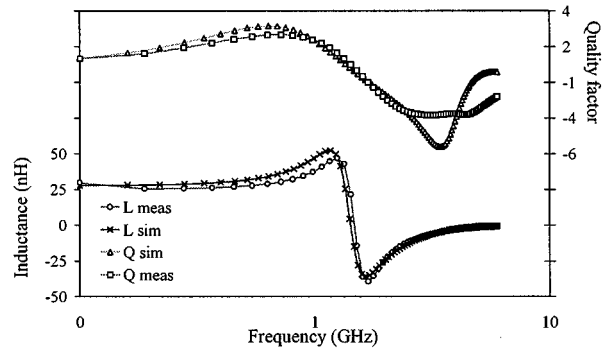


Fig. 10. L and Q of a two-layer, metal 3-1, five-turn spiral inductor—STM's HSB2 (area $286 \times 286 \mu\text{m}^2$, track width $14 \mu\text{m}$, and track spacing $4 \mu\text{m}$).

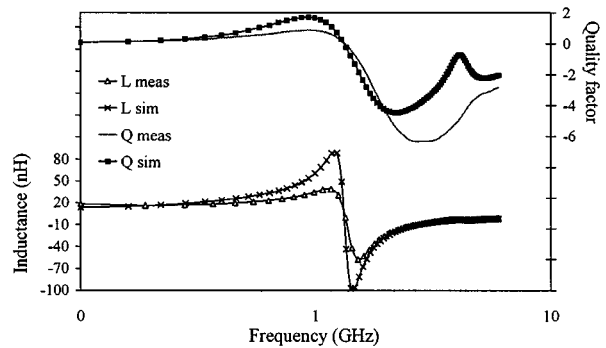


Fig. 11. L and Q of a three-layer, metal 3-2-1, four-turn spiral inductor—STM's HSB2 (area $250 \times 250 \mu\text{m}^2$, track width $14 \mu\text{m}$, and track spacing $4 \mu\text{m}$).

with the same geometrical characteristics would be around 7.5 nH, which means that there is an increase in the value of L that exceeds 300%!

As an extension of the concept of multi-layer inductor structures, a three-layer inductor has been fabricated and tested. Fig. 11 presents the performance (measurement and simulated SISF model) of such an inductor with the following geometrical characteristics: area of $250 \times 250 \mu\text{m}^2$, track width of $14 \mu\text{m}$, and track spacing of $4 \mu\text{m}$. A planar spiral inductor laid out on the third metal layer would exhibit no more than 6 nH of inductance. In this case, there is an increase of more than 600% or in other words, area savings of the same percentage.

Unfortunately, the elements presented above demonstrate very poor quality-factor. This is due to the fact that the first metal layer is very thin compared to the second metal layer, which could easily be used instead in such a structure. Two-layer inductor structures, consisting of spirals on the third and second metal layer, exhibit quality-factor values around $Q = 4.5$. Another important remark is that multi-layer inductors in general, exhibit very low resonance frequencies, a fact that is predicted accurately by SISF. Therefore, during circuit design, extreme attention should be paid to that frequency point where the inductor starts behaving as a capacitor.

E. Integrated Transformers and Coupled Inductor Structures

Despite being critical elements in many RF circuit topologies, integrated transformers have not yet been widely utilized in Si IC's. One of the main reasons that has prevented designers from using them is their inadequate modeling. Fig. 12 displays on the

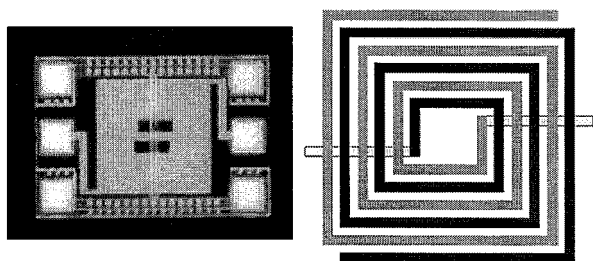


Fig. 12. Micrograph and layout representation of a transformer—primary and secondary in different shades—STM’s HSB2 (area $295 \times 295 \mu\text{m}^2$, five turns, track width $7 \mu\text{m}$, track spacing $15 \mu\text{m}$).

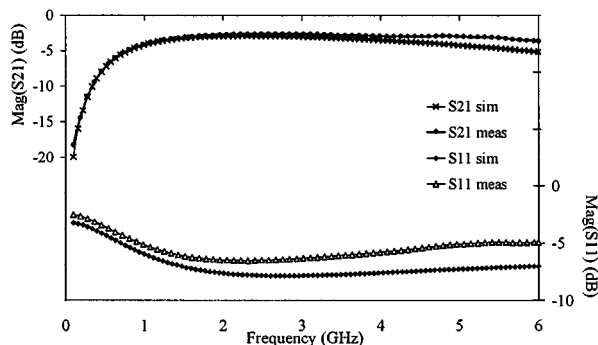


Fig. 13. Measurement versus simulation of the insertion and return losses of the planar transformer that is shown in Fig. 12.

left the micrograph of a planar transformer, and on the right a simple layout. Both the primary and the secondary coils of an integrated transformer can be laid out on the same or different metal layer.

The geometrical characteristics of the transformer displayed in Fig. 12 are: primary and secondary are five-turn spirals laid out on the third metal layer, with an area of $295 \times 295 \mu\text{m}^2$, a track width of $7 \mu\text{m}$, and a track spacing of $15 \mu\text{m}$. This transformer has been measured and modeled with SISP and the results for the insertion and return losses are presented in Fig. 13. In Fig. 25, the equivalent transform ratio n of the transformer is plotted and will be commented later.

Another issue of major importance in RF IC design is the electromagnetic crosstalk between neighboring on-chip inductors. Accurate modeling of the coupling among inductors ensures a first-time working silicon. Toward this target, Fig. 14 displays the test structure that has been fabricated to measure the coupling between two adjacent five-turn inductors ($250 \times 250 \mu\text{m}^2$). Measurement results along with simulation results from SISP models are presented in Fig. 15, exhibiting an accurate prediction of the isolation between the two inductors both for the magnitude and for the phase. The isolation beyond 1 GHz does not exceed 30 dB.

F. Dependence of Resonance Frequency on the Position of Substrate Ground Contacts

All of the fabricated inductors presented in Fig. 5(a) and (b) have very close to them a surrounding metal track filled with contacts to the silicon substrate. Research results have revealed certain dependence between the self-resonance frequency of the

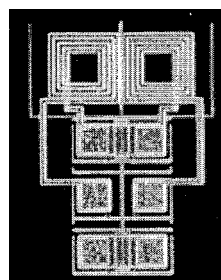


Fig. 14. Die micrograph of the test structure of adjacent spiral inductors.

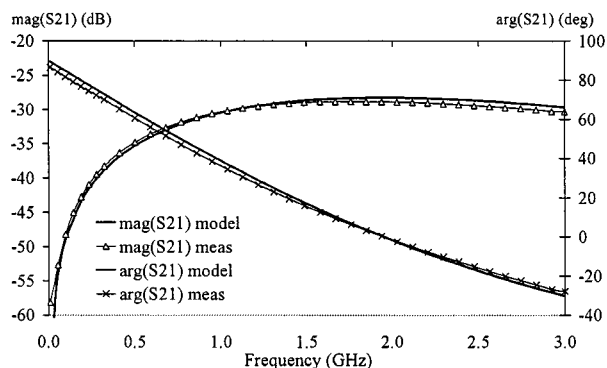


Fig. 15. Measurement versus simulation of the coupling between adjacent on-chip inductors— S_{21} of the structure shown in Fig. 14.

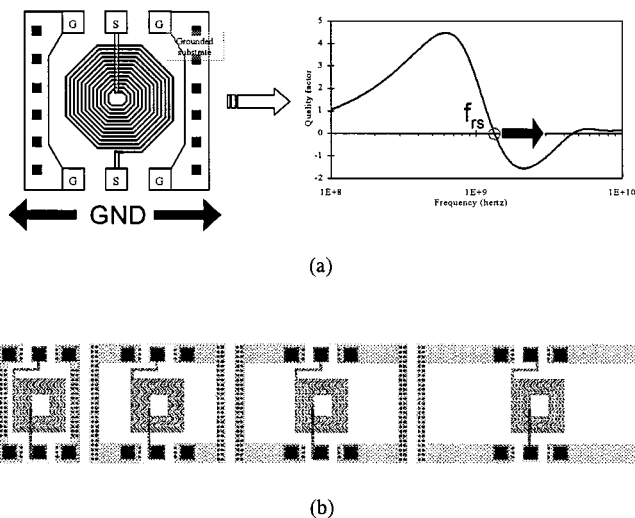


Fig. 16. (a) Substrate contacts placement and resonance-frequency relation. (b) Test-chip layout for the quantitative analysis of the phenomenon.

inductor and the distance between the ground pads and the spiral structure itself. As the ground pads are moved farther from the spiral inductor, the resonance frequency tends to increase. There is a certain distance from the inductor structure that this increase of the resonance frequency reaches a saturation value and does not increase anymore. The case described in this paragraph is presented graphically in Fig. 16(a). Fig. 16(b) displays the layout of four inductor structures designed to demonstrate the above effect. As the ground reference is moved farther from the inductor, the equivalent resistor that models the substrate behavior, R_s in Fig. 2, grows rapidly affecting seriously the resonance frequency f_{rs} . Thus, in order to avoid any undesirable performance variation of the inductor, extreme attention should be

paid to the position of all the substrate ground contacts that are placed near a spiral inductor for different reasons such as those contacts that are placed near MOS transistors to connect their body to a dc voltage. One safe rule of thumb is to keep close to inductive elements ground substrate contacts, as the ones shown in Fig. 16(a), to have the resonance frequency precisely defined and predicted by the proposed modeling technique.

V. DESIGN AND OPTIMIZATION OF ON-CHIP INDUCTIVE ELEMENTS: HINTS AND GUIDELINES

A. Stand-Alone Inductor Structures

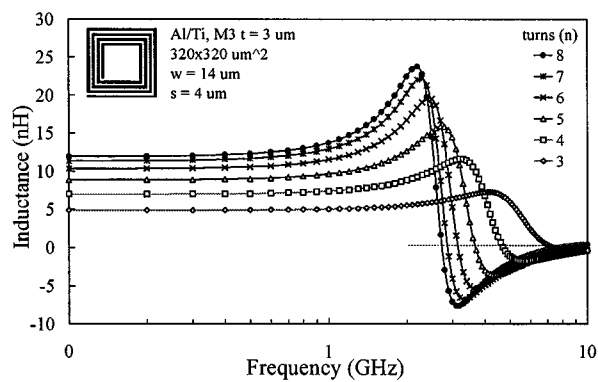
The following figures (Figs. 17–19) display the way in which the quality factor, inductance, and resonance frequency relate to essential technological parameters such as conductor thickness (t) and resistance (R_{sh}), insulator thickness (h_{ins}), and substrate resistivity (R_{sub}), as well as to geometrical parameters such as number of turns (n), spiral track width (w), and track spacing (s). The analysis consists of two parts: the first part [Figs. 17(a)–18(c)] depicts the relation of L and Q only to geometrical parameters, while the rest of the figures display the relation to technological parameters. The characteristics of the inductor family under test are clarified by insets. The information extracted from these graphs and summarized concisely in Table III, can be used to provide useful on-chip inductor design guidelines. For the RFIC designer, it is shown that trade-offs exist between the inductance value and the quality factor, when increasing the area, adding more spiral turns or reducing the track width (w). Fig. 17(a) and (b) display the inductance and quality-factor values related to frequency of a family of six square planar spiral inductors that have the same characteristics except the number of turns. As this number varies from $n = 3$ to $n = 8$, the inductance value increases and quality factor decreases, while resonance frequency decreases, too. The same type of case study for a family of two-layer structures is depicted in the next couple of figures, Fig. 17(c) and (d). Qualitative results for L and Q are similar. However, the inductance value of two-layer structures of the same footprint as their planar counterparts is more than 300% higher. Equivalently, the quality factor is reduced by more than 50%. The summary results of both cases are displayed in Fig. 17(e) for L and Fig. 17(f) for Q , comparing planar and two-layer structures. The next two figures [Fig. 17(g) and (h)] display Q as a function of frequency for both planar and two-layer square spirals when outer dimensions are varied, while all other characteristics are kept constant. Conclusions from this analysis are depicted in Fig. 18(a), (b), and (c), in which *low-frequency* L , Q_{max} , and f_{res} are given related to the total spiral footprint area. The conclusion drawn is that as the area occupied by the spiral inductor increases, the inductance value increases, while the value of Q and the resonance frequency decrease. In general, two-layer structures are preferred for their higher L values while their planar counterparts are preferred for their increased Q and higher resonance frequency. Therefore, in terms of Q losses and total area, the most economical way to increase the inductance is to employ extra inductor layers. With the aid of SISF, several novel structures can be introduced. Among these is the balanced-to-unbalanced (balun) transformer. A balun is constructed with a planar transformer

and a multi-turn spiral inductor laid out on a second layer as the primary coil. Typical amplitude and phase imbalances are displayed in Fig. 23. The geometrical characteristics are: primary is a seven-turn spiral, with an area of $250 \times 250 \mu\text{m}^2$, laid out on second metal layer, a track width of $8 \mu\text{m}$ and a spacing of $3 \mu\text{m}$; secondary comprises two four-turn spirals, in an area of $250 \times 250 \mu\text{m}^2$, laid out on third metal layer, with a track width of $7 \mu\text{m}$ and a spacing of $13 \mu\text{m}$. The performance of the simulated balun is satisfactory up to 3 GHz, where the amplitude imbalance does not exceed 0.1 dB and the phase imbalance deviates less than 1° from 180° .

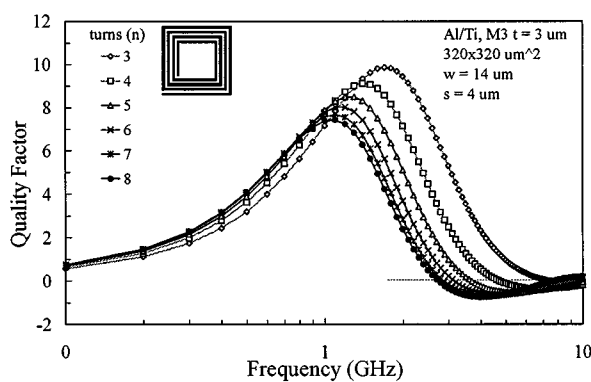
For the process engineer, significant benefits in inductor performance can be achieved by making metal lines and/or insulator layers thicker, by employing less resistive conductive materials, or by making the substrate more resistive. The benefits in terms of Q can be reaped by increasing the thickness t of the conductor, as exhibited in Fig. 18(d). Quality-factor relation to conductor thickness at three specific frequencies is displayed in Fig. 18(e), a comparison that has derived from the analysis of Fig. 18(d). Fig. 18(f) displays the decreasing relation of the low-frequency inductance value (L), with respect to maximum quality-factor (Q_{max}), at varying conductor thickness. This relation reveals that as the conductor thickness increase from $t = 0.8 \mu\text{m}$ to $t = 3.2 \mu\text{m}$, L changes within a range of 7%, while Q changes within a range of 50%! Similar qualitative conclusions can be drawn from Fig. 18(g) and (h), which prove how crucial the selection of the conductor material is to the maximum Q value of the inductor. Standard materials used for the metallization layers, such as Al/Ti alloy, Cu, and Au, are explicitly indicated. The dependence of the quality factor and the resonance frequency on the thickness of the insulator between the spiral inductor and the substrate is illustrated in Fig. 19(a) and (b). Remarkable is the fact that the variation of the insulating material affects not only the resonance frequency, but also the maximum quality-factor. Finally, substrate resistivity seriously affects resonance frequency and maximum Q values, as shown in Fig. 19(c) and (d). In the latter case, a minimum in Q_{max} with respect to substrate resistivity calls for careful process tuning. A generic trend that can be traced from Fig. 19(c) is that as the substrate resistivity increases the resonance frequency increases, too, making much safer the usage of spiral inductors in a wider frequency band.

The analysis presented in this section, apart from providing designers with an insight to the relations among geometrical and technological parameters of spiral inductors, aims to suggest a clear heading to process engineers in order to alter technology profiles and improve integrated inductors. For example, it is inferred that typical digital CMOS processes can hardly be used for pure analog RF cells when integrated inductors are employed, due to their low-resistive substrates. However, there are certain alterations that can be made to the substrate doping or to the top metal layer that will significantly refine the performance of on-chip inductive elements.

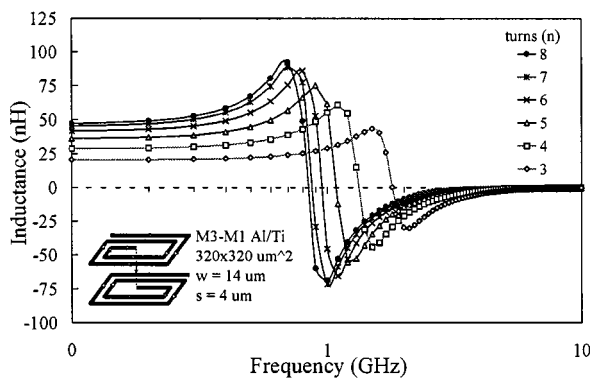
Serving the main objective of this paper, which is to give a thorough insight of the performance of integrated inductors, a family of square spiral inductors has been selected as a means to illustrate how the quality factor and the inductance of such structures depend on their outer dimensions and their



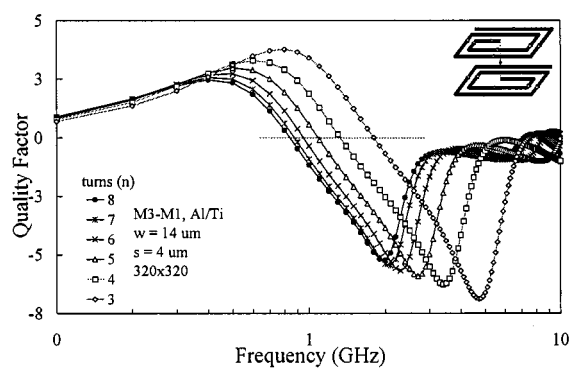
(a)



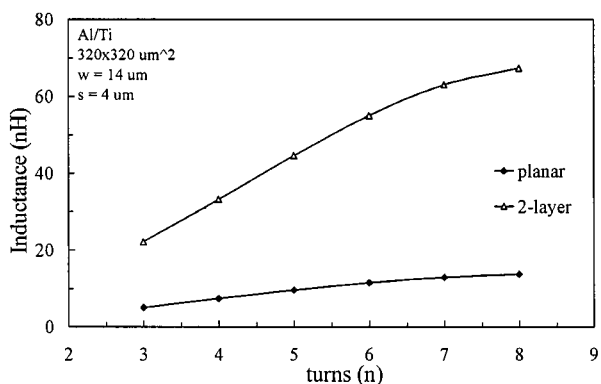
(b)



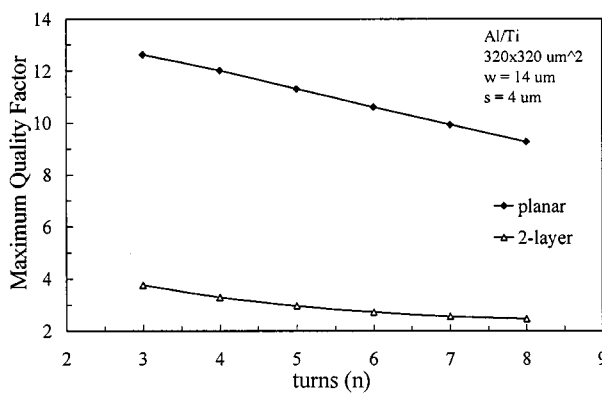
(c)



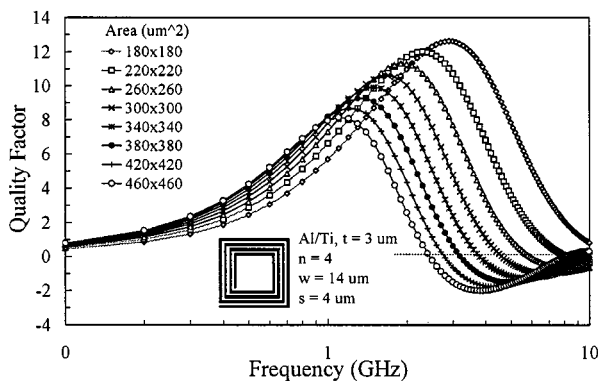
(d)



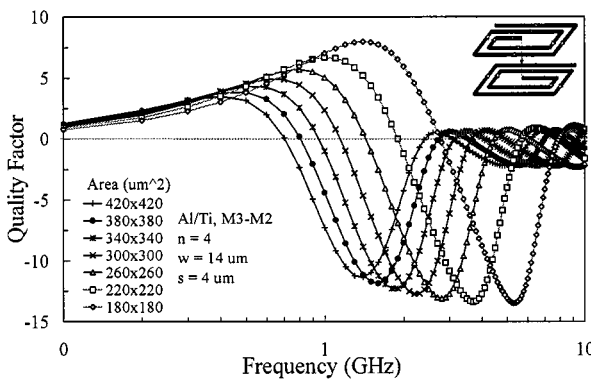
(e)



(f)



(g)



(h)

Fig. 17. (a) L versus frequency of planar inductors for varying number of turns. (b) Q versus frequency of planar inductors for varying number of turns. (c) L versus frequency of two-layer inductors for varying number of turns. (d) Q versus frequency of two-layer inductors for varying number of turns. (e) Comparison of L versus number of turns for planar and two-layer inductors. (f) Comparison of Q_{max} versus number of turns. (g) Q versus frequency of planar inductors for varying area. (h) Q versus frequency of two-layer inductors for varying area.

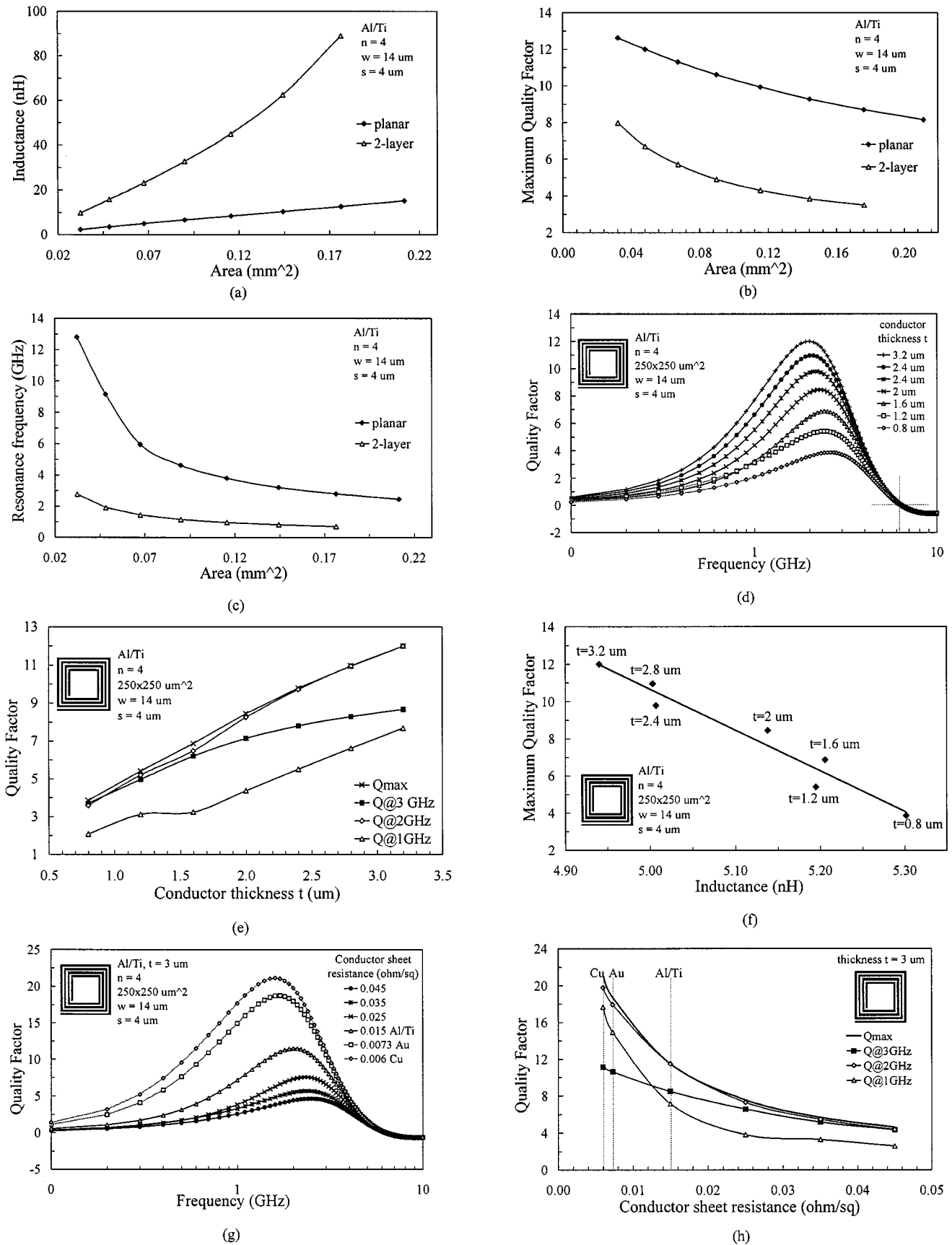


Fig. 18. (a) L versus area for planar and two-layer inductors. (b) Q_{max} versus area for planar and two-layer inductors. (c) Resonance frequency versus area for planar and two-layer inductors. (d) Q versus frequency for varying conductor thickness. (e) Q versus conductor thickness shown at three different frequencies. (f) Maximum Q versus L shown for varying conductor thickness. (g) Q versus frequency for varying conductor sheet resistance. (h) Q versus conductor sheet resistance shown at three different frequencies.

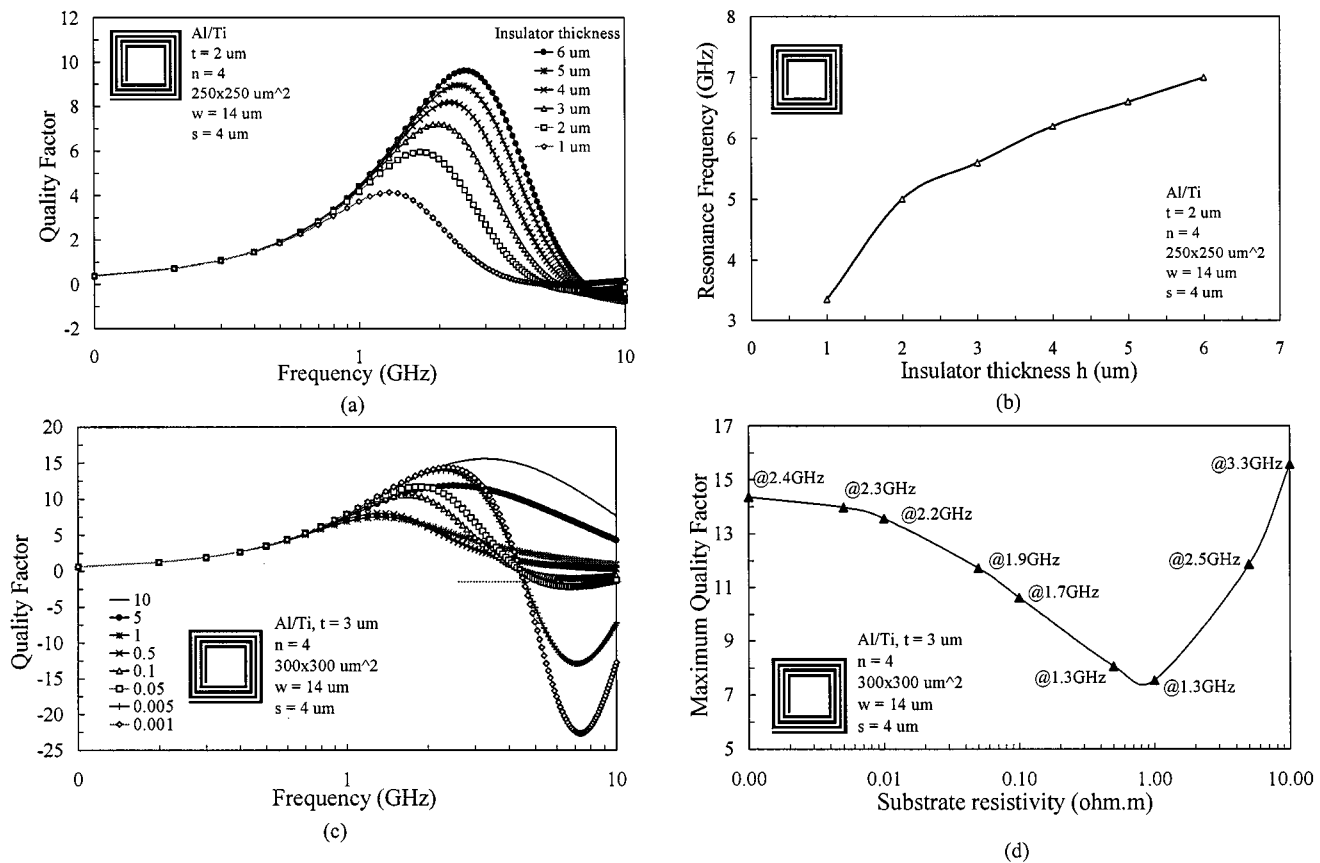


Fig. 19. (a) Q versus frequency for varying insulator material thickness. (b) Resonance frequency versus insulator thickness for square planar inductors. (c) Q versus frequency for varying substrate resistivity. (d) Q_{\max} versus substrate resistivity at various frequencies.

number of turns, examined simultaneously, in the form of comprehensive nomographs. Fig. 20 displays the dependence of the maximum quality-factor (Q) on the aforementioned geometrical characteristics, while Fig. 21 presents the dependence of the low-frequency inductance (L), as defined with Region I in Fig. 1. The combination of the two nomographs can be a valuable tool during the selection process of an appropriate spiral inductor that satisfies the silicon-area budget of the layout. A standard silicon process has been used for the modeling of the family of square spiral inductors. The values of some key technological parameters of this silicon process are shown in Table IV.

Generally, the maximum quality-factor value is more technology than geometry dependent, and hence, the absolute sheet resistance and thickness values highly affect the results of the respective nomograph. On the contrary, inductance values are more geometry dependent and hence the respective nomograph is valid for a wide range of IC technologies.

B. Integrated Transformers and Coupled Inductor Structures

The effect of physical separation on the electromagnetic crosstalk between neighboring inductors can now be predicted using the modeling techniques presented in this paper, a task that—in [26]—required fabrication and measurement.

Five pairs of identical spiral inductors have been simulated to examine how the isolation (S_{21}) between them varies as the distance between them changes. The results displayed in Fig. 22

TABLE III
INTEGRATED INDUCTOR PERFORMANCE TRENDS

	Q_{\max}	L	f_{res}
Conductor thickness (t)	↑ ⇒ ↗	—	—
Conductor sheet resistance (R_{sh})	↑ ⇒ ↘	—	—
Insulator thickness (h)	↑ ⇒ ↗	—	↗
Substrate resistivity (ρ)	↑ ⇒ ↘↗	—	↗
Area	↑ ⇒ ↘	↗	↘
Number of turns (n)	↑ ⇒ ↘	↗	↘
Track width (w)	↑ ⇒ ↗	↘	↘
Multi-layer inductor, extra layer	↑ ⇒ ↘	↗	↘

↗: increase, ↘: decrease, —: almost constant, ↘↗: exhibits minimum

prove that the isolation between two inductors that are $800\text{-}\mu\text{m}$ away (between their nearest sides) can be beyond 55 dB.

The essential need for transformers in RF circuit design leads to an investigation of the performance of integrated transformers in terms of insertion and return losses [28]. Three distinct cases of transformer families have been analyzed that illustrate the dependence of transformer losses on geometrical characteristics. Fig. 24(a) displays the insertion (S_{21}) and return (S_{11}) losses of planar transformers occupying an area of $350 \times 350 \mu\text{m}^2$, with a track width of $9 \mu\text{m}$ and a track spacing of $12 \mu\text{m}$. The number

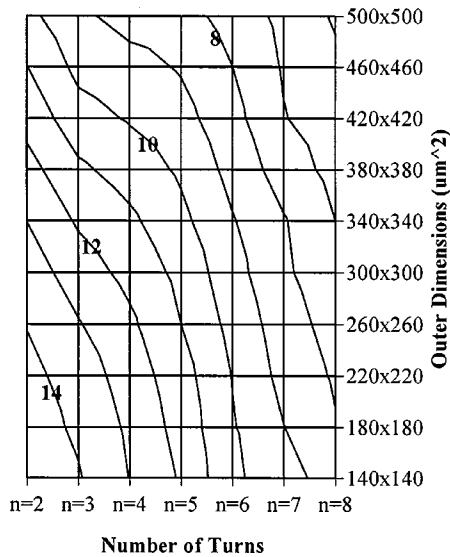


Fig. 20. Nomograph of quality-factor dependence on outer dimensions and number of turns of square spiral inductors.

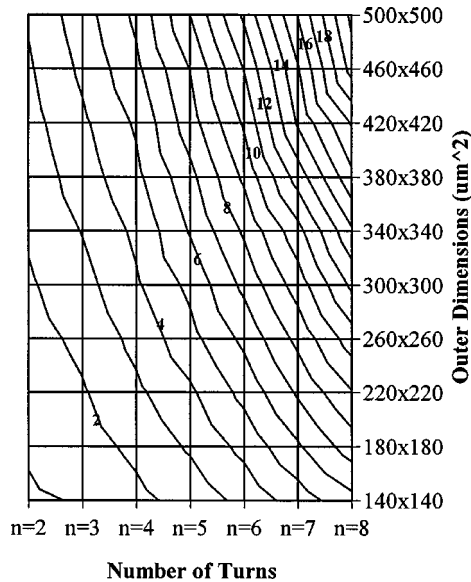


Fig. 21. Nomograph of inductance value dependence on outer dimensions and number of turns of square spiral inductors.

of turns varies from three to eight. As the number of turns increases, the insertion loss also increases at lower frequencies, while this is reversed at higher frequencies. In addition, the return loss is always greater for transformers with a higher number of turns.

In Fig. 24(b), both losses are examined for a family of transformers that have a constant number of turns, track width, and spacing but varying outer dimensions. As the transformer grows bigger ($400 \times 400 \mu\text{m}^2$), the return loss increases. Finally, in Fig. 24(c), the last family of transformers has constant outer dimensions, track spacing, and number of turns, but the track width varies from 9 to $15 \mu\text{m}$.

The transform ratio (n) of a transformer is defined as the ratio of the number of turns of the primary to that of the secondary coil. Although the number of turns of the two integrated spiral inductors that form the transformer are equal, the ratio

TABLE IV
TECHNOLOGY PARAMETERS USED FOR THE SIMULATION OF THE STRUCTURES UTILIZED IN THE NOMOGRAPHS OF FIGS. 20 AND 21

Technology parameter	Value
Metal 3 sheet resistance	0.017 Ohm/sq.
Metal 3 thickness	2.1 μm
Metal 3 to substrate area capacitance	0.008 fF/ μm^2
Metal 2 sheet resistance	0.036 Ohm/sq.
Metal 2 thickness	1.2 μm
Metal 2 to substrate area capacitance	0.015 fF/ μm^2
Si – substrate resistivity	0.05 Ohm . m
Si – substrate thickness	360 μm

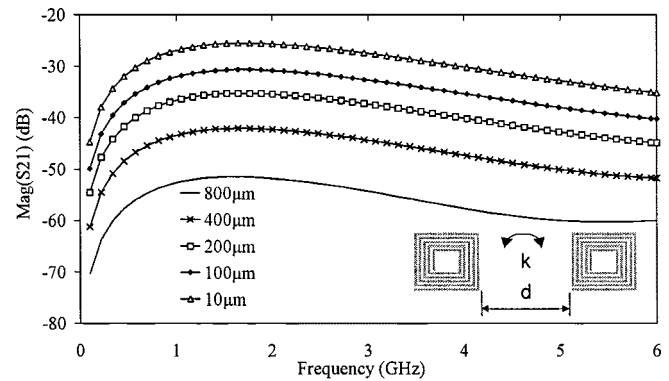


Fig. 22. Isolation versus frequency and distance (in μm) of two square spiral inductors.

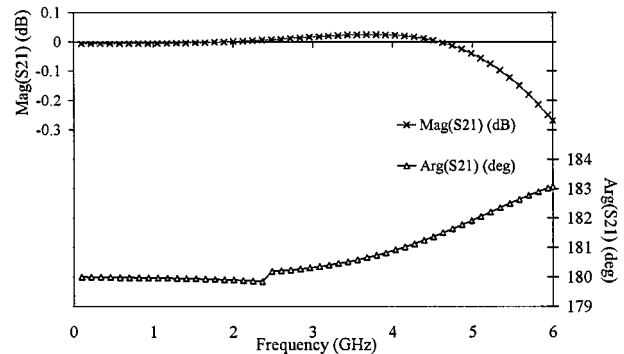


Fig. 23. Amplitude and phase imbalance of a two-layer balun.

n that is calculated from the Z parameters of the equivalent two-port is not unity. Instead, it is a complex quantity that is displayed in Fig. 25 for the transformer that was used as an example in Fig. 12. In general, ratio n rarely exhibits a magnitude higher than the value of 2, even if the ratio of turns is much higher than 2.

C. Circuit-Performance Dependence on Coupling Effects

The current trend in 1–2 GHz one-chip RF front-ends dictates the existence of more than one inductor on the same chip ([1], [3], [27]). In such a case, the magnetic coupling between individual inductors or in intended transformers can play an important role in the performance of the overall system. Therefore, the layout of the circuit drastically affects its electrical behavior.

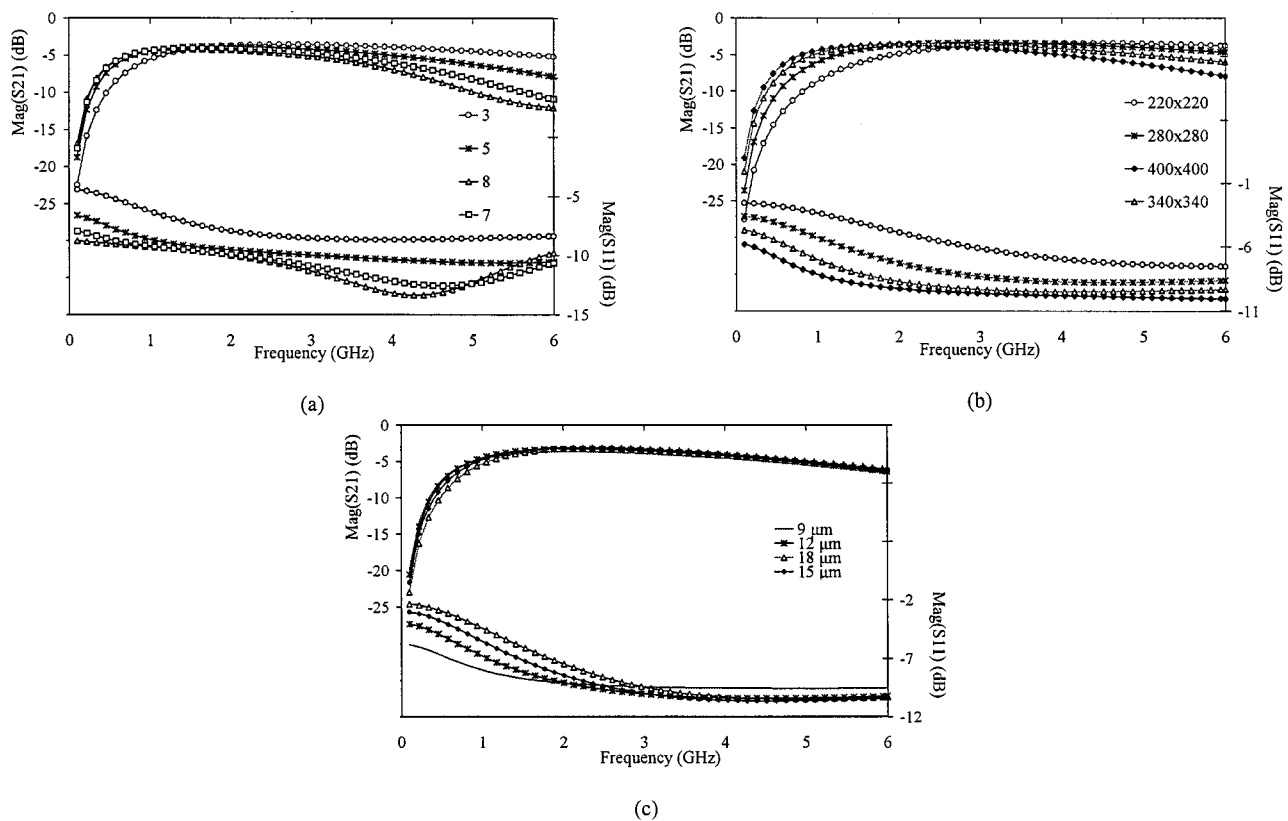


Fig. 24. Integrated transformers: simulation results of models extracted by SISF. (a) Insertion and return losses versus number of turns. (b) Insertion and return losses versus outer dimensions. (c) Insertion and return losses versus track width.

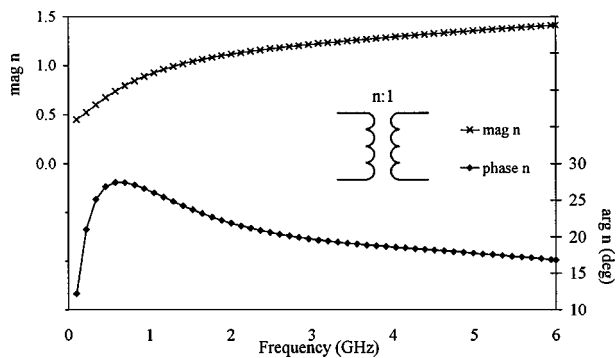


Fig. 25. Calculated equivalent transform ratio n for the transformer in Fig. 12.

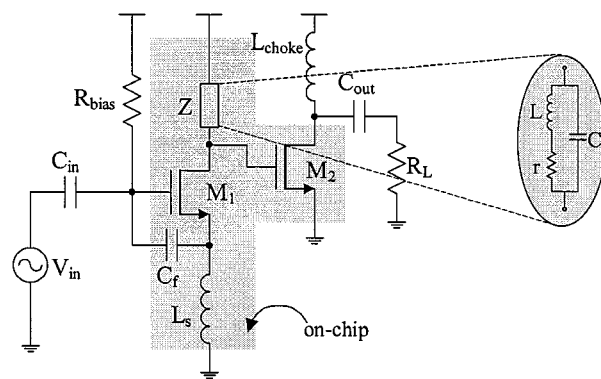


Fig. 26. LNA schematic and simplified model of the LC-tank Z .

The modeling technique presented in this paper is capable of predicting related phenomena, leading to reliable and effective simulations, and thus drastically reducing the design effort.

The design of a simple tuned low-noise amplifier is used as a vehicle to demonstrate the capabilities of the proposed modeling technique; however, it is by no means optimized in terms of noise, gain and silicon area. The LNA is designed in a digital submicron CMOS process and is operated around 1 GHz. The schematic diagram of the LNA is shown in Fig. 26, where the shaded area represents the on-chip components including load Z , that is the LC tank, and L_s , which is impedance matching inductor. The designer can select the inductors' geometry either by using nomographs or by simulation with SISF.

The magnetic coupling of the two integrated inductors of the LNA can seriously affect system performance and its im-

proper modeling can lead to a degraded frequency response. Input-impedance matching and S_{21} of the amplifier is also affected by the coupling of the two inductors. Fig. 27 depicts the LNA performance variance in terms of gain, under different inductor placement schemes, as predicted by SISF. In case A, the two inductors are laid out on the third metallization layer; in case B, L_s is laid out on the second layer and partly under the inductor of load Z . The diagonal placement of the devices provides the necessary magnetic isolation for the optimum operation of the amplifier, at the cost of increased area coverage. However, if the gain degradation is acceptable, case B can lead to a more compact layout.

To give a more illustrative example of how the performance of an inductor is affected by the presence of other inductors in

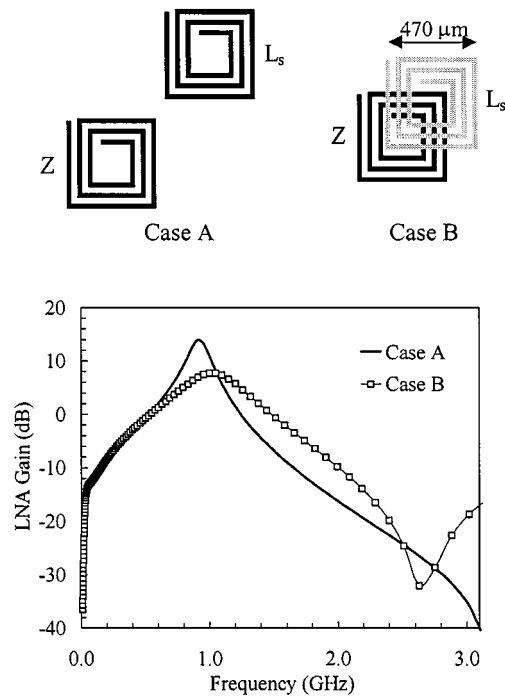


Fig. 27. LNA gain variance for two placement schemes of on-chip inductors.

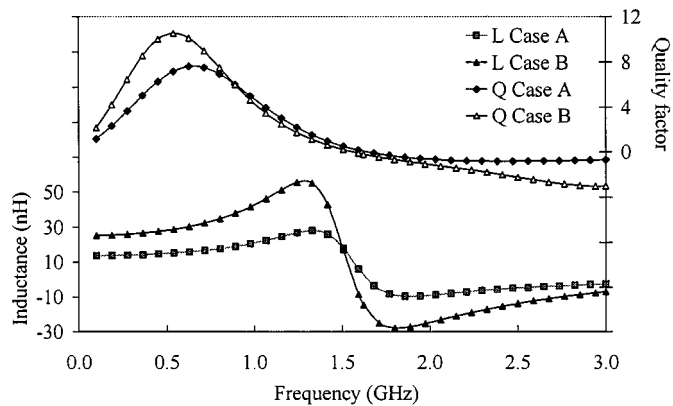


Fig. 28. L and Q of Z that is magnetically coupled to L_s .

its vicinity, Fig. 28 presents the L and Q values of the square inductor (Z) in the two distinct cases depicted in Fig. 27. Inductor L_s is driven with a separate current source that has the same phase as the source that drives Z . When L_s is too close to Z , its performance can be relatively changed, due to the magnetic coupling between the two, providing a very simple tuning tool. In other words, the L and Q values of an inductor can be tuned either by varying the magnitude and/or the phase of the current of a second inductor in its vicinity [29] or by changing their relative placement.

VI. CONCLUSION

An efficient modeling technique and a novel CAD tool for the accurate prediction of the performance of integrated inductors and transformers has been presented. This generic and process-independent approach generates lumped-element models that can easily plug into the RF IC design flow. Their accuracy has been established through comparisons with measurements of

numerous fabricated inductor structures. An analytical study of the performance of various cases of integrated inductors and transformers has been presented aiming to help designers and process engineers make the right decisions toward the optimization of these on-chip elements. Useful design guidelines are provided, to make the usage of spiral inductors less risky and more cost effective.

ACKNOWLEDGMENT

The authors would like to thank the following people that helped with the fabrication of the inductor structures: C. Alemani from STM, Catania, Italy, C. Dupuy from ATMEL-ES2, Rousset, France, J. Fenk from SIEMENS, Munich, Germany, and A. Sibrai from AMS, Graz, Austria.

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