A 7-GHz 1.8-dB NF CMOS Low-Noise Amplifier

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***Abstract*—A 7-GHz low-noise amplifier (LNA) was designed and fabricated using 0.25-μm CMOS technology. A cascode configuration with a dual-gate MOSFET and shielded pads were adopted to improve the gain and the noise performance. The effects of the dual-gate MOSFET and the shielded pads are discussed quantitatively. An associated gain of 8.9 dB, a minimum noise figure of 1.8 dB, and an input-referred third-order intercept point of +8.4 dBm were obtained at 7 GHz. The LNA consumes 6.9 mA from a 2.0-V supply voltage. These measured results indicate the feasibility of a CMOS LNA employing these techniques for low-noise and high-linearity applications at over 5 GHz.**

***Index Terms*—Dual-gate MOSFET, intercept point, low-noise amplifier, noise figure, shielded pad, Si substitute.**

I. Introduction

RECENTLY, wireless communication systems with a carrier frequency of over 5 GHz, such as intelligent transport system (ITS) and wireless LAN specified by IEEE 802.11a, have attracted considerable attention. Furthermore, a carrier frequency of up to 10 GHz is expected to be used for fourth-generation (4G) wireless systems.

Thanks to recent advances in CMOS technology, a transition frequency f_T is competitive with that of silicon bipolar junction transistor (Si-BJT) technology. The main noise sources of MOSFETs at high frequency are the thermal noise of channel and gate resistance. The gate resistance is reduced using low-resistance salicided gate material and a multifinger gate structure to obtain low noise performance [1], [2], and so the dominant noise source of MOSFETs is the thermal noise of a channel. On the other hand, the main noise sources of Si-BJTs are thermal noise of base resistance and shot noise of the collector current. To reduce base resistance, a large geometry device is needed, but this requires more collector current to keep the same high f_T value, which causes more shot noise. To reduce shot noise, a small collector current is needed, but this requires a small geometry device to keep the same high f_T value, which causes a large base resistor. So, reducing the thermal noise of the base resistance causes large shot noise, and vice versa. Hence, the noise performance of MOSFETs is superior to that of Si-BJTs. CMOS technology is also advantageous for low cost and large-scale integration.

Owing to these merits of the CMOS technology, many low-noise amplifiers (LNAs) using CMOS technology have been reported [3]–[7]. Considering the demand for systems with carrier frequency of over 5 GHz, realization of wireless ICs operable at over 5 GHz using CMOS technology is desirable. In this paper, we describe the performance of a 7-GHz LNA with a dual-gate MOSFET, and shielded pads used for its input and output ports. Improvements in low noise performance by adopting the dual-gate MOSFET and the shielded pads are discussed quantitatively.

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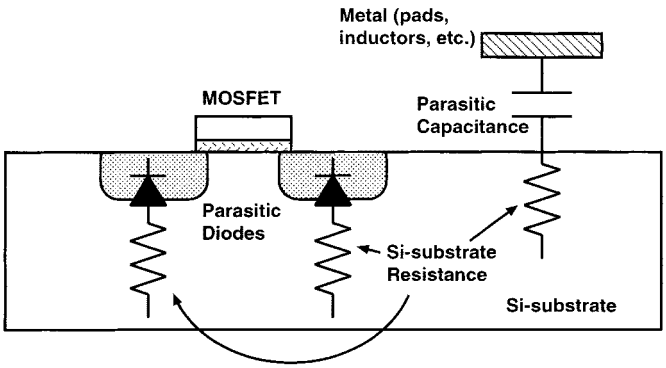

Fig. 1. Si-substrate resistance in CMOS technology.

II. Design Consideration for Low Noise Performance

A. Si-Substrate Resistance

At high frequency, the drain and source of a MOSFET, pads, inductors, and other elements on the Si substrate have resistive components due to resistivity of the Si substrate, as shown in Fig. 1. This parasitic resistance consumes signal power and generates thermal noise, and thus gain and noise performances of the LNA are degraded. Therefore, circuit techniques are required to reduce the effect of the resistivity due to the Si substrate in high-frequency circuit design. Here, two techniques are described for reducing the effect of the resistivity due to the Si substrate.

1) Dual-Gate MOSFET: Fig. 2 shows a schematic diagram of an LNA. A cascode configuration is chosen for improving high-frequency performance. The cascode configuration implemented using a dual-gate MOSFET is shown in Fig. 3. The area of the parasitic diodes at M1's drain and M2's source in Fig. 2 can be reduced significantly by using the dual-gate MOSFET. Part of the signal current output from M1 flows into the parasitic diodes, and this signal current is consumed by the Si-substrate resistance. Using the dual-gate MOSFET, this consumption in the Si substrate is reduced due to fact that the area of the parasitic diodes is small compared to that in the case using two conventional MOSFETs. In accordance with the design rule of MOSFETs, the area of the parasitic diode is reduced by a quarter using the dual-gate MOSFET in our case.

Circuit simulation results indicate that the LNA with the dual-gate MOSFET attains 1.2 dB higher gain (maximum

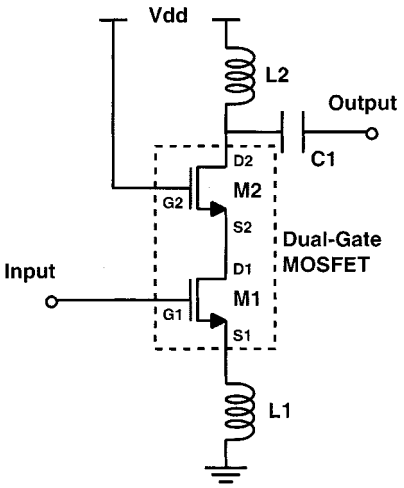

Fig. 2. Schematic diagram of LNA.

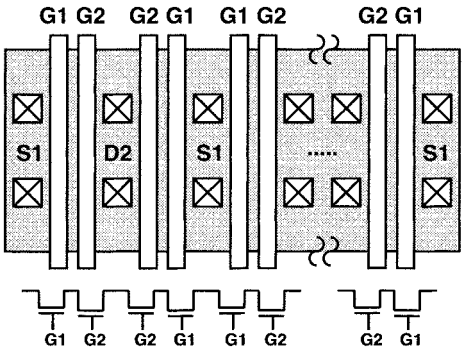

Fig. 3. Dual-gate MOSFETs.

available gain) and 0.7 dB lower noise figure (minimum noise figure) compared to the values in the case of conventional MOSFETs for M1 and M2.

2) Shielded Pads: Figs. 4 and 5 show structures and measured $S11$ characteristics for the unshielded conventional pad and the shielded pad, respectively. The conventional pad has a resistive component due to the Si-substrate resistance. Therefore, the measured result in Fig. 4 shows a capacitive characteristic with the parasitic resistance. The resistance value in the equivalent circuit shown in Fig. 4 is several tens of ohms, and this causes signal power loss and degrades gain and noise characteristics of the LNA. This degradation is particularly marked at high frequency of over 5 GHz.

To avoid such degradation, the shielded pads are used for input and output pads of the LNA [6]–[8]. This is because the shielded pads ideally have no resistive component, and so they consume no signal power and generate no noise. The measured result in Fig. 5 shows the characteristic to be the same as for a pure capacitance.

B. Other Factors Effective for Low Noise Performance

To reduce gate resistance of dual-gate MOSFET, salicided gate material and multifinger gate structure, shown in Fig. 3 are adopted.

An input matching circuit has a large effect on the noise performance. If the input matching circuit is composed using

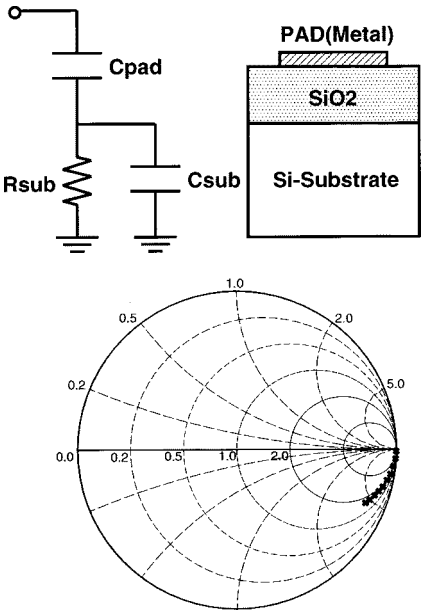

Fig. 4. Structure and measured $S11$ of the unshielded conventional pad (100 MHz–10 GHz).

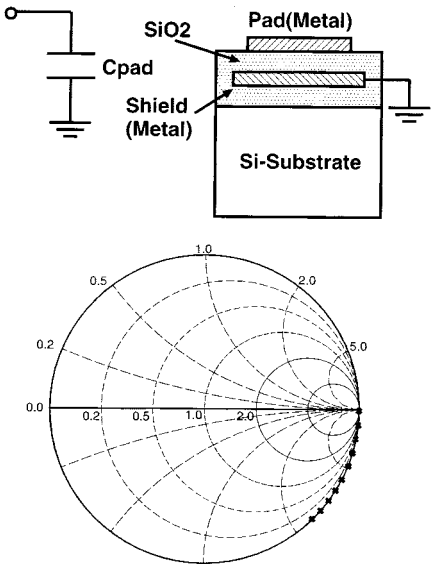

Fig. 5. Structure and measured $S11$ of the shielded pad (100 MHz–10 GHz).

on-chip elements with low Q values, the power of the input signal is greatly consumed in the resistive part of the on-chip input matching elements. To avoid such consumption, an external input matching circuit is indispensable for achieving very low noise performance.

Generally, a signal source impedance which achieves input impedance matching is different from that for the optimum noise figure. To achieve these conditions simultaneously, a degeneration inductor L1 should be connected to the source of M1 [9].

III. Measured Results

The LNA with a dual-gate MOSFET was fabricated using 0.25-μm CMOS technology. The Si-substrate resistivity is the medium value, i.e., 1–2 $\Omega\cdot$ cm, and so these parasitic resistances affect high-frequency circuit performances. Figs. 2 and 6 show

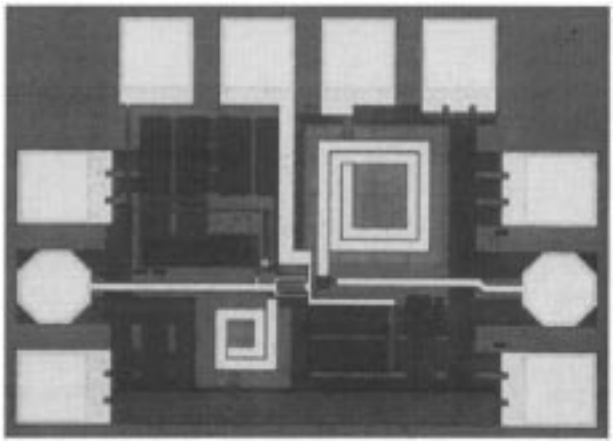

Fig. 6. Die photograph of LNA.

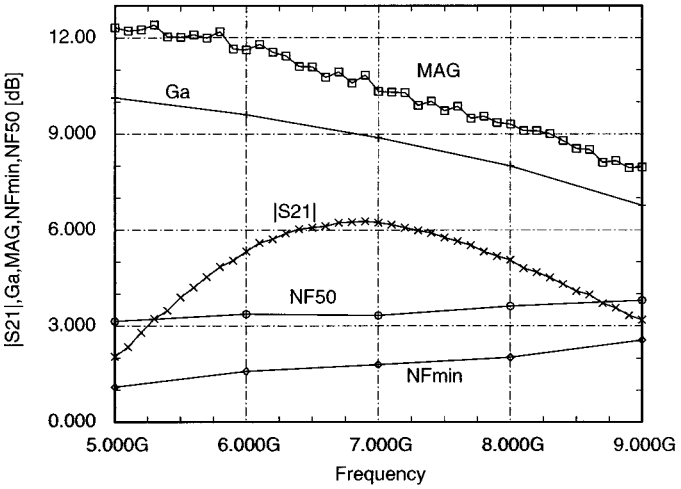

Fig. 7. Gains and noise figures of the LNA.

a circuit diagram and a die photograph of the LNA, respectively. The chip size including the area of the pads is 860 μm $\times$ 610 μm. The degeneration inductor L1, and the output matching elements L2 and C1 are integrated on the chip.

Measured results are obtained by using on-wafer probing technique. The power supply voltage is 2 V and the current consumption of the LNA is 6.9 mA.

Fig. 7 shows the frequency response of gain ($|S21|$, Ga, MAG) and noise figure (NFmin, NF50) for the LNA. $|S21|$, Ga, and MAG are the magnitude of $S21$, associated gain, and maximum available gain, respectively. NFmin is the minimum noise figure and NF50 is the noise figure when a signal source with 50-Ω impedance is connected directly to the LNA. NFmin of 1.8 dB and Ga of 8.9 dB are obtained at 7 GHz.

Fig. 8 shows $S11$, $S11^*$ from 5 to 9 GHz, and noise circles at 7 GHz. Γopt is the signal impedance which realize NFmin at 7 GHz, and $S11^*$ is the optimum signal impedance for impedance matching. $\Gamma\mathrm{opt}$ and $S11^*$ are close at 7 GHz, as shown in Fig. 8, owing to the degeneration inductor L1. This result indicates that both good impedance matching and low noise characteristic are realized simultaneously. For good impedance matching, the voltage standing-wave ratio (VSWR) should be less than 2; the input VSWR < 2 and NF < 2 dB can be satisfied by adding an appropriate matching circuit.

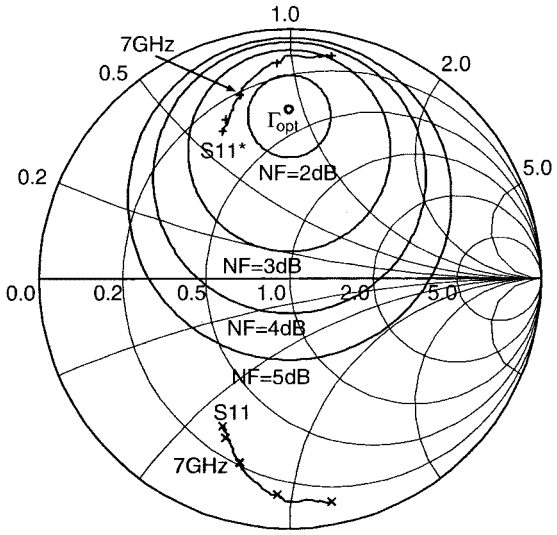

Fig. 8. $S11$ and noise circle of the LNA ($S11$, $S11^*$: 5–9 GHz).

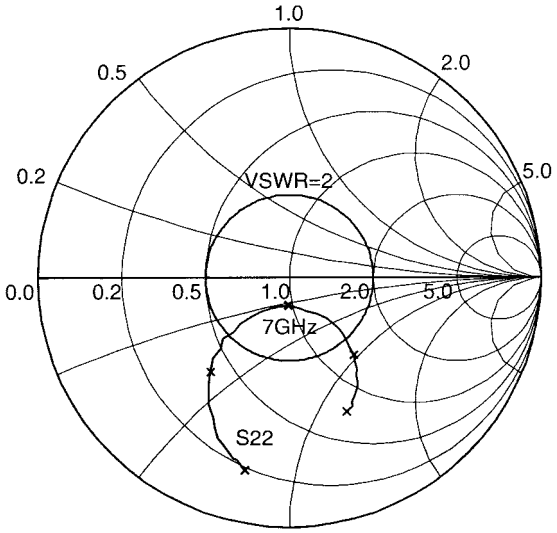

Fig. 9. $S22$ of the LNA (5–9 GHz).

Fig. 9 shows $S22$ of the LNA from 5 to 9 GHz. $S22$ is close to 50 Ω at 7 GHz owing to the on-chip output matching circuit, and the output VSWR is 1.3.

Fig. 10 shows intermodulation characteristics for the LNA with two-tone signal inputs ($f = 7.0$ GHz and 7.05 GHz). A very high input-referred third-order intercept point (IIP3) of $+8.4$ dBm is obtained without the input matching circuit. A 2.7 dB gain enhancement is achieved by adopting the input matching circuit which realizes NFmin at 7 GHz. In this case, the IIP3 is expected to be $+5.7$ dBm, and the LNA still attains high-linearity characteristic. Such a high IIP3 value is achieved due to the approximately square-low property of MOSFETs and appropriate valued degeneration inductor L1 of 0.3 nH. Table I summarizes the measured results of the LNA.

IV. Discussion

Generally, the Q value of a capacitive component is higher than that of inductors up to several GHz. At 7 GHz, the inductors used in the LNA have Q values of over 10 owing to low-re-

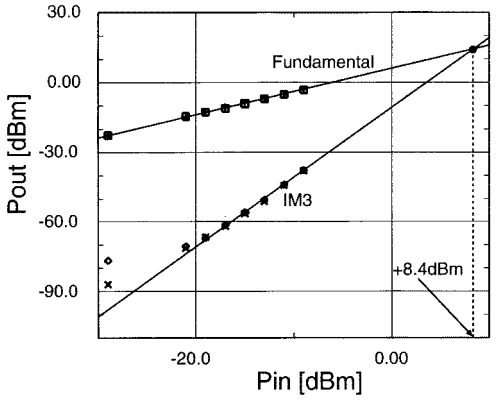

Fig. 10. IM3 characteristic of the LNA.

TABLE I
SUMMARY OF MEASURED RESULTS (WITHOUT INPUT MATCHING CIRCUIT)

Frequency[GHz]	7.0
Gain(|S21|)[dB]	6.2
Associated Gain(Ga)[dB]	8.9
MAG[dB]	10.3
NF50[dB]	3.3
NFmin[dB]	1.8
IIP3[dBm]	+8.4
Output VSWR	1.3
Supply Voltage[V]	2.0
Current Consumption[mA]	6.9

sistivity thick top-layer metal for the spiral and high operating frequency. But the Q value of the conventional pads is about 5, and this indicates signal power consumption due to the conventional pads is very significant at 7 GHz.

The effect of the shielded pads is evaluated by comparing the measured results of the LNA with the shielded pads and estimated results of the LNA with conventional pads. The correlation matrix [10] is used to calculate S parameters and noise parameters of the LNA with the conventional pads from the measured results of the LNA with the shielded pads and the measured results of the shielded and conventional pads.

Fig. 11 shows two-port representation of the LNA with the shielded pads. First, S parameters and noise parameters of the two-port network in Fig. 11 are measured using on-wafer probing techniques. The measured S parameters are transformed to Y parameters ($Y^{\mathrm{LNA,\,Shield}}$), and the correlation matrix in chain representation $C_A^{\mathrm{LNA,\,Shield}}$ of the LNA with the shielded pads is written as

$$C_A^{\mathrm{LNA,\,Shield}} = 2kT \begin{bmatrix} Rn & \dfrac{F\min-1}{2} - RnY\mathrm{opt} \\ \dfrac{F\min-1}{2} - RnY\mathrm{opt}^* & Rn|Y\mathrm{opt}|^2 \end{bmatrix} \quad (1)$$

using the measured noise parameters $F\min$, Rn, and $Y\mathrm{opt}$ ($=G\mathrm{opt} + jB\mathrm{opt}$). So, the correlation matrix in admittance representation $C_Y^{\mathrm{LNA,\,Shield}}$ is transformed from $C_A^{\mathrm{LNA,\,Shield}}$ using transform matrix T and its Hermitian conjugate $T^\dagger$

$$C_Y^{\mathrm{LNA,\,Shield}} = TC_A^{\mathrm{LNA,\,Shield}}T^\dagger. \quad (2)$$

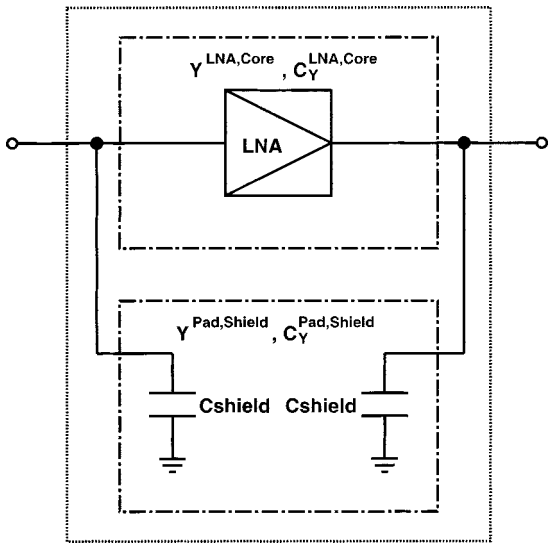

Fig. 11. LNA with shielded pads.

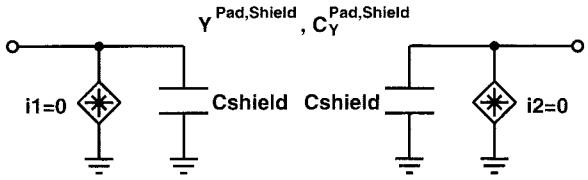

Fig. 12. Two-port representation of the shielded pads.

Fig. 12 shows two-port representation of the shielded pads only. Y parameters ($Y^{\mathrm{Pad,\,Shield}}$) and the correction matrix $C_Y^{\mathrm{Pad,\,Shield}}$ are clearly written as

$$Y^{\mathrm{Pad,\,Shield}} = \begin{bmatrix} j\omega C_{\mathrm{shield}} & 0 \\ 0 & j\omega C_{\mathrm{shield}} \end{bmatrix} \quad (3)$$

$$C_Y^{\mathrm{Pad,\,Shield}} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}. \quad (4)$$

C_{shield} is easily extracted for the measured S parameters of the two-port network in Fig. 12. So, Y parameters ($Y^{\mathrm{LNA,\,Core}}$) and the correction matrix ($C_Y^{\mathrm{LNA,\,Core}}$) for the LNA without any pads are

$$Y^{\mathrm{LNA,\,Core}} = Y^{\mathrm{LNA,\,Shield}} - Y^{\mathrm{Pad,\,Shield}} \quad (5)$$

$$C_Y^{\mathrm{LNA,\,Core}} = C_Y^{\mathrm{LNA,\,Shield}} - C_Y^{\mathrm{Pad,\,Shield}}. \quad (6)$$

The Norton's equivalent circuit of the conventional pads, shown in Fig. 13, can be extracted from the measured S parameters, and Y parameter (Y^{pad}) and the correction matrix (C_Y^{pad}) of the two-port network in Fig. 13 are written as

$$Y^{\mathrm{Pad,\,Conv}} = \begin{bmatrix} Y_{\mathrm{eq}} & 0 \\ 0 & Y_{\mathrm{eq}} \end{bmatrix} \quad (7)$$

$$C_Y^{\mathrm{Pad,\,Conv}} = \begin{bmatrix} \overline{i_{\mathrm{eq}} i_{\mathrm{eq}}^*} & 0 \\ 0 & \overline{i_{\mathrm{eq}} i_{\mathrm{eq}}^*} \end{bmatrix}. \quad (8)$$

From (5)–(8), Y parameters ($Y^{\mathrm{LNA,\,Conv}}$) and the correction matrix ($C_Y^{\mathrm{LNA,\,Conv}}$) for the LNA with the conventional pads are written as

$$Y^{\mathrm{LNA,\,Conv}} = Y^{\mathrm{LNA,\,Core}} + Y^{\mathrm{Pad,\,Conv}} \quad (9)$$

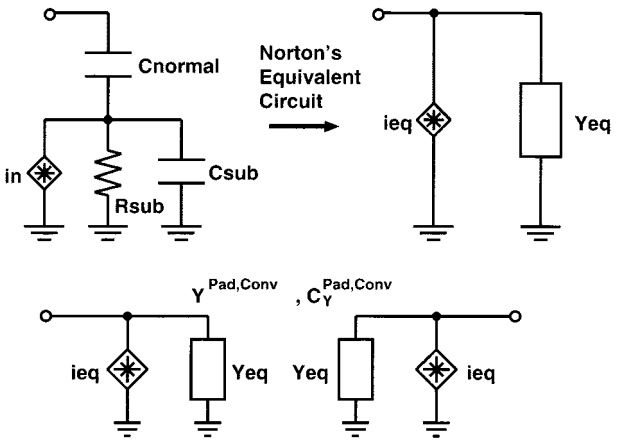

Fig. 13. Two-port representation of the unshielded conventional pads.

TABLE II
Ga AND NFmin FOR THE LNA

	Ga [dB]	NFmin [dB]
with shielded pads	8.9	1.8
with unshielded conventional pads	4.9	2.6

$$C_Y^{\mathrm{LNA,\,Conv}} = C_Y^{\mathrm{LNA,\,Core}} + C_Y^{\mathrm{Pad,\,Conv}}. \tag{10}$$

Then, we can transform S parameters and the noise parameters of the LNA with the conventional pads from $Y^{\mathrm{LNA,\,Conv}}$ and $C_Y^{\mathrm{LNA,\,Conv}}$.

Table II shows Ga and NFmin of the LNA with the shielded pads and conventional pads. These results indicate that 4-dB gain loss and 0.8-dB NF degradation occurs in the case of using the conventional pads.

Colvin *et al.* [8] compared the values of $|S21|$ and NF50 to evaluate the effect of the shielded pads. Because their results include the effect of the reflection for the impedance mismatch, they are not exact for the evaluation of the effect of the shielded pads. To avoid the effect of the reflection, we adopt the values of Ga and NFmin for comparison.

V. CONCLUSION

The circuit design and measured results of the 7-GHz LNA using 0.25-μm CMOS technology were presented. The dual-gate MOSFET and the shielded pads enhance the gain and improve the noise figure of the LNA. In particular, numerical comparisons between the LNA with the shielded and conventional pads are discussed in terms of low noise and high gain. The results of the comparison indicate that the shielded pads improve the noise figure by 0.8 dB and gain by 4 dB at 7 GHz. CMOS LNAs are available for wireless systems of over 5-GHz carrier frequency using the dual-gate MOSFET and the shielded pads.

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