Substrate Noise Generation in Complex Digital Systems: Efficient Modeling and Simulation Methodology and Experimental Verification

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***Abstract*—More and more system-on-chip designs require the integration of analog circuits on large digital chips and will therefore suffer from substrate noise coupling. To investigate the impact of substrate noise on analog circuits, information is needed about digital substrate noise generation. In this paper, a recently proposed simulation methodology to estimate the time-domain waveform of the substrate noise is applied to an 86-Kgate CMOS ASIC on a low-ohmic epi-type substrate. These simulation results have been compared with substrate noise measurements on this ASIC and the difference between the simulated and measured substrate noise rms voltage is less than 10%. The simulated time domain waveform and frequency spectrum of the substrate noise correspond well with the measurements, indicating the validity of this simulation methodology. Both measurements and simulations have been used to analyze the substrate noise generation in more detail. It has been found that direct noise coupling from the on-chip power supply to the substrate dominates the substrate noise generation and that more than 80% of the substrate noise is generated by simultaneous switching of the core cells. By varying the parameters of the simulation model, it has been concluded that a flip-chip packaging technique can reduce the substrate noise rms voltage by two orders of magnitude when compared to traditional wirebonding.**

***Index Terms*—Crosstalk, integrated circuit modeling, interference, mixed analog–digital integrated circuits, substrate noise.**

I. Introduction

THE NEED for ever-smaller electronic devices leads to the development of highly integrated mixed-signal ICs [1]. This integration of analog and digital circuits on one silicon substrate will cause substrate noise-coupling problems: the performance of the analog circuits will degrade due to substrate noise generated by the digital circuits. To analyze the substrate noise-coupling problem before the chip is fabricated, information is needed on the substrate noise that is generated by the digital part of the design and on the impact that this substrate noise will have on the performance of the analog circuits. For analog parts on a chip, it is possible, using commercially available CAD tools [2], to extract a SPICE model of the substrate and to study the impact of substrate noise on the performance of this analog circuit using SPICE simulations. For an accurate simulation of noise impact, however, the exact noise signal on the substrate must be known. Since it is not possible to simulate noise generation of large digital circuits at SPICE level, a new simulation methodology is needed. Simulation methodologies have been presented that make it possible to simulate the total noise current that is injected in the substrate by a digital design [3] or that can estimate the total noise power that is generated [4]. These techniques do not simulate the actual waveform of the voltage noise on the substrate, which is needed to simulate performance degradation of integrated analog circuits. Also, no verification of these methodologies with substrate noise measurements on realistic large ASICs have been shown. Most substrate noise experiments have been carried out on test chips with dedicated digital substrate noise generators [5], [6] or using only small digital CMOS circuits [7]. In previous work, we have described a simulation methodology that makes it possible to accurately and efficiently simulate the substrate noise voltage [8], [9] and the verification of this methodology with SPICE simulations for a small digital circuit of 1 Kgates. This paper will present an extension to that simulation methodology and show how it can be applied on a real digital signal processing ASIC, fabricated on a low-ohmic epi-type substrate. The substrate noise generation of this ASIC has been measured and corresponds very well with the simulation results. It will also be shown how this simulation methodology can help in the identification of the major substrate noise sources.

First, the sources of substrate noise generation and the simulation methodology are described. Next, the experimental ASIC is presented, and it is shown how the simulation methodology is applied for this ASIC. The resulting substrate noise simulations are compared with substrate noise measurements on this ASIC. Finally, the substrate noise generation is analyzed in more detail, showing the relationship between substrate noise generation and switching cell types, power-supply consumption, and package parasitics.

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II. Substrate Noise Simulation Methodology

This section describes the substrate noise simulation methodology that is used to analyze noise generation of large digital ASICs. First, a brief introduction is given about the sources of substrate noise in digital circuits.

A. Identification of the Noise Sources

In order to model and simulate substrate noise generation, it is important to first identify the major sources of substrate noise generation, namely, noise coupling from the switching transistors and noise coupling from the on-chip power supply [10].

Substrate noise is generated by switching transistors in two ways: capacitive coupling from active areas and from the gate to the substrate and, depending on the technology, by impact ionization. These noise generating mechanisms are all included in transistor models such as the BSIM3v3 model.

The second source of noise generation is noise coupling from the on-chip power supply to the substrate. The power-supply noise is caused by the package parasitics, such as bondwire inductance and resistance, in combination with the large power-supply current spikes that are generated by the switching CMOS circuits. Normally, the on-chip ground is connected in every standard cell to the substrate to prevent latchup. Due to these connections, all the noise on the digital ground will directly couple to the substrate. Because of the parasitic package and wirebond inductance in the power-supply lines, which is in series with the circuit capacitance between power and ground, ringing of the on-chip power supply can also occur. This ringing will couple directly to the substrate and is visible in the frequency spectrum of the generated substrate noise.

Both noise sources should be taken into account when simulating the substrate noise generation of digital circuits. Since the on-chip power-supply noise depends on the package parasitics, a package model must also be included in the simulation. When only the noise generation from the switching transistors is taken into account, as is presented in [3], then the substrate noise level will be underestimated, as will be shown later from our simulation results.

B. Overview of the Simulation Methodology

The substrate noise simulation methodology [8], shown in Fig. 1, consists of three parts. The first part is the library characterization which must be performed once for each new technology. During the library characterization, a substrate noise macro model is created of every standard cell, and the noise injection currents are extracted for every possible switching activity for every standard cell. The standard VHDL gate-level simulation library is also extended to enable the extraction of all switching events during a normal VHDL gate-level simulation.

The second part of the methodology starts with a given gate-level netlist of a digital design. From this netlist, a chip-level simulation model is created, using the previously extracted macro models for each separate gate. A model for the package parasitics is also added to the chip-level simulation model. Next, the gate-level netlist is used in a normal gate-level simulation, using the extended simulation library. The output of this simulation is a listing with all switching events. These switching events are used to calculate the total noise current waveform, using the current waveforms extracted in step one for each individual gate.

The third part of the methodology is the actual simulation of the substrate noise voltage. This is done by combining the chip-level simulation model with the total noise current sources, and solving this circuit with, for example, a SPICE simulator, to obtain the substrate noise voltage.

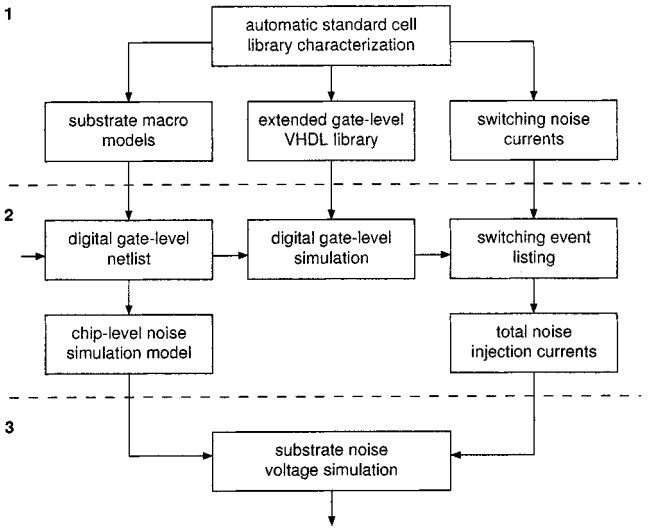

Fig. 1. Three-step substrate noise waveform simulation methodology.

III. Experimental Results

To verify the substrate noise simulation methodology, a digital signal processing ASIC has been designed on which the generated substrate noise voltage can be measured. In this section, it is explained how the substrate noise simulation methodology has been applied to this ASIC, and the simulation results are compared with measurements.

A. Experimental Digital ASIC

Previously, most substrate noise experiments have been performed using dedicated test chips or using only small CMOS circuits. Our experimental ASIC consists of an 86-Kgate digital signal processing circuit combined with analog substrate noise sensors to measure the substrate noise voltage [11], designed in a low-ohmic epi-type 0.5-μm CMOS technology. The digital circuit is a multirate up/down converter and channel select filter for cable modem applications [12]. This chip can upconvert or downconvert 12-bit I/Q data by a factor of 16 and perform channel selection. Fig. 2 shows the microphotograph of this chip and the location of the analog substrate noise sensors. These sensors amplify the substrate voltage by 3 dB in the frequency band from 20 kHz to 1 GHz [11].

For the substrate noise measurements, a 12-bit I/Q random data stream is provided to the ASIC by a digital pattern generator. The output data is observed with a logic analyzer. The load of this logic analyzer, seen by each output buffer of the ASIC, is around 12 pF in parallel with 100 kΩ.

B. Applying the Simulation Methodology

The first part of the methodology, namely, the library characterization, has already been performed [8] and will not be described here. It is, however, important to note that the effect of

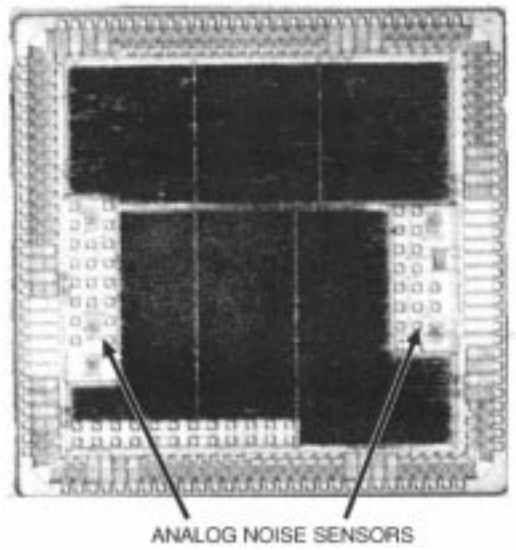

Fig. 2. Micrograph of the Robo4 ASIC, showing the location of the substrate noise sensors.

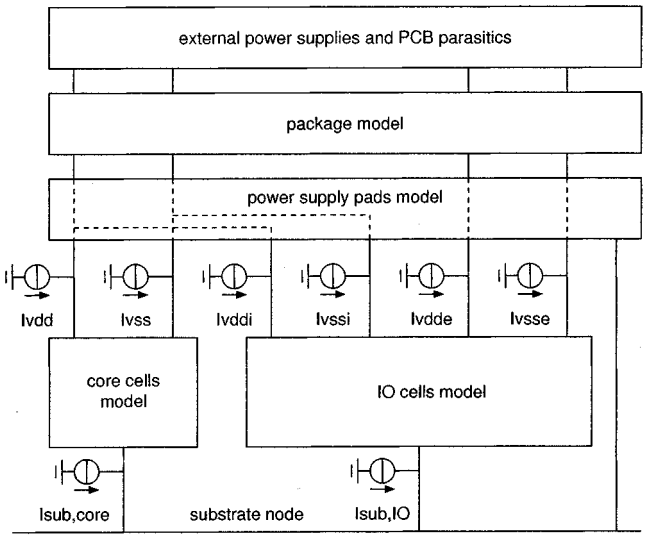

Fig. 3. General chip-level substrate noise simulation model.

the external load (formed by the logic analyzer) on the substrate noise generation of the output buffers is taken into account in this part of the library characterization and is included in the noise current waveforms that are injected into the substrate.

The second part of the methodology starts with the generation of a chip-level substrate noise simulation model from the gate-level netlist of the digital ASIC. This model includes connections between all power-supply nodes and the substrate. The substrate noise that is generated by switching digital signals is incorporated into a number of noise current sources that model the injection of noise into the substrate and the consumption of power-supply current. An example of such a chip-level model is shown in Fig. 3. The different blocks in this model are the core cells, the IO cells, the power-supply pads, the package parasitics, and the external sources and parasitics. The waveform of the current sources in this model is determined after the gate-level simulation by combining all switching events with the waveforms for each individual event.

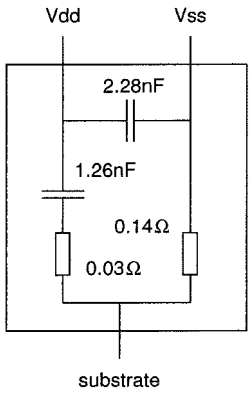

Fig. 4. Macro model of all core cells combined in parallel.

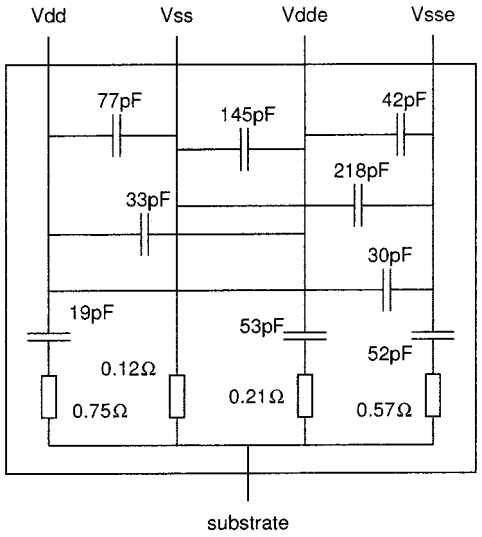

Fig. 5. Macro model of all IO buffers and power-supply pads combined in parallel.

The core cell model, shown in Fig. 4, is created by placing all models of every gate used in the design in parallel. The individual models can be placed in parallel because a low-ohmic epi-type substrate has been used and the entire substrate can be considered as one electrical node. It can be seen that the total resistance between the on-chip ground V_{ss} and the substrate, from all the substrate contacts placed in parallel, is very low (0.14 Ω), so all noise on the on-chip ground will also be present on the substrate.

The model used for the IO cells and power-supply pads has the same configuration, so one combined model can be created for all IO cells and power-supply pads in parallel. This model is shown in Fig. 5. The only difference between the IO cells and power-supply pads is that the IO cells are active switching cells and contribute to the noise generation. The power-supply pads are passive cells and only contribute to the impedance values in the final model.

Next, a model for the package must be added. This model can represent the real package of the chip with extracted or calculated model parameters, but it can also be used to explore different packaging options, by using variable parameters in this model. The experimental ASIC has been mounted in a 120-pin ceramic pin grid array (CPGA) package. The package para-

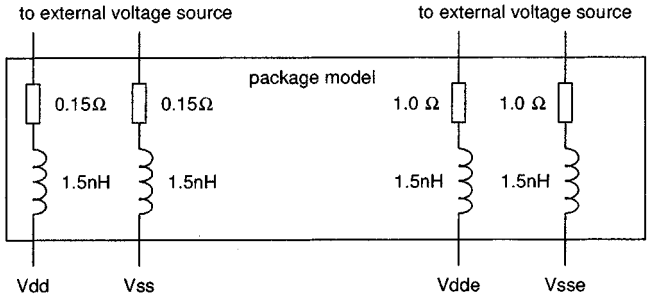

Fig. 6. Macro model of the power-supply connections for the CPGA package.

sitics of the power-supply connections have been obtained by measuring the impedance of a power-supply pin pair with a network analyzer. An average inductance value of 12 nH for one connection from chip to package pin has been measured. These impedance measurements can also be used to check the total on-chip capacitance that is connected over a power supply. The capacitance values that have been measured correspond well with the extracted model parameters. Since for each supply eight parallel connections have been used, an inductance value of 1.5 nH has been used in the package model. This model is shown in Fig. 6.

Finally, a model for the external power-supply sources and possible printd circuit board (PCB) components and/or parasitics can be added. In the simulation model for the experimental ASIC, everything that is external to the packaged chip is considered as ideal, and only two perfect power-supply sources are included. Parasitic components such as series resistance in decoupling capacitors on the PCB have been included in the series resistance of the package model. This resistor value is the only fitting parameter in the entire model. All other model parameters are automatically calculated from the gate-level netlist of the digital design and a circuit level SPICE netlist is automatically created for the chip-level simulation model.

C. Obtaining the Noise Current Waveforms

Next, the waveforms of the current sources in the chip-level simulation methodology have to be calculated. This is realized by first doing a normal gate-level simulation of the digital circuit, for a particular test bench, with the extended simulation library. Because the extended simulation library is used, every switching event on an input pin of a digital gate is recorded to an output file. This output file lists the time occurrence, switching type, and cell type of each switching event. The total noise current source waveform can now be calculated by adding the waveform for each individual event to the total noise current source.

In the final simulation model, the substrate noise generation is modeled by current sources that represent noise injection into the substrate by switching gates ($I_{\mathrm{sub,\,core}}$ and $I_{\mathrm{sub,\,IO}}$), power-supply current consumption for the core cells ($I_{V_{dd}}, I_{V_{ss}}$), and power-supply current consumption for the IO cells ($I_{V_{ddi}}, I_{V_{ssi}}, I_{V_{dde}}, I_{V_{sse}}$).

These final waveforms are only valid for one particular digital gate-level simulation testbench, while the simulation model itself is entirely defined by the gate-level netlist. With the calculated current waveforms and the chip-level simulation model, the substrate noise generation can now be simulated.

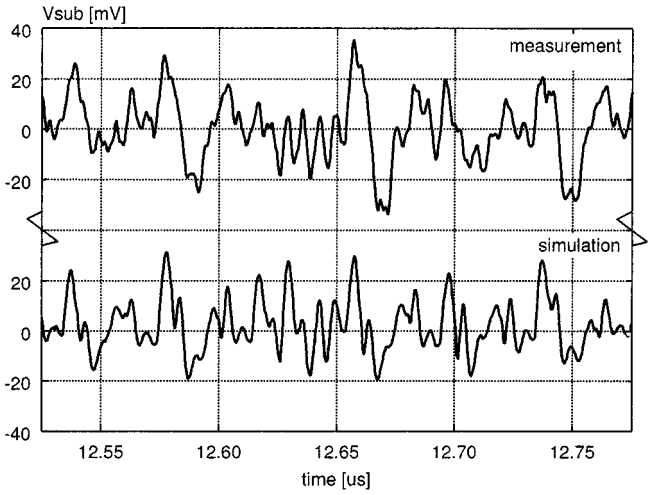

Fig. 7. Comparison of measured and simulated substrate noise generation when the digital circuit is performing 16 times upconversion from 3.125 to 50 MHz.

TABLE I
COMPARISON OF MEASURED AND SIMULATED RMS AND PEAK-TO-PEAK SUBSTRATE NOISE VOLTAGES IN A 5-μs TIME PERIOD

	measurement	simulation	error
Vsub,rms	13.3 mV	12.0 mV	9.8 %
Vsub,pp	80.6 mV	96.0 mV	19 %

D. Comparison With Measurements

Fig. 7 shows a comparison of the measured and simulated substrate noise voltage when the digital circuit is operating in 16 times upconversion mode. An external clock source of 50 MHz is used that is internally divided by 16, which results in data being upconverted from the 3.125-MHz clock domain to the 50-MHz clock domain. The rms value of the measured substrate noise voltage in a 5-μs time period is 13.3 mV. For the same time period, the rms value of the simulated substrate noise voltage is 12.0 mV, which differs 9.8% from the measurement. The maximum peak-to-peak substrate noise voltage is 80.6 mV for the measurement and 96.0 mV for the simulation. These data are summarized in Table I.

Fig. 8 shows a fast Fourier transform (FFT) of the measured and simulated substrate noise voltage. The difference in the total power of the measured and simulated spectrum is only 1 dB. The same difference is found when only the total power at all clock multiples (of 3.125 MHz) or only the total power in the noise floor are compared. The largest difference between a measured and simulated noise peak at multiples of the 50-MHz clock is 5 dB. Table II gives an overview of these comparisons.

Fig. 8 shows that most noise is generated at multiples of the lowest clock frequency of 3.125 MHz. The noise level at the clock multiples can easily be 40 dB above the substrate noise floor. Other effects such as ringing of the digital power

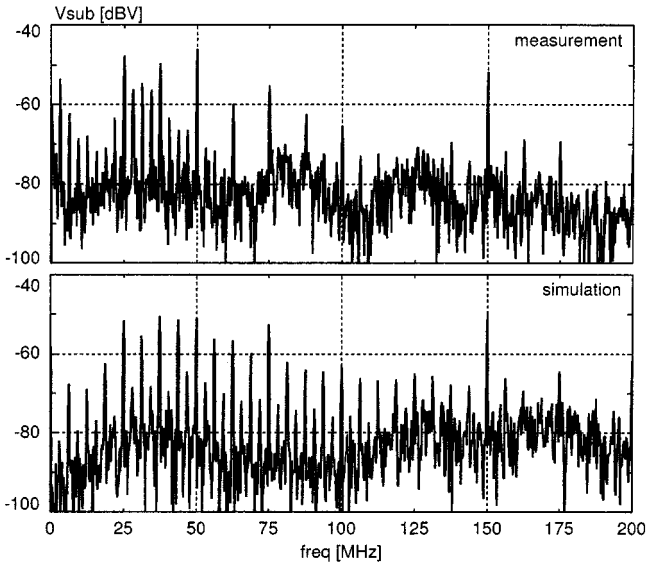

Fig. 8. Comparison of measured and simulated substrate noise generation in the frequency domain.

TABLE II
COMPARISON OF MEASURED AND SIMULATED SUBSTRATE NOISE POWER AND AMPLITUDE WITH $F_{\mathrm{CLK}} = 50$ MHZ AND FOR A TIME WINDOW OF 4.8 μs. NOTE THAT THE POWER HAS BEEN CALCULATED IN A 50-Ω LOAD ONLY AS REFERENCE

	measurement	simulation	error
Psub total	-25.8 dBm	-26.8 dBm	1 dB
Psub at n/16 * Fclk	-27.9 dBm	-28.9 dBm	1 dB
Psub in noise floor	-30.0 dBm	-31.0 dBm	1 dB
Vsub at Fclk	-46 dBV	-51 dBV	5 dB
Vsub at 2*Fclk	-65 dBV	-63 dBV	2 dB
Vsub at 3*Fclk	-52 dBV	-50 dBV	2 dB

supply can also be recognized in the substrate noise frequency spectrum. The combination of the bondwire inductance and the on-chip circuit capacitance over the power supply forms an *LC* tank that oscillates at a specific frequency. This oscillation or ringing frequency can be recognized in the frequency spectrum of the substrate noise signal. From the extracted bondwire inductance and on-chip capacitance, it follows that this frequency is around 40 MHz, and in the measured and simulated frequency spectra, there is indeed an increase of substrate noise with 10–20 dB around this frequency.

IV. SUBSTRATE NOISE ANALYSIS

The chip-level substrate noise simulation model can be used to analyze the major sources of substrate noise generation. This can be done by disabling certain noise current sources or changing the package model. This section describes a number of experiments that analyze the substrate noise generation by changing the simulation model.

A. Core Cell Versus IO Cell Switching

Fig. 9 shows the measured and simulated substrate noise voltage for 16 times upconversion of data from the 3.125-MHz

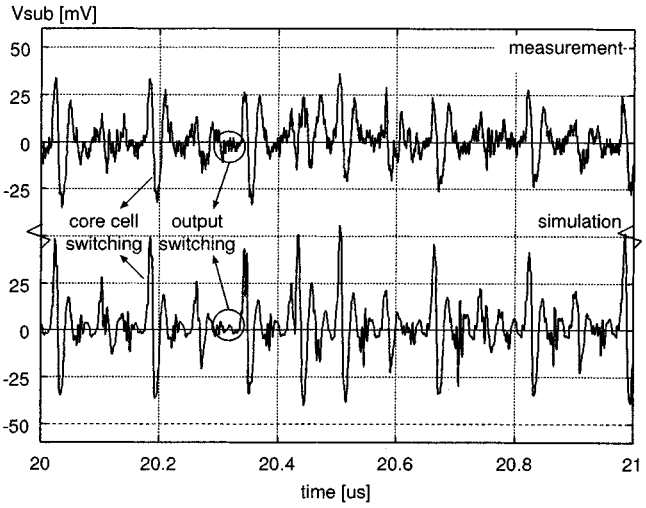

Fig. 9. Measured and simulated substrate noise voltage with indication of the noise sources.

clock domain to the 50-MHz clock domain. By comparing this measured signal with the gate-level simulation, the major noise contributors can be identified. From this comparison, it can be concluded that the major noise spikes are generated by simultaneous switching of a large number of core cells (mainly flip-flops) at each clock edge of the 3.125-MHz clock. For this operation mode of the circuit, the switching of the output buffers generates only a minor noise contribution.

When the substrate noise simulation is performed with only the noise current sources for the core part active, or only the noise current sources for the IO cells active, it is possible to quantify the noise contribution of the IO cells. For this simulation, the IO cells generate 18% of the total rms substrate noise voltage. When the circuit is operating in downconversion mode, with data output at the slow clock frequency, the IO cells only contribute 7% of the total substrate noise power. These results indicate that simultaneous switching activity of a large number of core cells can be a dominant source of substrate noise generation. The noise generation of the IO buffers is, however, very much dependent on technology, circuit operation, and even PCB design (e.g., output impedance), and cannot be neglected.

B. Substrate Noise Versus Clock Frequency and Supply Voltage

To check the relationship between substrate noise generation and power consumption, the substrate noise rms voltage has been measured as function of the supply voltage V_{dd} and the clock frequency. The results are shown in Fig. 10. It can be seen that the rms value of the substrate noise voltage scales linearly with the supply voltage and scales with the square root of the frequency. This means that the substrate noise power scales as expected in the same way as the CMOS dynamic power consumption.

C. Substrate Noise Versus Package Parasitics

The parameters of the package model (the value of the inductance and resistance) can be easily changed in the simulations to analyze the effect of these parasitics on the total substrate noise

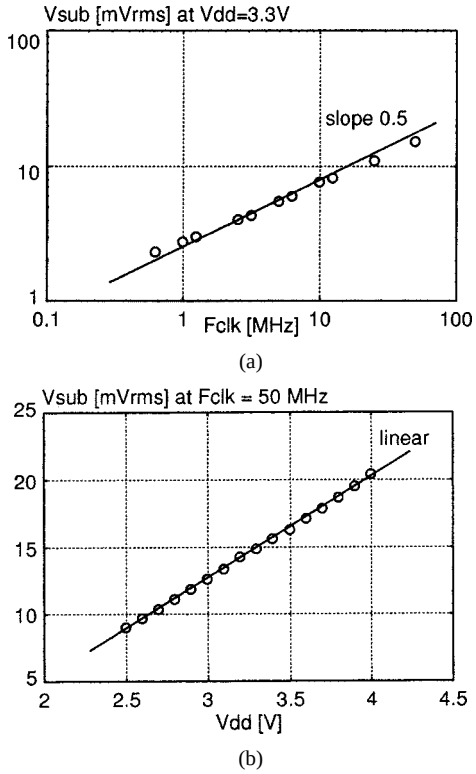

Fig. 10. Measured rms substrate noise voltage versus (a) clock frequency and (b) supply voltage.

generation. In this way, it is also possible to explore different packaging options for a chip.

Fig. 11 shows the simulated rms substrate voltage for the experimental ASIC versus the inductor and resistor value of these package parasitics. Indicated in this figure by "W" is the approximate location of the parasitics from the CPGA package in which the chip was wirebonded (12 nH in series with 1 Ω for every connection). Indicated by "C" is the approximate location of the package parasitics (1 nH in series with 0.1 Ω) for a Ball grid array (BGA) chip scale package (CSP) [13]. Indicated by "F" is the approximate location of the parasitics for an ideal flip-chip mounting in which only the parasitics of the flip-chip bumps (10 pH in series with 30 mΩ) have been taken into account [14].

It can be seen that packaging with lower parasitic inductance can offer a large decrease of substrate noise. Despite the flip-chip mounting used in the CSP, this package still has large parasitics from the redistribution traces, and the substrate noise generation is only about 3 times less than for the CPGA package. In the ideal case, with only package parasitics from the flip-chip bumps, the substrate noise is reduced by two orders of magnitude. But even for this ideal case, the substrate noise is still dominated by noise coupling from the power supply, since the absolute minimum level of substrate noise is still around one order of magnitude lower. This minimum substrate noise level corresponds to a situation without any power-supply noise. All substrate noise is then generated by the switching transistors.

It can also be seen that at high inductance values the rms substrate noise can be reduced by optimizing the parasitic series resistance. This can be explained by the fact that with these high inductance values the substrate noise is dominated by coupling of ringing from the power supply. This ringing can be reduced (damped) when the series resistance is set to a certain optimum value [15]. For higher series resistance values, the resistive voltage drop begins to dominate the noise generation.

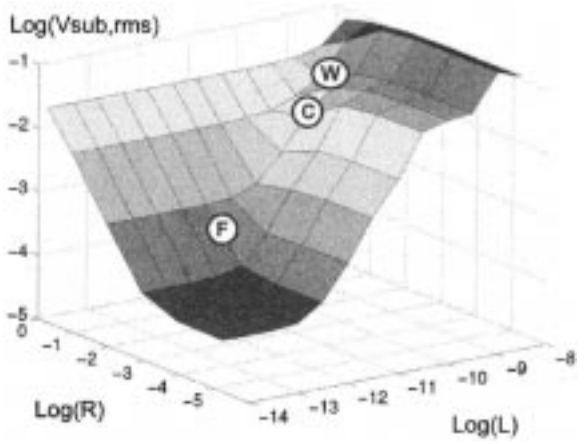

Fig. 11. Simulated rms substrate voltage versus parasitic package inductance and resistance.

TABLE III
COMPARISON OF SIMULATION TIMES FOR THE ROBO4 ASIC AND A SMALL 1-KGATE DIGITAL CIRCUIT

	Robo4 ASIC 86 Kgates	multiplier 994 gates
Simulated time	1 μs	5 μs
No. switching events	150000	63500
Clock frequency	50 MHz	42 MHz
Full SPICE level simulation	N/A	37 hours
VHDL gate-level simulation	11:27 min	29 sec
Substrate noise simulation	12:30 min	55 sec
Speedup	N/A	1586 x

These simulations show the importance of package parasitics in substrate noise generation and also indicate that simulating substrate noise without power-supply noise coupling will result in noise levels that are much too low. Therefore, the problem of substrate noise coupling should always be examined for packaged ASICs and even external parasitics from a PCB need to be taken into account.

Table III gives an overview of the simulation times for this experimental ASIC and for a smaller 1-Kgate circuit. The substrate noise simulation time for the ASIC is about the same as the VHDL gate-level simulation time. Comparison with a full SPICE simulation of the digital circuit with its substrate model is not feasible due to the circuit size. For a 1-Kgate circuit, the speedup with respect to a full SPICE simulation is more than 1500 times.

V. CONCLUSION

An efficient and accurate simulation methodology for substrate noise generation of large digital circuits has been presented. This methodology makes it possible to simulate an accu-

rate time waveform of the substrate noise voltage, generated by a digital circuit for a particular gate-level simulation. To verify this simulation methodology, it has been applied to an 86-Kgate CMOS ASIC. The simulated rms substrate noise voltage differs less than 10% from measurements. From measurements and simulations, it can be concluded that most substrate noise is generated from direct coupling of on-chip power-supply noise to the substrate. Because the power-supply noise determines the substrate noise, it is very important to take the complete packaged chip into account when analyzing the substrate noise levels.

This simulation methodology can be used to quickly evaluate substrate noise generation of packaged digital ASICs. Because of the efficient way in which the simulations are perfomed, this methodology can not only be used as final verification of a finished design, but can also be used during the design phase, to study the impact of, e.g., gate-level synthesis options on the substrate noise generation.

By varying the package parasitics, it has been observed that low-parasitics packaging techniques can reduce the rms substrate voltage level by two orders of magnitude. But even for the ideal flip-chip mounting technique, the power-supply noise still dominates the substrate noise generation. Effects such as ringing or ground bounce of the power supply, which cause extra substrate noise generation, can also be identified from the simulations.

This simulation methodology, in which all power-supply connections to the substrate are modeled and the substrate noise generation from switching signals is included in a number of noise current sources, has proven to be a useful and effective way to estimate the total substrate noise voltage and also allows identification of the major noise contributors and simulate the effect of the environment (e.g., package, PCB) on the substrate noise generation.

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