RF Circuit Design Aspects of Spiral Inductors on Silicon

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***Abstract*—The design and optimization of spiral inductors on silicon substrates, the related layout issues in integrated circuits, and the effect of the inductor-Q on the performance of radio-frequency (RF) building blocks are discussed. Integrated spiral inductors with inductances of 0.5–100 nH and Q's up to 40 are shown to be feasible in very-large-scale-integration silicon technology. Circuit design aspects, such as a minimum inductor area, the cross talk between inductors, and the effect of a substrate contact on the inductor characteristics are addressed. Important RF building blocks, such as a bandpass filter, low-noise amplifier, and voltage-controlled oscillator are shown to benefit substantially from an improved inductor-Q.**

I. Introduction

SPIRAL inductors are important, performance-limiting components in monolithic radio-frequency (RF) circuits, such as voltage-controlled oscillators (VCO's), low-noise amplifiers (LNA's), and passive-element filters [1], [2]. The quality factor (Q) of the inductors is limited by the resistive losses in the spiral coil and by the substrate losses [$Q = \text{im}(Z)/\text{re}(Z)$ with Z the impedance of the inductor]. It has been shown recently that high Q's can be achieved in state-of-the-art silicon fabrication processes [3], [4]. Here, we discuss inductor optimization for RF circuit design and specific layout issues, verified by experiments. In particular, design, modeling, and specific circuit layout issues of spiral inductors on silicon substrates are discussed in Section II. In Section III, we evaluate and demonstrate the significance of the inductor-Q in three basic RF circuits, and Section IV will provide a summary of the results and some conclusions.

II. Design and Circuit Implementation of Spiral Inductors on Silicon

A. Basic Design, Modeling, and Optimization

A spiral inductor can be built on a silicon substrate by using the multilevel interconnects that are routinely provided with today's mainstream silicon fabrication processes. A minimum of two metal layers is needed to build the basic spiral coil (M3 in Fig. 1) and an underpass contact (M2 in Fig. 1) to return the inner terminal of the coil to the outside. The lateral structure of an inductor is defined by the number of turns (n), the wire width (W) and space (S), and the total area covered $(d_o x d_o)$,

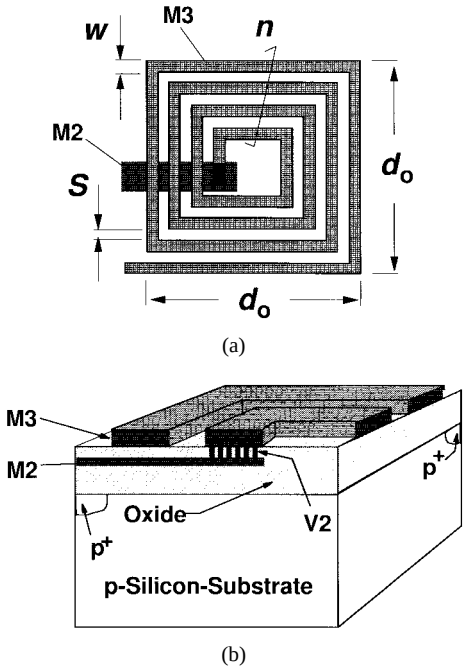

Fig. 1. (a) Plan and (b) cross-sectional views of a spiral inductor structure (metal layer M1 is omitted to reduce C_{Ox}).

as shown in Fig. 1(a). A simple lumped-element model is instrumental in describing the electrical device characteristics (Fig. 2). The spiral coil itself is modeled by an ideal inductance (L_s), a series resistance (R_s), representing the ohmic losses in the coil, and an interwire capacitance (C_p). With the integration on a silicon substrate, oxide capacitances (C_{Ox}) and bulk resistances (R_B) have to be added to the model to represent the RF signal flow through the silicon substrate (the capacitance of the silicon substrate was neglected). In BiCMOS processes, silicon substrates with a typical resistivity of 10 Ω-cm are used so that eddy currents in the silicon are negligible [3]. CMOS, in contrast, usually has p/p^+ substrates ($\ll$0.01 Ω-cm), in which eddy currents can be considerable. The effect of the eddy currents can be represented in the model in Fig. 2 by a reduced L_S. R_B and L_S also depend on the substrate thickness and whether the chip is mounted onto a metal plate in the package or onto a lossless substrate [5].

In the preferred configuration of a substrate with a high, but still conventional, resistivity such as 10 Ω-cm, the substrate potential can only be defined laterally spaced from the spiral coil, which is represented in Fig. 2 as a contact to the node in between C_{Ox} and R_B near the outer terminal. The substrate

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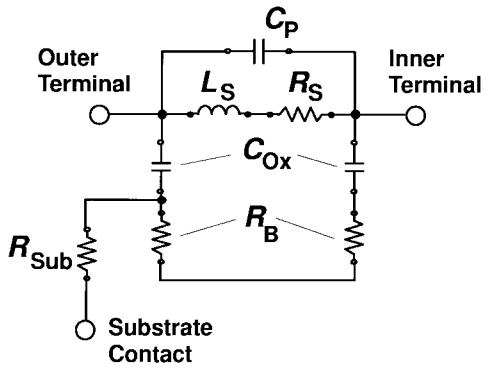


Fig. 2. Lumped-element model of a spiral inductor on silicon, including a possible substrate contact.

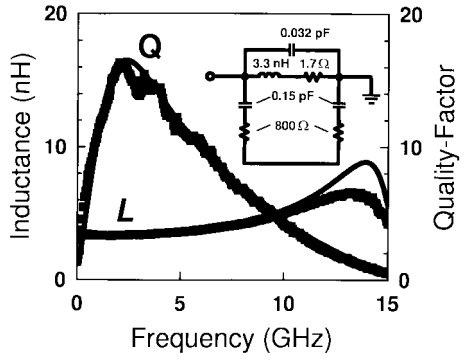


Fig. 3. Electrical characteristics and lumped-element model (inset) of a 3.3-nH Cu inductor (lines = modeling, markers = measurements).

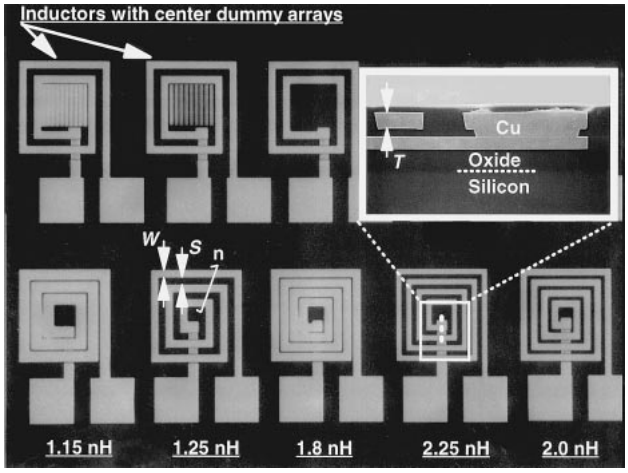


Fig. 4. Plan and cross-sectional (inset) views of Cu inductors. Also shown are inductors with metal dummy arrays in their center area.

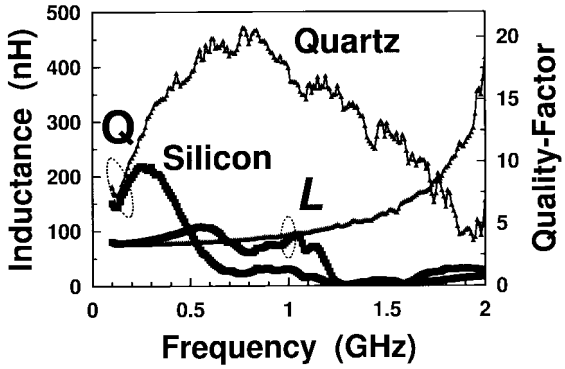


Fig. 5. Frequency dependence of inductance and quality factor of an 80-nH Cu inductor on silicon and on quartz substrates.

contact can be placed close to the inductor (small $R_{\rm Sub}$ in Fig. 2) or can be left floating by spacing any substrate contact away from the device (large $R_{\rm Sub}$ in Fig. 2). The effect of the substrate contact on the inductor characteristics will be explained in Section II-C. The Q develops a distinct maximum ($\rm Q_{max}$) at a frequency (f_0), which depends on the coil losses (R_S) and the substrate losses ($C_{\rm Ox}$ and R_B). For good parameter control and ease in circuit design, it is important that the inductance be constant near $f_0 (L \simeq L_S)$. This is achieved by using a minimum doping concentration under the inductor (i.e., a high value of R_B), so that self-resonance ($f_{\rm SR}$) occurs mainly via the small interwire capacitance C_P sufficiently beyond f_0 instead of via the comparably much larger $C_{\rm Ox}$, near f_0 (Fig. 3). The agreement of modeling and measurements results near f_0 are usually very good in spite of the simplicity of the model, as shown in Fig. 3.

From the typical frequency dependence of Q, as shown in Fig. 3, it is obvious that the optimization of a spiral inductor has to aim for a coordinated reduction of R_S and the substrate losses in R_B, determined by the total impedance of $C_{\rm Ox}$ and R_B, in order to arrive at the highest possible $\rm Q_{max}$ at f_0. The parasitics $C_{\rm Ox}$ and R_B are responsible for the falloff of Q beyond f_0, provided that f_0 is small. In mainstream silicon fabrication processes, one can take advantage of multilevel interconnects by looking for a tradeoff between the shunting of several metal layers in order to lower R_S and by omitting the lowest metal layers to reduce $C_{\rm Ox}$ (M1 omitted in Fig. 1). Further, the available blockout masks should be applied in the fabrication process to keep the doping level under the spiral coil at a minimum in order to maximize R_B [Fig. 1(b)]. This is a conservative approach since it does not require any alteration of the fabrication processes that are used in today's manufacturing lines. An innovative approach can lead to much higher $\rm Q_{max}$ values by introducing low-resistive metallization and low-loss substrates. Recent results of inductor optimization have benefited in particular from the introduction of copper (Cu) Damascene interconnect technology (Fig. 4), which leads to a reduced R_S and thus an increased $\rm Q_{max}$ at the currently relevant frequencies in comparison to aluminum (Al) interconnects. Figs. 3 and 5 show that this new interconnect technology enables Q values beyond ten even for very large inductances. It is also shown in Fig. 5 that the elimination of the substrate losses by using micromachining techniques ($C_{\rm Ox} = 0$, $R_B \rightarrow \infty$) in addition to the lower coil resistance leads to a further increase of $\rm Q_{max}$ at a higher f_0 ("quartz" versus "silicon" in Fig. 5). In this experiment, the substrate silicon was removed by using selective etching of the silicon, and the remaining thin-film structure was bonded onto a quartz substrate. The micromachined version of the Cu inductor in Fig. 3 had a $\rm Q_{max} \simeq 60$ at 6 GHz. The electrical characteristics of a 16-turn inductor with 80-nH inductance in Fig. 5 show that the Cu metallization already leads to $\rm Q_{max} > 10$ ("silicon"), but with

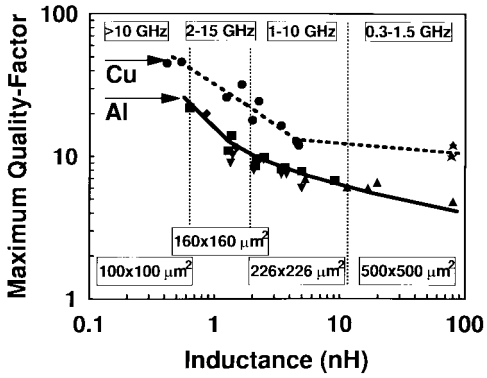


Fig. 6. Maximum quality factors versus inductances for Al and Cu inductors. The ranges of f_0, and of the inductor total areas, are listed as insets at the top and bottom, respectively.

the additional removal of the substrate losses, an additional twofold increase of Q_{max} and an elevation of f_0 become possible ("Quartz").

Fig. 6 shows that the $\sim 2\times$ lower resistivity and the $\sim 2\times$ greater conductor thickness [~ 4 μm versus ~ 2 μm (T in inset of Fig. 4)] of Cu compared to the Al process led to a 3–4$\times$ increased Q_{max} over the entire range of feasible inductance values. The figure also shows that f_0 is, to first order, set by the inductor area. It is further obvious from the results in Fig. 6 that large inductance values typically combine with comparably small Q's, while the opposite is the case for small inductances. That is mainly a result of the substrate losses: an increase of the number of turns in the spiral coil or an increase of the coil area results in an increased magnetic flux, and thus a high inductance value, but also in a proportionally higher series resistance. From that point of view, the Q should not be very different if one compares large to small inductances. Taking into account the RF current flow through the substrate, however, results in a comparably stronger degradation of Q for large inductance values, as observed in Fig. 6. Also, for the same total area—i.e., the same "footprint"—of the spiral coil, a small inductance value combines with a comparably larger Q [3]. Fortunately, in many RF building blocks, such as filters or impedance matching networks, the required inductance values are smaller at the higher frequencies, at which a comparably higher Q is needed.

B. Design for Minimum Inductor Area

The inductor size should be minimized, as inductors consume a large fraction of the circuit area [6]. This can first be achieved by choosing a minimum width of the coil conductor. For three Al test inductors with the same area (226×226 μm^2) and $n = 4$, we measured that Q_{max}, was the largest for $W = S = 12.5$ μm ($L = 2.5$ nH, $Q_{max} = 10$), Q_{max} was medium for $W = 16$ μm and $S = 10$ μm ($L = 2.15$ nH, $Q_{max} = 9.5$), and Q_{max} was the smallest for $W = 20$ μm and $S = 4$ μm ($L = 2.1$ nH, $Q_{max} = 8.6$), all at $f_0 = 4.5$ GHz [Fig. 7(a)]. (For the Cu process, those values were $L = 2.3$ nH, $Q_{max} = 22$ versus $L = 2.0$ nH, $Q_{max} = 15$ versus $L = 1.8$ nH, $Q_{max} = 10.5$.) Fig. 7(a) shows that the main reason for this difference in Q is likely caused by the skin effect in the

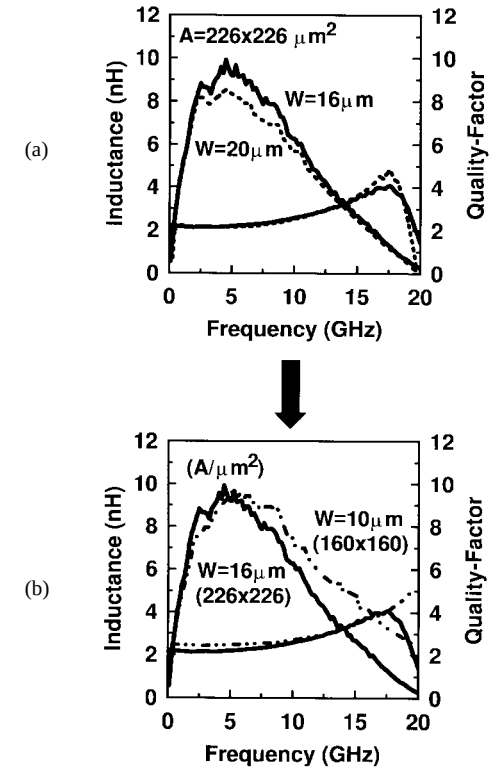
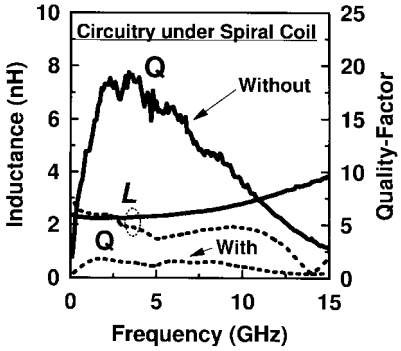


Fig. 7. Inductance and Q versus frequency of (a) inductors with two different widths but the same total area and (b) inductors with different total areas but similar electrical characteristics.

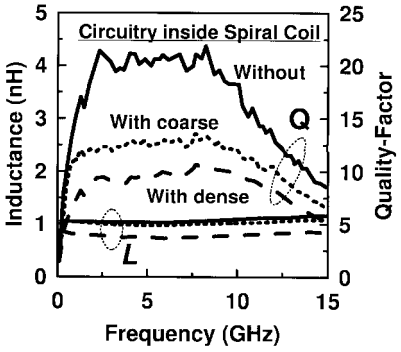
coil conductor layer, which leads to current's crowding to the edges of the conductor. The increase in conductor width from $W = 16$ μm to $W = 20$ μm does not lead to a significant reduction of the high-frequency resistance, as seen from the very similar increase of Q with frequency below f_0 in Fig. 7(a). The falloff of Q beyond f_0, however, occurs at lower frequencies for the wider conductor due to the larger C_{Ox} [2]. For those reasons, the width of the coil conductor should only be large enough to reduce the ohmic losses in balance with other losses in the inductor structure. An increase beyond this level will have detrimental effects on the inductor-Q.

Since $S = 4$ μm did provide a sufficiently high f_{SR} (20 GHz), the inductor could be fabricated with a minimum W and $S \simeq 4$ μm, reducing the area consumption significantly. Based on this conclusion, an Al inductor with $W = 10$ μm and $S = 3.5$ μm had $L = 2.45$ nH and $Q_{max} = 9.7$ at $f_0 = 5.3$ GHz, with a reduced area of 160×160 μm^2, a result that was very similar to that of the 2$\times$ larger inductor with an area of 225×225 μm^2 and with $W = 16$ μm [Fig. 7(b)]. The results certainly do not indicate a general design rule for the spiral coil layout, but they illustrate how effectively the inductor area can be minimized without sacrificing the electrical characteristics.

Chip area can also be conserved by constructing an inductor with two vertically stacked spiral coils instead of using one coil with an underpass contact [7]. An inductance of 7 nH and $Q_{max} = 13.6$ were achieved with two stacked Cu coils compared to $L = 4.5$ nH and $Q_{max} = 12.5$ for a single-coil Cu inductor, showing that a higher inductance value can be gained for a given area and a similar Q_{max}. The improvement,



(a)



(b)

Fig. 8. Frequency dependence of inductance and Q of inductors built at metal levels M5 and M6 over SRAM interconnects at M1–M3 or over silicon.

however, comes at the expense of f_0's being reduced from 2.2 to 1.8 GHz and $f_{\rm SR}$'s being lowered from 12.8 to 4.3 GHz, restricting the range of operating frequency.

Another *potential* way to conserve chip area is to build the inductors over circuitry or to place circuitry in the open center space of an inductor. To explore the first option, an inductor was built at the metal levels M5 and M6 over dense SRAM interconnects fabricated at M1–M3. The result in Fig. 8(a) showed that fabrication of inductors over circuitry was not a viable option to conserve chip area because $Q_{\max}$ was $\sim 4\times$ smaller and f_0 was $\sim 5\times$ lower compared to the case without the SRAM wiring. Hollow Cu inductors with two turns and with or without metal dummy features (not grounded) with different metal pitches in the center area (Fig. 4) were fabricated to investigate qualitatively the option of placing circuitry in the inductor's center space. While the structure with the free center area had $Q_{\max} = 34$, $Q_{\max} = 22$ was measured for the less dense dummy features, and with the dense dummy lines $Q_{\max}$ was 14 [Fig. 8(b)]. The inductance, however, changed by less than 5%, showing that devices can be added to the inductor's center area as long as the density is moderate, no closed wire loops are formed, and control of the Q is not critical.

C. Circuit Layout Issues

Besides the inductor-size optimization, the electromagnetic coupling between inductors can complicate the RF circuit design and layout. We investigated this issue by fabricating pairs of inductors (226×226 μm^2 area each) with different spacings, wired for two-port S-parameter testing (Fig. 9, inset). The inductor pairs were built over 10-Ω-cm silicon substrates. The insertion loss, which indicates the degree of coupling, was found to be 29 dB at 5 GHz if the two inductors were placed as close as possible (i.e., 236 μm center–center). The insertion loss was reduced with increasing inductor spacing, having a value close to that measured for the open contact pads near 500 μm. With the inductor of the second port shorted, we found that even for the minimum distance, an effect on L was not noticeable and Q was degraded by only $\sim$5%. If, however, the inductor pairs were built over p^+/p^- substrates, as typically used in CMOS technology, a considerable capacitive coupling between the ports would be observed, which would overshadow the electromagnetic cross-talk effects [8]. On 10-Ω-cm substrates, the inductor proximity effects were small enough not to restrict the RF circuit layout in most cases. If inductors are used in LNA's, however, where power levels can be extremely low, cross talk can become a serious issue, and adequate spacing of the LNA to the other circuitry and special isolation structures become necessary.

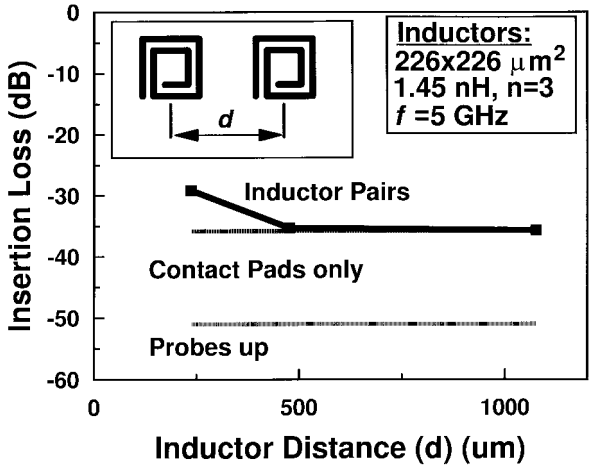


Fig. 9. Insertion loss as a function of the spacing of inductor pairs.

Another layout issue results from the poor definition of the substrate bias if the substrate resistivity is high. The substrate bias can only be defined by using a substrate contact outside of the spiral coil, which would be different in the regions underneath the coil as a result of the high substrate resistivity. In the model, the substrate contact can be represented by a resistor $R_{\rm Sub}$, as shown in Fig. 2. The effect of the contact on the electrical characteristics of the one- and two-port inductor configurations has been investigated, and the results were presented elsewhere [9]. In that work, the Q-factor in the one-port configuration (one terminal at ground) was found to increase by $\sim$40% at the expense of a reduced $f_{\rm SR}$ if a string of substrate contacts enclosing the spiral coil (halo substrate contact [9]) was applied. This tradeoff between $Q_{\max}$ and $f_{\rm SR}$ applies to silicon substrate contacts as well as to metal ground shield structures underneath the spiral coil [5]. The effect of a substrate contact is diminished, and $Q_{\max}$ is significantly reduced, if the silicon resistivity is low [9]. The effect of the substrate contact on the inductor characteristics is one example of the effect of the circuit layout on the device models in

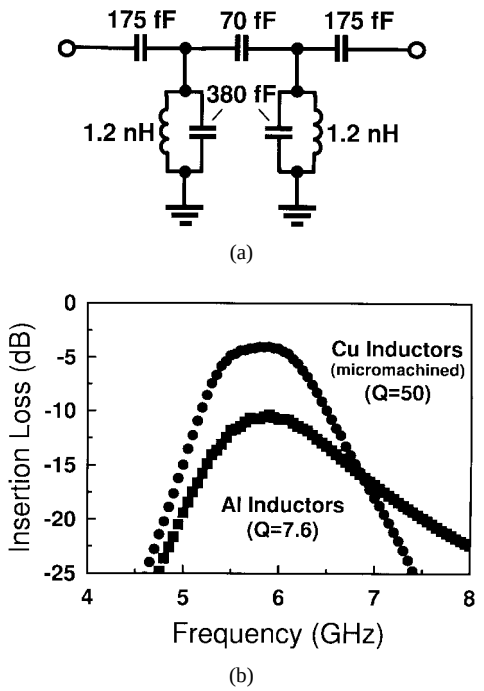


Fig. 10. (a) Schematics and (b) insertion loss of a coupled-resonator bandpass filter with use of either Al or micromachined Cu inductors. The 3-dB bandwidth relative to the center frequency (the Q of the filter) was set to ~5.4 by the capacitance ratio.

monolithic RF systems, indicating that the traditional concept of discrete device models may not be sufficient for RF circuit design on silicon.

III. Effect of Inductor-Q on RF Circuit Performance

The effect of the inductor-Q is very obvious in a bandpass filter (BPF) if high-Q metal-insulator-metal capacitors are used [Fig. 10(a)]. A first version of the BPF was built using Al inductors with a Q of 7.6. For the selected filter-Q of ~5.5, based on the ratio of the capacitance value in the inductance–capacitance resonator and of the capacitance that couples the resonators, an insertion loss of ~10 dB was measured [Fig. 10(b)]. The same BPF fabricated on a p^+/p^- substrate had ~15-dB insertion loss due to a reduced inductor-Q of 4.6 [not shown in Fig. 10(b)]. With micromachined Cu inductors ($Q \simeq 50$), the insertion loss improved to ~3.5 dB. Extrapolating from this result, we estimated that for this best case inductor implementation, a filter-Q of ten can be achieved with an insertion loss of ~5 dB. Those values may still not be sufficient in some RF designs, indicating that the integration of RF filters is one of the major challenges in the integration of monolithic RF transceivers.

As a second RF circuit, a 5.8-GHz LNA was fabricated by using a 0.5-μm SiGe-BiCMOS process[1] and was investigated by simulation [Fig. 11(a)]. In this circuit, a high inductor-Q allows one to design either for a reduced power consumption or a maximum figure of merit (FoM) [10], i.e., FoM = S21/(NF × P_{DC}) with the gain S21, the noise figure NF, and the power consumption P_{DC}. At $P_{DC} = 10$ mW and 2-V

[1]See IBM's SiGe technology home page at http://www.chips.ibm.com/sige/technology.html.

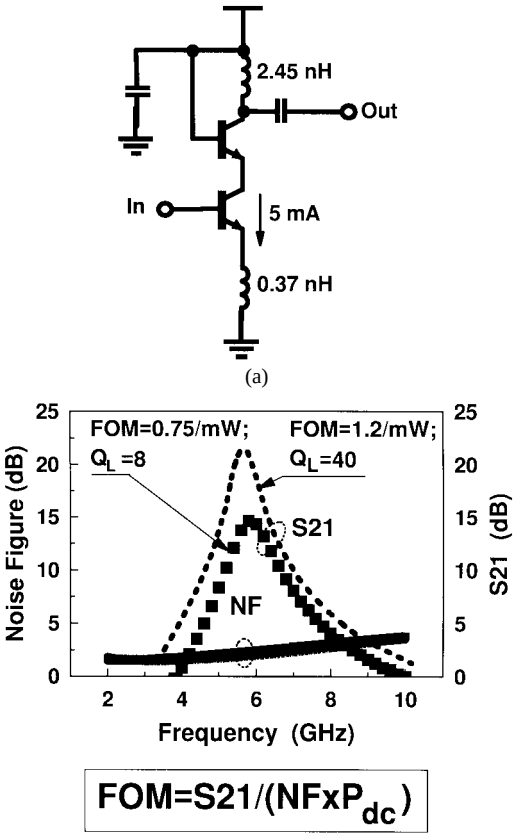


Fig. 11. (a) Schematic and (b) simulated and measured noise figure and insertion loss versus frequency of a 5.8-GHz LNA using inductors with Q = 8 or 40.

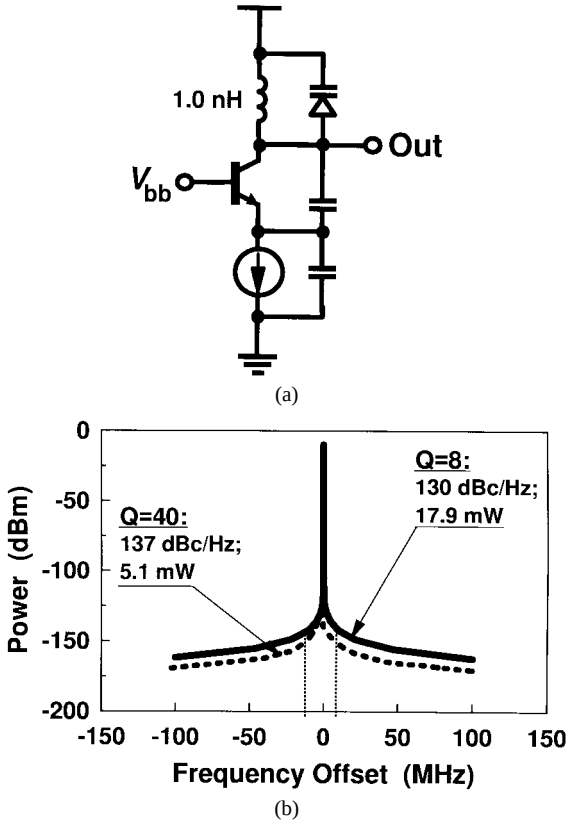


Fig. 12. (a) Schematic and (b) power versus frequency of a 5.0-GHz VCO using an inductor with Q = 8 or 40.

supply voltage, the FoM was found by simulation to improve from 0.75 to 1.2 mW^{-1} if an inductor-Q of 40 was used in place of $Q = 8$ [Fig. 11(b)]. For the *fabricated* LNA with an inductor-Q of ten, $\text{FoM} = 0.53\ \text{mW}^{-1}$ and $\text{NF} = 2.5$ dB were calculated and measured because the emitter inductor in the circuit was 0.23 nH instead of the desired 0.37 nH. With the correct value, $\text{FoM} \simeq 0.85\ \text{mW}^{-1}$ is expected.

Like the LNA, VCO's suffer especially from low-Q on-chip inductors. A 5.5-GHz SiGe VCO, based on a Colpitts oscillator [11], was investigated by simulation, assuming a 3-V supply voltage and a varactor-Q of 30 [Fig. 12(a)]. DC power reduction was identified as a key benefit of a high inductor-Q due to reduced gain requirements from the active circuitry. At 10-MHz offset, the phase noise was -130 dBc/Hz and the power was 17.9 mW for an inductor-Q of eight, and -137 dBc/Hz and 5.1 mW were found for $Q = 40$, showing that a $5\times$ increase in inductor-Q translates into a $3.5\times$ power savings and 7-dB better phase noise [Fig. 12(b)].

IV. Conclusions

In summary, integrated spiral inductors with inductances ranging from about 0.5 to 100 nH and Q's up to 40 can be provided for RF circuit design on silicon by using Al or Cu interconnect technologies. A low inductance value typically combines with a comparably high Q at a high f_0. A proper choice of conductor line width and, in some cases, utilization of the inductor coil's inner space for placement of circuitry can be instrumental to conserve chip area. In most cases, electromagnetic coupling between inductors is not an issue that affects the circuit layout. Important RF system building blocks, such as bandpass filters, LNA's, and VCO's, were found to benefit substantially from an improved inductor-Q.

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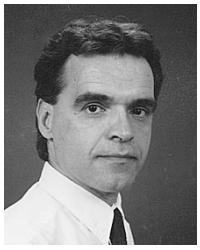
D. C. Edelstein received the B.S., M.S., and Ph.D. degrees in applied physics from Cornell University, Ithaca, NY, in 1982, 1986, and 1990, respectively.

His thesis work involved ultrafast quantum electronics studies in III–V semiconductors and the development of new femtosecond lasers and measurement techniques, most notably, the femtosecond optical parametric oscillator. He currently is a Research Staff Member in IBM's Research Division at the T. J. Watson Research Center, Yorktown Heights, NY. Since 1989, he has worked at IBM on advanced interconnect technology for VLSI/ULSI applications. This work has included process integration, advanced materials development, reliability, electrical performance modeling, interconnect scaling, dielectric, and high-speed measurements. In general, this work was all applied to research of copper on-chip interconnects. For the past five years, he has played a leadership role in the development and qualification of copper interconnects for IBM's ULSI CMOS programs.



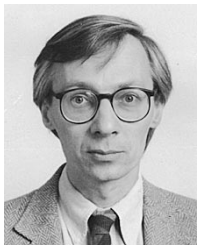
Mehmet Soyuer (S'79–M'88–SM'96) received the B.S. and M.S. degrees in electrical engineering from the Middle East Technical University, Ankara, Turkey, in 1976 and 1978, respectively, and the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1988.

He was a Teaching Associate and Research Assistant at the Middle East Technical University and at the University of California, Berkeley. He joined IBM's T. J. Watson Research Center, Yorktown Heights, NY, as a Research Staff Member in 1988. His research work involved high-frequency mixed-signal IC designs, in particular monolithic phase-locked-loop designs for clock and data recovery, clock multiplication, and frequency synthesis using silicon technologies. During 1995–1997, he was a Project Leader for Si and SiGe RF and microwave IC designs covering frequency bands of 1–20 GHz. In 1997, he became Manager of the Mixed-Signal Communications IC Design Group. He is the author of numerous articles in the areas of analog, mixed-signal, RF, microwave, and nonlinear electronic circuit design. He has received six U.S. patents. His research interests include high-speed integrated circuits, technologies, and systems for data communications.

Dr. Soyuer was a NATO Science Scholar from 1979 to 1982. He has received several IBM Research Division Awards.

H. A. Ainspan received the B.S. and M.S. degrees in electrical engineering from Columbia University, NY, in 1989 and 1991, respectively.

In 1989, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, where he has been involved in the design of mixed-signal and RF IC's for high-speed data links using Si and GaAs technologies. He is the coauthor of 22 external publications. He has received one patent.



Keith A. Jenkins (M'98) received the Ph.D. degree in physics from Columbia University, NY, for work done in experimental high energy physics.

He was with The Rockefeller University until 1983, when he joined the IBM Research Division at the T. J. Watson Research Center, Yorktown Heights, NY, where he first worked in Josephson technology. He later joined the Silicon Technology Department, where he worked in a variety of device and circuit subjects, including high-frequency measurement techniques, electron-beam circuit testing, radiation-device interactions, and low-temperature electronics. He presently is a Senior Engineer in the VLSI Systems Department. His current activities include evaluation of the performance of VLSI circuits, phase-locked loops and integrated silicon RF circuits, and research into the transient behavior of silicon-on-insulator FET's.