# A 115-mW, 0.5-$\mu$m CMOS GPS Receiver with Wide Dynamic-Range Active Filters

Derek K. Shaeffer, *Student Member, IEEE*, Arvin R. Shahani, S. S. Mohan, *Student Member, IEEE*,
Hirad Samavati, *Student Member, IEEE*, Hamid R. Rategh, *Student Member, IEEE*,
Maria del Mar Hershenson, *Student Member, IEEE*, Min Xu, *Student Member, IEEE*,
C. Patrick Yue, *Student Member, IEEE*, Daniel J. Eddleman, *Student Member, IEEE*, and Thomas H. Lee, *Member, IEEE*

*Abstract*— This paper presents a 115-mW Global Positioning System radio receiver that is implemented in a 0.5-$\mu$m CMOS technology. The receiver includes the complete analog signal path, comprising a low-noise amplifier, I-Q mixers, on-chip active filters, and 1-bit analog-digital converters. In addition, it includes a low-power phase-locked loop that synthesizes the first local oscillator. The receiver achieves a 2.8-dB noise figure (prelimiter), a 56-dB spurious-free dynamic range, and a 17-dB signal-to-noise ratio for a noncoherent digital back-end implementation when detecting a signal power of $-130$ dBm at the radio-frequency input.

*Index Terms*— Active filters, CMOS amplifiers, CMOS radio receiver, Global Positioning System, low-IF receiver, low-noise amplification, mixers, radio receiver, satellite communications, single-chip radio, wireless communications.

## I. INTRODUCTION

THE Global Positioning System (GPS) comprises 24 satellites in low earth orbit that continually broadcast their position and local time [1]. Through satellite range measurements, a terrestrial (or airborne) receiver can determine its absolute position and time as long as four satellites are within view.

Portable, consumer GPS receivers require solutions that are compact, cheap, and low power. To enable widespread proliferation of GPS capabilities into consumer products, an integrated receiver should minimize the number of off-chip components, particularly the number of expensive passive filters. These considerations motivate the present research into highly integrated CMOS solutions.

This paper describes the design and implementation of a 115-mW GPS receiver in a 0.5-$\mu$m CMOS process. Section II begins by describing the GPS system in more detail, along with two receiver architectures that typify modern integrated commercial receivers. Section III presents a new architecture that takes advantage of certain peculiar characteristics of the GPS signal spectrum to achieve a very high level of integration. The details of the receiver gain and frequency plan are also presented to motivate subsequent discussion of the signal-path building blocks in Section IV. This section includes a complete description of the signal-path design,

with special attention paid to the low-noise amplifier (LNA) and the on-chip active channel filter, two blocks that pose special design challenges. Section V presents experimental measurements of the receiver, and the paper concludes with a summary in Section VI.

## II. THE GLOBAL POSITIONING SYSTEM

The GPS satellites broadcast signals in two 20-MHz-wide bands: the L1 band, centered at 1.575 42 GHz, and the L2 band, centered at 1.2276 GHz. Both center frequencies are integer multiples of 10.23 MHz. Two direct-sequence spread-spectrum signals are broadcast in these two bands. These are known as the P code (or precision code) and the C/A code (or coarse acquisition code). The P code, which is intended for military use, is broadcast in *both* bands, while the C/A code is broadcast only in the L1 band. Note that the signal spectra of these two codes overlap.

At the antenna of a GPS receiver, the received signal power is typically $-130$ dBm. Because we are interested in the 2-MHz main lobe of the C/A code, the noise power is simply given by $kTB \approx -111$ dBm ($T = 290$ K). Hence, the received signal-to-noise ratio (SNR) at the antenna is about $-19$ dB.

The bit rate of the C/A code is only 50 bits/s. Thus, the processing gain is given by

$$G_P = 10 \log \left( \frac{T_b}{T_c} \right) = 43 \, \text{dB} \tag{1}$$

where $T_b$ is the bit period of the C/A code and $T_c$ is the chip period. So, with an antenna temperature of 290 K and an otherwise *noiseless* receiver, the postcorrelation SNR would be about 24 dB.

### A. Typical GPS Receiver Architectures

Two architectures are widely used in commercial GPS receivers today. These are illustrated in Fig. 1.

The first, and more widespread, is the dual-conversion architecture. In this approach, the GPS L1 band is translated to a moderate intermediate frequency (IF) of approximately 100–200 MHz where it is filtered off-chip before a second downconversion to a lower IF of around 1–10 MHz. There, the signal is filtered a second time before being amplified to a detectable level.

Fig. 1.   Typical GPS receiver architectures.



Fig. 2.   The GPS L1 band signal spectrum when downconverted to a 2-MHz intermediate frequency.
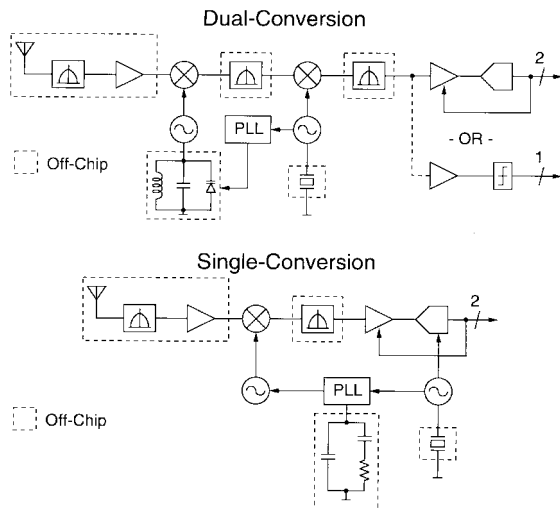
The second approach is the single-conversion architecture. As the name implies, only a single IF is used, generally with off-chip filtering. The IF is directly sampled and then converted to baseband in a subsequent digital step. An alternative approach subsamples the IF directly to baseband.

Both architectures have several attributes in common. First, an off-chip LNA or active antenna is generally postulated. This permits remote placement of the antenna from the receiver itself. It is also common to have several off-chip filters, including IF filters, phase-locked-loop (PLL) filters, and/or voltage-controlled oscillator (VCO) tanks. The first of these is generally difficult to integrate; however, the loop filter and tank circuitry are easily realized in integrated form. In addition, both architectures use coarse quantization (1–2 bits) in the signal path, with a modest automatic gain control being required in the 2-bit case. This is possible due to the large processing gain of the GPS signal combined with its less-than-unity received SNR. In fact, there is only a 3-dB loss associated with the use of one bit when compared to fine quantization. If two bits are used, the loss is only about 0.7 dB [2].

The clear disadvantage of these architectures is that a number of off-chip components are required. The key barrier to integration is the need for high-frequency ($\approx$100 MHz) off-chip IF filters.

### B. Opportunities for a Low-IF Architecture

One alternative would be to implement the receiver with a low-IF architecture. This architecture suffers from the well-documented problem of limited image rejection due to the need for stringent matching of in-phase (I) and quadrature (Q) channels [3], [4]. This limitation makes the low-IF approach unsuitable for many applications. However, when we examine the GPS signal spectrum, an opportunity emerges.

In consumer applications, where the C/A code main lobe is of primary concern, we can take advantage of the narrow main lobe and relatively wide channel in a low-IF implementation. This concept is illustrated in Fig. 2, where the L1 band has been downconverted to an intermediate frequency of 2 MHz.
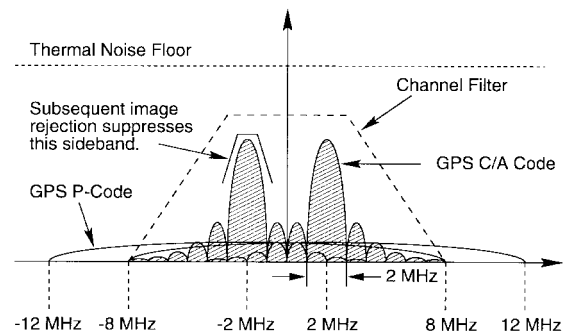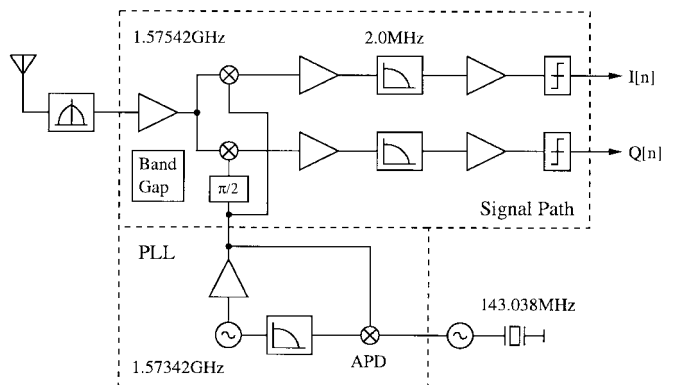


Fig. 3.   Block diagram of the CMOS GPS receiver.

This choice of IF causes the image signal to lie within the GPS band; thus, the receiver need only reject the *noise* of the unwanted sideband. The required rejection is only about 10 dB, which is easily attained with ordinary levels of component matching. In addition, the spectrum from 3 to 8 MHz can be used as a transition band for the active IF filter. This permits a reduction of the required filter order that will lead to improved dynamic range for a given filter power consumption.

These considerations make the low-IF architecture an attractive choice for a highly integrated GPS receiver.

### III. GPS RECEIVER ARCHITECTURE

A detailed block diagram of the CMOS receiver is shown in Fig. 3. The complete analog signal path is integrated, including the LNA, mixers, I and Q local oscillator (LO) drivers, IF amplifiers (IFA's), active filters, limiting amplifiers, and 1-bit analog-to-digital (A/D) converters. In addition, an on-chip PLL comprises a VCO, loop filter, charge, pump and phase detectors. The prescaler is eliminated in favor of *aperture phase detectors,* which only operate at the reference rate, thus reducing power consumption and switching noise [5].

Most of the receiver is biased with two on-chip bandgap references, with the exception of the LNA and the I and Q LO drivers. The LNA is biased with a separate self-referenced constant-$g_m$ bias network to eliminate any possible interaction with other blocks through parasitic bias coupling and to stabilize its gain and input match. Similarly, the I and Q drivers are biased by another constant-$g_m$ network for better regulation of the I and Q phase and amplitude.

TABLE I
RECEIVER GAIN PLAN

| Specification | LNA | Mix | IFA | Fltr | LA |
|---|---|---|---|---|---|
| Avail. Gain (dB) | 16 | −4 | 16 | −3 | 78 |
| Output Z (kΩ) | 0.4 | 0.4 | 2 | 1 | 60 |
| Noise Figure (dB) | 2.4 | 6 | 7 | 18 | 8 |
| OIP3 (dBm) | 7 | 5 | 10 | 0 | − |
| Total NF (dB) | 2.4 | 2.5 | 2.8 | 2.9 | 2.9 |
| ONoise (dBm) | −94 | −98 | −81 | −84 | − |
| *For $P_s = -53dBm$:* | | | | | |
| OIM3 (dBm) | −125 | −127 | −95 | −84 | − |
| SNR (dB) | 57 | 57 | 56 | 56 | − |
| SDR (dB) | 88 | 86 | 70 | 56 | − |

### A. Image-Noise Cancellation

As in the familiar Weaver single-sideband (SSB) modulator [6], the low-IF architecture depends on image cancellation to suppress the noise of the unwanted sideband. In cases where the image consists entirely of noise, the cancellation depends on the cross correlation of the noise signals in the two channels. However, the limiters in the signal path will reduce the cross correlation of the two noise processes, thereby drastically reducing the amount of cancellation. This leads one to ask whether an image-reject architecture makes sense when only 1-bit quantization is used in the I and Q signal paths.

When a low intermediate frequency is used, the noise powers in the signal band and the image band are equal. In this special case, it can be shown that the noise signals at the outputs of the limiters are uncorrelated so that subsequent downconversion and summation leads to a 3-dB SNR improvement compared to the SNR in each channel. Because this is the same improvement provided by an image-reject architecture with fine quantization, we conclude that, in this special case, the benefit of image-noise rejection can be achieved despite coarse quantization in the signal path.

### B. Receiver Gain Plan

Table I shows the distribution of gain and noise figure throughout the receiver. From this table, it is clear that the on-chip filter is the dynamic range limiting block because it has the largest noise figure and the smallest output third-order intercept point (OIP3). Thus, the system gain plan is driven primarily by the need to suppress the filter noise when referred to the system input. For this reason, the filter design problem will be examined in detail in Section IV.

At −53-dBm available source power, the third-order intermodulation (IM3) products at the filter output have a power that is approximately equal to the noise power in a 2-MHz bandwidth. This is the condition for peak spurious-free dynamic range (SFDR), which is about 56 dB.

## IV. SIGNAL PATH

The signal path of the receiver includes the LNA, mixers, LO drivers, IF amplifiers, active $G_m$-$C$ filters, and limiting amplifiers. In the following sections, each of these blocks is presented in some detail.
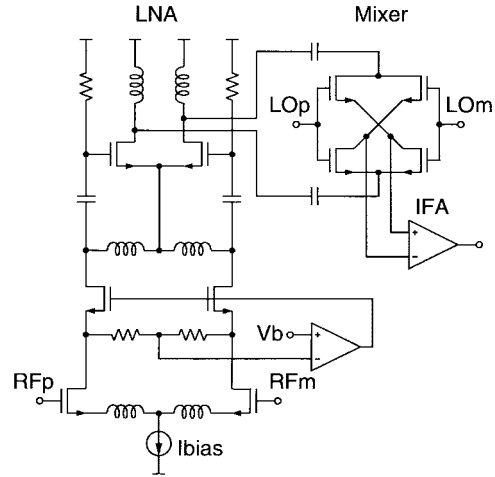


Fig. 4. Simplified schematic of the LNA and mixer. Some biasing details are omitted for clarity.

### A. Low-Noise Amplifier

Fig. 4 shows a simplified circuit schematic of the LNA and one of the two mixers [7]. The LNA uses a differential architecture to permit some rejection of common-mode interference from substrate and supply perturbations. The amplifier has two stages: a cascode input stage and a simple common-source output stage. Inductive interstage tuning leads to a bandpass characteristic for the amplifier and also allows bias current sharing. Using a cascode input stage minimizes interactions between the interstage tank and the input matching network, leading to improved stability. The input matching is performed off-chip.

To bias the first stage, a feedback amplifier servos the gate voltages of the cascode devices so that their source nodes have the desired common-mode voltage. This allows the amplifier to operate reliably on the low (2.5-V) supply voltage, despite supply, temperature, and process variations.

The second stage is ac coupled to the interstage tank, and its output is tuned for improved gain and to reject any low-frequency noise. AC coupling is also used between the LNA and mixer so that the gates of the mixer devices can be biased at the supply potential.

To optimize the noise figure of the LNA, it is important to model the *induced gate noise* of the input devices [8]–[12]. This noise source plays an important role in determining the fundamental limits of noise performance for CMOS LNA's but is not included in standard MOS models, with the exception of the Philips MOS9 model [13]. In addition, one should be careful to consider the effect of back-gate epitaxial noise [14], which can result in an apparent increase in $\gamma$, the coefficient of drain noise. Finally, $\gamma$ may also increase due to hot-electron effects [15].

To evaluate the magnitude of the epitaxial resistance noise, we can model the epitaxial layer as a resistance in series with the bulk terminal of the device [16]. There is a noise voltage associated with this resistance, which, together with the drain current noise of the device, produces a total drain current noise

of

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\{\gamma g_{d0} + g_{mb}^2 R_{\text{epi}}\} = 4kT\gamma_{\text{eff}} g_{d0} \qquad (2)$$

where

$$\gamma_{\text{eff}} \approx \gamma + \frac{g_{mb}^2 R_{\text{epi}}}{g_{d0}}. \qquad (3)$$

For the present 0.5-$\mu$m technology and the particular device size and layout geometry used in this LNA

$$0.09 \leq \frac{g_{mb}^2 R_{\text{epi}}}{g_{d0}} \leq 0.2. \qquad (4)$$

The lower bound uses the approach outlined in [16] for estimating $R_{\text{epi}}$, while the upper bound uses a much more conservative approach based on a trapezoidal approximation for the epitaxial spreading resistance [17], assuming that substrate contacts are distant from the device. With closely spaced substrate contacts, this number will be reduced even further. Thus, the epitaxial resistance is of secondary importance in this case.

From [3], the power-constrained minimum noise factor for a single field-effect transistor (FET) amplifier whose input is impedance matched to 50 $\Omega$ is approximately

$$F = 1 + 2.4\frac{\gamma}{\alpha}\left(\frac{f_0}{f_T}\right) \qquad (5)$$

where $\alpha = g_m/g_{d0}$. From simulation, we can determine approximate values for $f_T$ and $\alpha$. Assuming that $f_T = 8.45$ GHz, $\alpha = 0.85$, and $\gamma \approx 1.2$, we find that

$$F \approx 2.15 \text{ dB}. \qquad (6)$$

Note that this approximation only accounts for noise in the input devices. In this technology, the optimum occurs for an input device width of about 260 $\mu$m.

To simulate the noise figure of the entire LNA, one can include the influence of the induced gate noise current by modifying the BSIM-3 device model to include an additive noise *charge* in the formulation of the total gate charge. This noisy charge term has a power spectral density of

$$\frac{\overline{Q_g^2}}{\Delta f} = 4kT\delta\frac{C_{gs}^2}{5g_{d0}}. \qquad (7)$$

Including the induced gate noise, a simulation of the complete LNA yields a noise figure of 2.3 dB with the assumption of $\gamma = 1.2$. This number is very close to the measured result of 2.4 dB. Without the induced gate noise model, the simulated noise figure drops to 1.8 dB. The conclusion is that only a modest increase in $\gamma$ is required to reconcile simulations with measurements once the induced gate noise is included. In light of results reported in [12] and [15], it is plausible that this increase results from hot-electron effects. In addition, this $\gamma$ agrees well with independent noise measurements made on individual test devices [18].
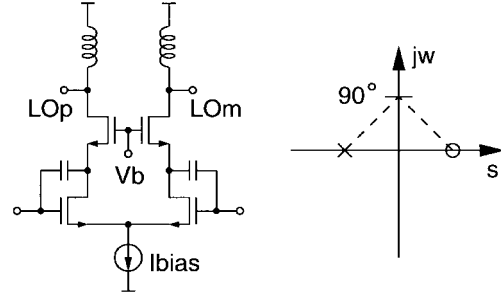


Fig. 5. Quadrature generation with the Miller capacitance.

### B. Mixer and LO Drivers

The LNA output is ac coupled to the input ports of the I and Q mixers. The LO driver for each mixer is a simple cascode amplifier that is inductively tuned to resonate with the input capacitance of the mixer LO port. Fig. 5 illustrates the quadrature version of the driver, which uses a Miller feedback capacitance to generate a transconductance of approximately

$$G_m \approx g_m\frac{1 - sC/g_m}{1 + sC/g_m}. \qquad (8)$$

This expression has a left half-plane (LHP) pole and a right half-plane (RHP) zero, resulting in an all-pass characteristic with a phase shift of 90° at $\omega = g_m/C$. To regulate the pole/zero frequency, a constant-$g_m$ bias source generates $I_{\text{bias}}$. This technique is suitable for use in this particular receiver due to the relaxed requirements for I/Q matching.

Although the mixer core consumes negligible power, the LO driver consumes power to drive the input capacitance of the mixer. This links the mixer noise figure to the LO-driver power consumption because the size of the switches influences both quantities.

The SSB noise factor of an ideal mixer (one that has no internal resistive losses) is given by

$$F = L_c \qquad (9)$$

where $L_c$ is the power-conversion loss of the mixer. Due to the linear time-variant nature of the mixer and its reactive IF termination, the conversion loss for a sinusoidal LO drive can be as low as 2.1 dB [7], which betters the classical result of 3.92 dB for a square-wave drive. Equation (9) can be modified to include the on-resistance of the mixer switches, which appears in series with the source resistance. Thus

$$F = L_c\left[1 + \frac{2\overline{R_m}}{R_s}\right] \qquad (10)$$

where $\overline{R_m}$ is the average on-resistance of a single switch.

To determine $\overline{R_m}$, we can assume that

$$\overline{R_m} = \frac{1}{\overline{g_{ds}}} = \frac{L}{\mu_{\text{eff}}C_{\text{ox}}W\overline{V_{od}}} \qquad (11)$$

where $\overline{V_{od}}$ is the average overdrive voltage supplied by the LO driver. If the LO driver has a tail current of $I_0$, the amplitude of one of the LO-driver outputs is given by

$$A_{\text{LO}} = \frac{\eta_I I_0 Q_L}{2\omega_{\text{LO}}C} \qquad (12)$$

where $Q_L$ is the $Q$ of the load inductors and $C$ is the total load capacitance on the LO-driver output. The parameter $\eta_I$ accounts for the fact that not all of the bias current is available at the output, due to parasitic losses in the LO driver itself. The capacitance $C$ comprises two switch gate capacitances plus the self-capacitance of the LO driver. If the driver has a certain self-resonant frequency $\omega_{SR}$, then the allowed switch capacitance is given by

$$C_{ox}WL = \frac{C}{2}\left[1 - \frac{\omega_{LO}^2}{\omega_{SR}^2}\right]. \tag{13}$$

Last, combining (10)–(13), we find an approximate formula for the mixer noise factor

$$F = L_c\left[1 + \frac{\omega_{LO}/\omega_C}{1 - (\omega_{LO}/\omega_{SR})^2}\right] \tag{14}$$

where $\omega_C$ is a critical frequency given by

$$\omega_C = \frac{R_s Q_L \mu_{eff} \eta_I I_0}{8\pi L^2} \tag{15}$$

beyond which the achievable noise figure begins to degrade rapidly. For a reasonable choice of self-resonant frequency, the noise figure is degraded by 3 dB when $\omega_{LO} = \omega_C$.

As a brief example, suppose that $\omega_{LO} = 10$ Grps, $\omega_{SR} = 30$ Grps, $R_s = 100\,\Omega$, $Q_L = 5$, $\mu_{eff} = 250\,\text{cm}^2/\text{Vs}$, $\eta_I = 0.75$, $I_0 = 4$ mA, and $L = 0.5\,\mu$m. Then $\omega_C \approx 6$ Grps and $F = 2.9L_c$, resulting in a loss of 4.6 dB over the ideal (internally lossless) mixer. If $R_s$ is increased to $400\,\Omega$, then $F = 1.5L_c$, which is a loss of 1.7 dB when compared to the ideal case.

Although this analysis is greatly simplified, the result yields some intuition about fundamental tradeoffs. In particular, the performance of this type of mixer should improve dramatically as technology scales due to the $1/L^2$ factor in $\omega_C$. For a given bias current, the noise performance is strongly influenced by the $Q_L$ of the spiral inductor loads. In addition, the driver self-resonant frequency should be no lower than about $3\omega_{LO}$ to avoid a sharp degradation in noise figure.

Notably absent from the result is any dependence on the switch size. As one reduces the switch size (and increases the load inductance value), the voltage swing at the gate of the switch increases so that the average on-resistance $\overline{R_m}$ remains roughly constant. So, the size of the switch is a relatively free parameter that can be optimized for maximum linearity.

## C. IF Amplifier

As shown in Fig. 4, the mixer drives the IFA directly. To minimize signal currents flowing in the mixer switches, the IFA should present a relatively high input impedance. In addition, the output impedance of the IFA should be well defined for use as a termination resistor for the active filter that follows. Last, the IFA should make efficient use of its bias current while providing a linear transfer characteristic.

Fig. 6 shows an amplifier that meets these requirements. Devices M1–M3 form a linearized voltage buffer that, through feedback action, causes a constant current $I_{bias}$ to flow from
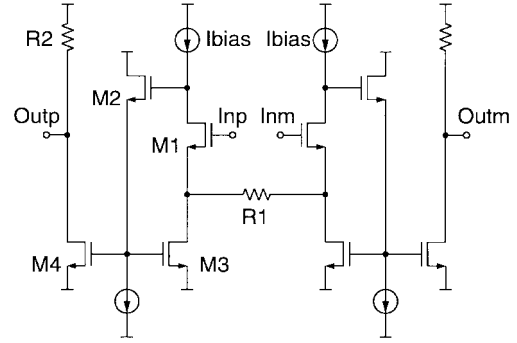


Fig. 6. Simplified schematic of the IFA. Some biasing details have been removed for clarity.
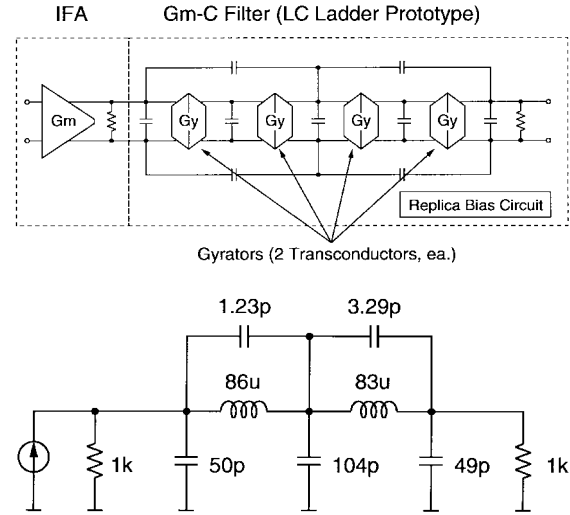


Fig. 7. Block diagram of the on-chip $G_m$-$C$ filter and its equivalent half-circuit.

drain to source in M1. Thus, the input voltage experiences a nearly constant level shift and is placed across the input resistor. This remains true for any input amplitude until the peak current flowing in the resistor is equal to $I_{bias}$. At this point, the feedback breaks down and the amplifier saturates.

Because the linear signal current must flow in device M3, one may mirror this current to the output load with device M4. The voltage gain is then given by

$$A_v = \frac{2MR_2}{R_1} \tag{16}$$

where $M$ is the current mirror gain.

## D. Active $G_m$-$C$ Filter

Fig. 7 illustrates a block diagram of the on-chip active filter and its equivalent half-circuit. The IFA drives the input of the filter directly, and the load resistors in the IFA output stage also terminate the filter input. Similarly, a real resistor provides the output termination, permitting a reduction in power consumption.

As shown in Table I, the filter is the dynamic range limiting block in the system. Previous studies have typically examined the dynamic range problem in active filters by assuming that
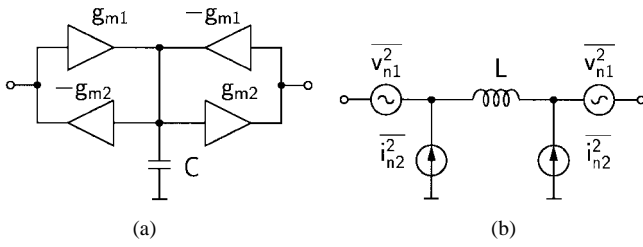
Fig. 8. A simple gyrator and its equivalent circuit with noise sources.

the largest acceptable signal voltage is a fixed parameter [19], often expressed as a simple fraction of the supply voltage [20]. One problem with such an approach is that it partly obscures the dependence of dynamic range on power consumption and choice of transconductor architecture. In previous work where the dynamic range is formulated explicitly without such assumptions, the analysis is typically limited to the specific architecture under discussion and is therefore lacking in generality [21], [22].

In the following discussion, we derive an expression for dynamic range with power consumption as an explicit constraint that is broadly applicable to $G_m$-$C$ filters, independent of transconductor architecture. In doing so, we will determine a transconductor figure of merit that can be applied to aid the selection of an architecture that maximizes the dynamic range of the filter for a given power consumption.

We begin by deriving the minimum noise figure of the filter.

*1) Noise Figure:* To determine the noise figure, we construct a noise model of each gyrator to understand how its internal amplifiers contribute noise to the system.

Fig. 8(a) shows an equivalent circuit of a simple gyrator that implements a floating inductor. Each transconductor generates thermal noise at its output that degrades the noise figure of the filter. By referring the transconductor noise sources to the external terminals of the gyrator, one arrives at the equivalent circuit shown in Fig. 8(b), where

$$L = \frac{C}{g_{m1}g_{m2}} \tag{17}$$

$$\frac{\overline{v_{n1}^2}}{\Delta f} = \frac{4kT\epsilon}{g_{m1}} \tag{18}$$

$$\frac{\overline{i_{n2}^2}}{\Delta f} = 4kT\epsilon g_{m2} \tag{19}$$

where $\epsilon > 1$ is a factor describing the amount of excess noise generated by a transconductor cell when compared to a real conductance of the same value.

At low frequencies, the inductor presents a short, and the voltage and current noise sources contributed by all of the gyrators in the filter sum together so that

$$\overline{v_n^2} = 2N_L\overline{v_{n1}^2} \tag{20}$$

$$\overline{i_n^2} = 2N_L\overline{i_{n2}^2} \tag{21}$$

where $N_L$ is the number of inductors in the filter. The corresponding minimum spot noise factor is

$$F_{\min} = 2\left[1 + 2\epsilon N_L\sqrt{\frac{g_{m2}}{g_{m1}}}\right] \approx 4\epsilon N_L\sqrt{\frac{g_{m2}}{g_{m1}}} \tag{22}$$

which occurs for an optimum terminating resistance of

$$R_t = \frac{1}{\sqrt{g_{m1}g_{m2}}}. \tag{23}$$

It is interesting to note that the minimum noise figure depends primarily on the order of the filter (through $N_L$) and on the architecture of the transconductor (through $\epsilon$). In fact, the minimum noise figure does not depend on the choice of $R_t$, implying that a fixed *power* gain is required preceding the filter to minimize its contribution to the system noise figure. Some improvement can be obtained by adjusting the relative magnitudes of $g_{m1}$ and $g_{m2}$, but this degree of freedom is constrained by the need for good distortion performance, as shown in the next section.

*2) Third-Order Intermodulation Distortion:* The analysis of distortion mechanisms in the filter is considerably more complex than the noise analysis of the previous section. In a communications system, however, certain simplifications can be made by restricting the analysis to IM3 distortion and ignoring the more difficult case of harmonic distortion. The virtue of IM3 distortion for analytical purposes is that the distortion products lie close to the fundamental products as long as the fundamental tones are close to one another. In what follows, we will assume that the fundamental frequencies are *arbitrarily* close to one another.

To begin, we adopt the assumption of small levels of distortion. With this assumption, we can model the distortion of a given transconductor in one of two ways. In the first method, we replace the nonlinear transconductor with a linear one and attribute the distortion products to an additive current source in the output of the transconductor. Alternatively, we can refer the output distortion current to the input as an equivalent input-referred distortion voltage. The distortion current and voltage have magnitudes given by

$$|v_d| = |V|\left(\frac{|V|}{V_{IP3}}\right)^2 \tag{24}$$

$$|i_d| = |I|\left(\frac{|I|}{I_{IP3}}\right)^2 \tag{25}$$

where

$$I_{IP3} = g_m V_{IP3} \tag{26}$$

is a measure of the third-order intercept point of the transconductor. The voltage and current intercept points are related by $g_m$ because they are extrapolated from low-amplitude distortion measurements, below the onset of gain compression.

Using these transconductor models in a simple gyrator results in the circuit shown in Fig. 9. This construction illustrates that it is important to consider both the voltage swing across the gyrator input $g_{m1}$ and the current swing through the feedback transconductor $g_{m2}$.

The greatest distortion will occur when the largest signal voltage appears across the gyrator. This condition corresponds to the resonance of the inductor with the other filter elements. Because the inductor voltage and current are in quadrature with one another, and because the fundamental frequencies are arbitrarily close to each other, we can assume that the resulting
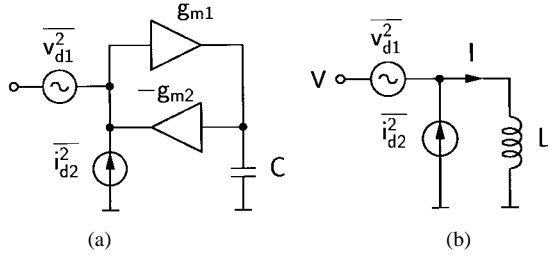
Fig. 9. Distortion models for a gyrator. (a) Full gyrator. (b) Equivalent circuit.
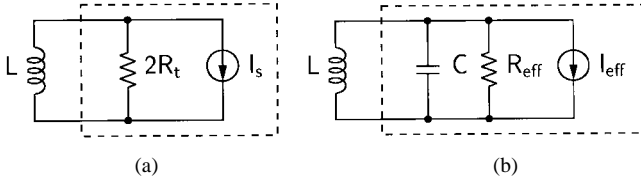


Fig. 10. Equivalent circuit presented by the filter network to the inductor (a) at dc and (b) at resonance.

distortion products are also in quadrature. Thus, the total distortion voltage appearing across the inductor at resonance is

$$|v_{dt}|^2 = |v_{d1}|^2 + (\omega_0 L Q_r)^2 |i_{d2}|^2 \qquad (27)$$

where $Q_r$ is the $Q$ of the resonance.

Noting that $|V| = \omega_0 L |I|$, and combining (23)–(27), we can express the total distortion voltage as

$$|v_{dt}|^2 = \frac{|V|^6}{V_{\text{IP3}}^4}\left[1 + \frac{Q_r^2}{Q_t^4}\left(\frac{g_{m1}}{g_{m2}}\right)^2\right] \qquad (28)$$

where we have defined

$$Q_t = \frac{\omega_0 L}{R_t} = \omega_0 L \sqrt{g_{m1} g_{m2}}. \qquad (29)$$

Finally, to relate the magnitude of the inductor voltage $|V|$ to the source voltage $V_s$, consider Fig. 10, which illustrates the equivalent circuits presented by the filter to the inductor at dc and at resonance. The filter acts as an impedance transforming network, causing the termination resistance $2R_t$ to be transformed to an effective parallel resistance $R_{\text{eff}}$ at resonance. The source current $I_s$ is also transformed to an effective current $I_{\text{eff}}$ by the inverse square root of the impedance transformation ratio. Thus

$$\frac{|V|}{V_s} = \frac{I_{\text{eff}}}{I_s}\frac{R_{\text{eff}}}{2R_t} = \sqrt{\frac{R_{\text{eff}}}{2R_t}} \qquad (30)$$

or, in terms of $Q_r$ and $Q_t$

$$\frac{|V|}{V_s} = \sqrt{\frac{Q_r Q_t}{2}}. \qquad (31)$$

By substituting (31) into (28), we can relate the distortion voltage to the source voltage

$$|v_{dt}|^2 = \frac{|V_s|^6}{V_{\text{IP3}}^4}\frac{Q_r^3 Q_t^3}{8}\left[1 + \frac{Q_r^2}{Q_t^4}\left(\frac{g_{m1}}{g_{m2}}\right)^2\right] = \frac{|V_s|^6}{V_{\text{IP3,eff}}^4} \qquad (32)$$

where $V_{\text{IP3,eff}}$ is the effective IIP3 voltage, referred to the input of the filter.

This analysis has, so far, assumed that only one inductor is present. With multiple inductors, the analysis becomes more complex. However, we can form a pessimistic bound by assuming that the $N_L$ inductors contribute equal amounts of distortion power. With this assumption, the IIP3 *available power* is

$$\text{IIP3} = \frac{V_{\text{IP3,eff}}^2}{8 R_t N_L^{1/2}}$$

$$\approx \frac{V_{\text{IP3}}^2}{R_t N_L^{1/2}(2 Q_r Q_t)^{3/2}\left[1 + \frac{Q_r^2}{Q_t^4}\left(\frac{g_{m1}}{g_{m2}}\right)^2\right]^{1/2}}. \qquad (33)$$

Although this expression is approximate, it yields some insight on how the IIP3 will depend on the relative magnitudes of various parameters. In particular, $N_L, Q_r$, and $Q_t$ are set by the desired filter characteristic and are thus relatively inflexible parameters. Also, note that reducing the impedance level of the filter will result in improved distortion because voltage levels are reduced for a given signal power. Finally, the ratio of $g_{m1}$ and $g_{m2}$ strongly influences the linearity because this ratio determines the current-handling capability of the active inductor.

In the next section, we will explore how to optimize the dynamic range of the filter, based on these results for noise figure and IIP3.

*3) Optimizing Dynamic Range:* The condition for minimum noise figure is expressed in (23) and determines the *product* of $g_{m1}$ and $g_{m2}$. The *ratio* of these transconductances is a free parameter that can be used to maximize dynamic range. The peak SFDR is the dynamic range for which IM3 distortion products and the in-band noise power are equal. In terms of $F$ and IIP3, we have

$$\text{SFDR} = \left[\frac{\text{IIP3}}{FktB}\right]^{2/3}. \qquad (34)$$

Using (22) and (33), we can formulate the SFDR as

$$\text{SFDR}$$
$$= \left[\frac{V_{\text{IP3}}^2}{4kTB\epsilon(2N_L Q_r Q_t)^{3/2}R_t\left[\frac{g_{m2}}{g_{m1}} + \frac{Q_r^2}{Q_t^4}\frac{g_{m1}}{g_{m2}}\right]^{1/2}}\right]^{2/3}. \qquad (35)$$

Maximizing this expression is equivalent to minimizing

$$R_t\left[\frac{g_{m2}}{g_{m1}} + \frac{Q_r^2}{Q_t^4}\frac{g_{m1}}{g_{m2}}\right]^{1/2}. \qquad (36)$$

The condition for minimum noise figure is expressed in (23). Substituting this for $R_t$ in (36) yields

$$\left[\frac{1}{g_{m1}^2} + \frac{1}{g_{m2}^2}\frac{Q_r^2}{Q_t^4}\right]^{1/2}. \qquad (37)$$

We can minimize (37) subject to a constant-power constraint if we set

$$g_{m1} + g_{m2} = \frac{\beta P_D}{2N_L} = \beta\overline{P_D} \qquad (38)$$

where $\overline{P_D}$ is the power dissipation per gyrator and $\beta$ is the transconductance per unit power dissipated in the gyrator. Taking the derivative of (37) and setting it equal to zero yields the condition for maximizing dynamic range, which is that

$$\frac{g_{m2}}{g_{m1}} = \frac{Q_r^{2/3}}{Q_t^{4/3}}. \tag{39}$$

So, in general, it is *not* optimal to have $g_{m1} = g_{m2}$. This is particularly true of high-$Q$ filters, which tend to have a larger optimum ratio of the two transconductances due to larger circulating currents in the inductors at resonance.

Combining (38) and (39) with (35), we can express the peak SFDR as

$$\text{SFDR}_{\text{pk}} = \frac{\left[\dfrac{\overline{P_D}}{4kTB}\dfrac{\beta V_{\text{IP3}}^2}{\epsilon}\right]^{2/3}}{2N_L Q_r Q_t \left[1 + \dfrac{Q_r^{2/3}}{Q_t^{4/3}}\right]}. \tag{40}$$

This expression for dynamic range deserves close attention. The denominator is determined entirely by the *filter* architecture. In particular, the higher the $Q$ and the greater the number of inductors, the lower the dynamic range will be, assuming all other factors are held constant. So, architectures that relax the required filter order and $Q$ will benefit from increased dynamic range. The numerator of the expression is determined by the *transconductor* architecture, including $\overline{P_D}$, the power per gyrator. Note that expending more power increases the dynamic range by lowering the optimum terminating impedance. The form of the numerator suggests that a good figure of merit for a transconductor architecture is

$$\Gamma_m = \frac{\beta V_{\text{IP3}}^2}{\epsilon} \tag{41}$$

which is a unitless quantity because $\beta$ has units of $\text{V}^{-2}$. Hence, it is important to select a transconductor architecture that is power-efficient ($\beta$), linear ($V_{\text{IP3}}$), and low noise ($\epsilon$). Choosing such an architecture forms the subject of the next section.

*4) Power-Efficient Transconductors:* The gyrator transconductor architecture sets the overall performance of the filter. To implement a low-power filter, it is essential to select a transconductor architecture that is linear and that maximizes the $G_m/I_{\text{bias}}$ ratio, thereby maximizing $\beta$.

Class-A transconductors are fundamentally limited in this regard because the linear input voltage range $V_x$ can only be increased at the expense of $G_m$ if the power consumption is fixed. That is

$$G_m V_x \propto I_{\text{bias}}. \tag{42}$$

This tradeoff between $G_m$ and linearity makes class-A techniques unattractive.

An alternative, class-AB approach takes advantage of the square-law behavior of CMOS devices. If a differential amplifier is constructed out of two square-law amplifiers, the resulting differential gain is *linear*. For two such transconductors with differential input $\Delta v$

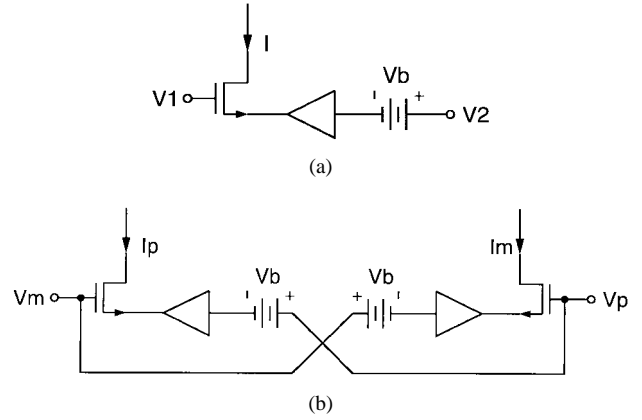$$\beta_0(\Delta v + V_b)^2 - \beta_0(-\Delta v + V_b)^2 = 4\beta_0 V_b \Delta v. \tag{43}$$



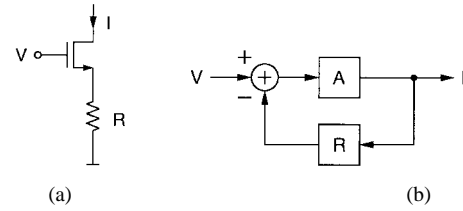Fig. 11.  A class-AB transconductor. (a) Square-law prototype. (b) Linear prototype.



Fig. 12.  Mobility degradation modeled as series feedback. (a) Equivalent circuit. (b) System view.

Thus, the output is linearly proportional to the input.

To implement a square-law transconductance characteristic, one might consider the circuit of Fig. 11(a). In this circuit, the input voltage $V_1 - V_2$ is level shifted and placed across an NMOS device. To the extent that the NMOS follows a square law, the overall transconductor is square law. Using two of these transconductors as shown in Fig. 11(b), we can construct a linear differential transconductor. However, due to velocity saturation and vertical field mobility degradation, the NMOS will exhibit subsquare-law behavior. Velocity saturation can be mitigated by adopting a longer channel length, but vertical field mobility degradation depends on the thickness of the gate oxide, which is not a flexible parameter.

To understand the role of mobility degradation, one can model this effect with an ideal square-law device and simple series feedback, as shown in Fig. 12. If the mobility-degraded current is given by

$$I = \frac{\beta_0(V_{gs} - V_T)^2}{1 + \theta(V_{gs} - V_T)} \tag{44}$$

then one may model the degradation as the result of an *ideal* square-law device degenerated by a resistor of value

$$R = \frac{\theta}{2\beta_0}. \tag{45}$$

In the equivalent system model, the resistor appears as a negative feedback term, with the forward path A representing the desired squaring operation

$$I = \beta_0(V)^2. \tag{46}$$

When viewed from this perspective, it is clear that the remedy to mobility degradation is positive feedback, as shown
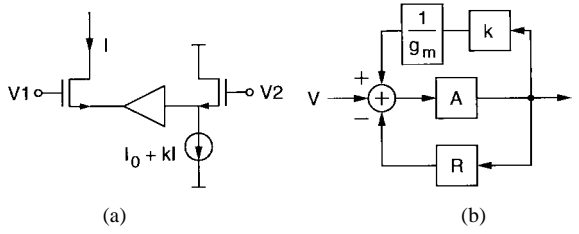
Fig. 13. Canceling mobility degradation with positive feedback. (a) Modified transconductance cell. (b) System view.
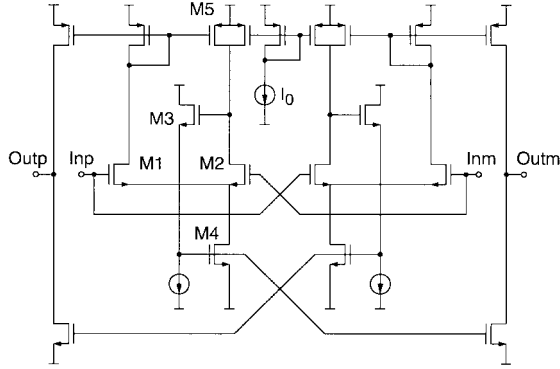


Fig. 14. A linearized class-AB transconductor.



Fig. 15. Normalized transconductance characteristic, with and without positive feedback.

in Fig. 13. The proper amount of positive feedback can be selected by setting

$$k \approx g_m R = \frac{g_m \theta}{2\beta_0} = \theta V_{od} \left[ \frac{1 + \theta V_{od}/2}{(1 + \theta V_{od})^2} \right] \qquad (47)$$

where $V_{od} = V_{gs} - V_T$ with the inputs balanced. In reality, $k$ must be adjusted to compensate for second-order effects due to other nonidealities, such as channel-length modulation and body effect. Thus, (47) is only approximate. Note that a practical value of $k$ for this process is about 0.2. This small amount of positive feedback does not pose a stability threat.

In contrast to linearization by negative feedback in the class-A case, this approach linearizes by *positive* feedback, increasing both $G_m$ and the linear input range with negligible additional static power consumption.

A transconductor that applies these concepts is illustrated in Fig. 14. The voltage buffer of Fig. 13 is implemented with M2–M4, which form a linearized, level-shifting buffer, similar to that used in the IFA. Thus, M1 is the transconducting NMOS device, and M5 implements the positive feedback path by sampling the output current of M1 and adjusting the bias current to M2.

Fig. 15 demonstrates the benefits of positive feedback in this architecture. The lower curve shows the nonlinearity in $G_m$ when positive feedback is omitted. The bowing is nearly eliminated with the addition of device M5 and is relatively insensitive to reasonable variation in the length of that device.

Eight of these transconductors are used in the on-chip filter, which has a total power consumption of 9.7 mW and a differential terminating impedance of 2 k$\Omega$. The filter achieves a peak SFDR of greater than 60 dB.
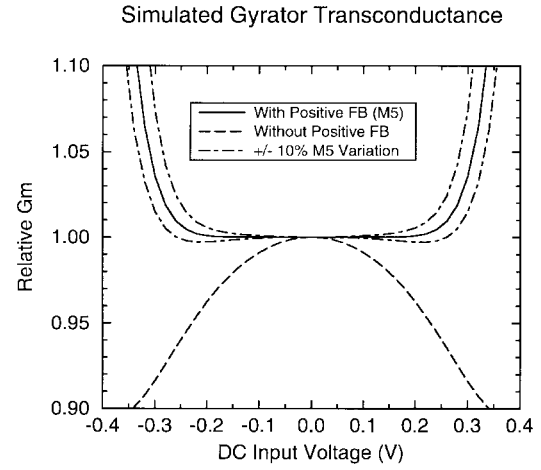
### E. Limiting Amplifier and Comparator

The final two stages in the receiver signal path are the limiting amplifier and output comparator. The limiting amplifier is a five-stage amplifier that uses simple differential pairs. The stages are ac coupled to one another to prevent the propagation of dc offsets through the chain, with the exception of the very first stage, which is dc coupled to the filter output. With a 2-MHz IF frequency, the lower pole of the ac coupling should be somewhat below 1 MHz to prevent distortion of the C/A code main lobe. The limiting amplifier nominally provides 96 dB of voltage gain and 78 dB of power gain, which is more than sufficient to amplify system thermal noise up to a detectable level for the comparator that follows.

The comparator is a standard Yukawa latch [23] that accepts a single clock supplied from off-chip and that is driven directly by the output stage of the limiting amplifier. The comparator is clocked at about 16 MHz, yielding an oversampling factor of approximately two.

Note that although the vast majority of system gain occurs in these two blocks, they occupy less than on-eighth of the total die area of the chip. No signs of instability were observed, despite the large gain.

## V. EXPERIMENTAL RESULTS

The GPS receiver is implemented in a 0.5-$\mu$m CMOS process, and a die micrograph is shown in Fig. 16. The layout consumes 11.2 mm$^2$ and uses 16 spiral inductors in the RF and PLL sections, with inductance values of 1.2–14.3 nH and quality factors of 4.7–6.7. These spirals use patterned ground shields for improved quality factor and reduced cross talk between spirals [24]. The inductor simulation model used in this work is described in [25]. Based on measurements of several of the inductors in this receiver, the model is typically accurate to within 5%.

The entire signal path of the chip is differential, and careful attention is paid to symmetry throughout the layout. The I and Q channels are also symmetrically placed about the horizontal centerline of the chip. To reduce interaction between the LNA and PLL circuitry, separate supplies are run from the outer
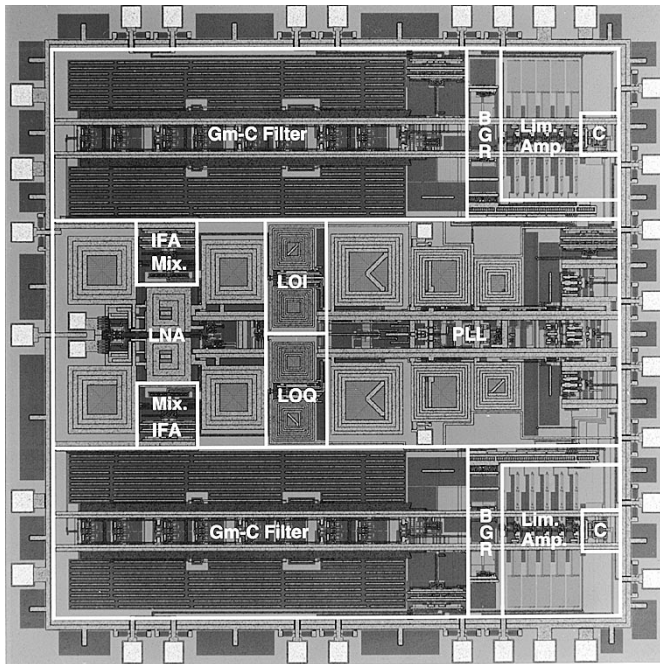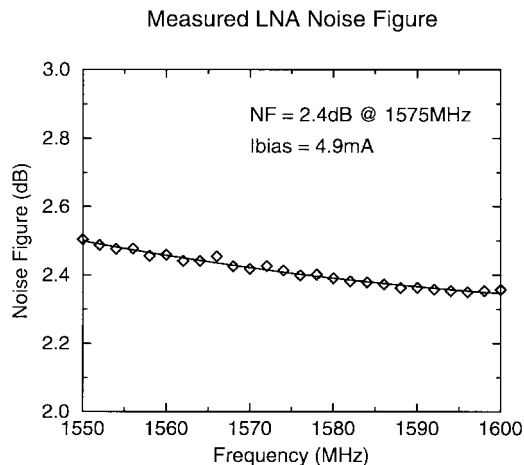
Fig. 16. Die micrograph of the GPS receiver.

Fig. 18. Measured signal-path frequency response.

Fig. 17. Measured LNA noise figure.

Fig. 19. Results of a two-tone IM3 test.

supply ring, where extensive on-chip capacitive bypassing is used (about 1.2 nF, in all).

The LNA is also laid out as a separate test structure so that its noise figure can be independently measured. The result is shown in Fig. 17. The LNA has a noise figure of 2.4 dB at 1.575 GHz with 4.9 mA of bias current in the amplifier core, suggesting that an equivalent single-ended amplifier would consume 2.45 mA of bias current. This measurement is made for an input return loss of better than 20 dB.

Several test points exist for measuring intermediate points along the signal path. In particular, an output buffer amplifier permits signa-path measurements after the filter and before the limiting amplifier. Much of the signal-path data are based on measurements at this test point.

Fig. 18 shows the signal-path frequency response as measured before the limiting amplifier. The simulated and measured responses agree very well. The filter exhibits about 77
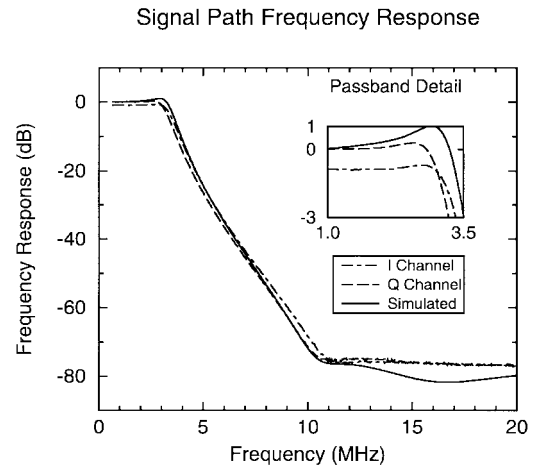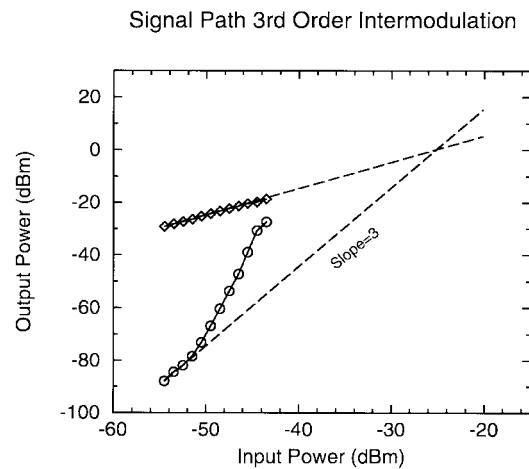
dB of stopband rejection and less than 1 dB of passband peaking. Mismatch in I and Q amplitudes is observed, some of which is attributed to board components. Unfortunately, a direct measurement of the on-chip I and Q matching is not possible, but the success or failure of image rejection can be ascertained by measuring the postdetection SNR, as will be shown shortly.

A spot noise figure of 2.8 dB is also measured at the output of the filter. This number is in good agreement with the predicted value of 2.9 dB from design simulations of the individual receiver blocks. The use of a 1-bit quantizer causes an SNR degradation that can be accounted for by increasing the effective noise figure to 4.5 dB.

To determine the linearity of the system, two tests are performed: a two-tone IM3 test and a 1-dB blocking desensitization test. These are shown in Figs. 19 and 20.

For the IM3 test, two in-band test tones are applied to the system at 1.575 62 and 1.575 42 GHz. Note that the classical behavior of the IM3 products breaks down above an available source power of $-51$ dBm. The subsequent rise in distortion may be attributed to the rapid increase in $G_m$ observable in the filter transconductor characteristic of Fig. 15 when the input amplitude exceeds a certain value. Because the received
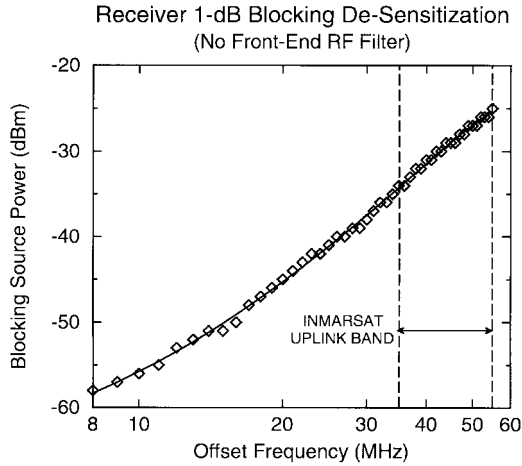
## Receiver 1-dB Blocking De-Sensitization
### (No Front-End RF Filter)



Fig. 20.   Measured 1-dB blocking desensitization point.

## Receiver Output Spectrum
### (Pre-Correlation)



Fig. 21.   FFT of the I channel output bit sequence.

signal power in the GPS system is very low, an extrapolation from low source powers is most relevant, yielding a $-25$-dBm input-referred IP3. This number is set almost entirely by distortion in the active filter.

A more relevant performance measure for this system is the 1-dB blocking point. In Fig. 20, a single out-of-band blocker is applied to the system, and its power is increased until a 1-dB reduction in the in-band SNR is observed. The band of frequencies that presents the greatest blocking threat is the INMARSAT uplink band, positioned at an offset of 35–55 MHz from the GPS center frequency of 1.575 GHz. At the lower edge of this band, the receiver has a 1-dB blocking point of $-35$-dBm available source power. Note that no external RF filtering is used in making this measurement. With a reasonable filter, this number would improve by 15–20 dB in the final system. It is believed that the blocking performance of the receiver is set by the VCO phase noise, estimated to be about $-135$ dBc/Hz at 35-MHz offset.

With the signal path and PLL verified separately, the full receiver is finally tested with a simulated GPS signal applied to the input at $-130$-dBm available source power. The 1-bit digital output stream is captured for the I and Q channels and digitally downconverted using a *noncoherent* back end to reduce the computational complexity. The use of a noncoherent back end causes an additional SNR degradation that elevates the effective noise figure to about 6.7 dB.

A fast Fourier transform (FFT) of the I channel is shown in Fig. 21. Despite the decorrelating effects of the limiter, the filter characteristic is still visible as an increase in the noise floor from 1 to 3 MHz. The spectrum is free of spurs, with the exception of a single spur attributable to one of the bench-top references used for the PLL.

The downconverted bit sequences are correlated with a reference copy of the GPS spreading code, and the resulting cross correlation as a function of code phase is plotted in Fig. 22. By comparing the magnitude of the correlation peak with the variance of the off-peak cross correlation, one concludes that the output SNR is about 17 dB. Recalling that a received SNR of $-19$ dB is expected, with a processing gain of 43 dB and
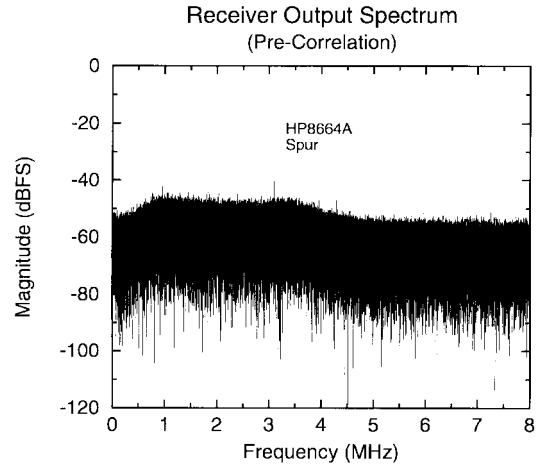
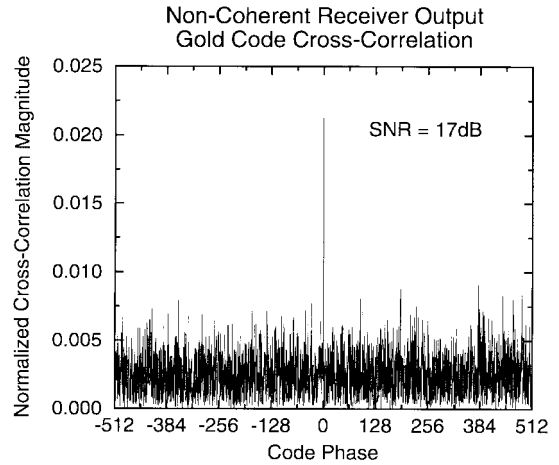## Non-Coherent Receiver Output
### Gold Code Cross-Correlation



Fig. 22.   Cross correlation at the receiver output.

an effective noise figure of 6.7 dB, we expect

$$SNR = -19\,\text{dB} + 43\,\text{dB} - 6.7\,\text{dB} = 17.3\,\text{dB} \qquad (48)$$

which agrees very well with the measured result of 17 dB. The conclusion is that the I/Q matching in the system is sufficient for effective cancellation of the image noise.

Table II summarizes the receiver performance.

### VI. SUMMARY AND CONCLUSIONS

In summary, this paper describes the implementation of a complete CMOS GPS receiver that includes all necessary active blocks in the RF and analog signal path, plus a PLL for LO synthesis. The signal path successfully applies the low-IF architecture by exploiting details of the GPS signal structure to permit a reduction in the I/Q matching requirements and a relaxation of the channel filtering problem. Optimization procedures have been described for designing the active filter, which is the dynamic-range limiting block in the signal path.

The final system consumes 115 mW from a 2.5-V power supply and occupies 11.2 mm$^2$ of die area in a 0.5-$\mu$m CMOS process. It is capable of detecting a $-130$-dBm GPS signal with a noncoherent back-end SNR of 17 dB.

TABLE II
MEASURED GPS RECEIVER PERFORMANCE

| *Signal Path Performance* | |
|---|---|
| LNA Noise Figure | 2.4dB |
| LNA S11 | −20dB |
| Coherent Receiver NF | 2.8dB |
| IIP3 (Filter-limited) | −25dBm @ −51dBm $P_s$ |
| Peak SFDR | 56dB |
| Filter Cutoff Frequency | 3.5MHz |
| Filter Passband Peaking | ≤ 1dB |
| Filter Stopband Attenuation | ≥ 52dB @ 8MHz |
| | ≥ 68dB @ 10MHz |
| Pre-Filter Power Gain | 28dB |
| Pre-Filter Voltage Gain | 41dB |
| Total Power Gain | ≈ 103dB |
| Total Voltage Gain | ≈ 131dB |
| Non-Coherent Output SNR | 17dB |
| LO Leakage @ LNA Input | < −72dBm |
| | |
| *Power Dissipation* | |
| Signal Path | 79mW |
| PLL / VCO | 36mW |
| Supply Voltage | 2.5V |
| | |
| *Implementation* | |
| Die Area | $11.2mm^2$ |
| Technology | 0.5-$\mu$m CMOS |

## ACKNOWLEDGMENT

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**Derek K. Shaeffer** (S'98) received the B.S. degree from the University of Southern California, Los Angeles, in 1993 and the M.S. degree from Stanford University, Stanford, CA, in 1995 where he is currently pursuing the Ph.D. degree.

From 1992 to 1997, he was with Tektronix, Inc. Beaverton, OR, where he designed A/D converter and communications circuits in CMOS and bipolar technologies. His current research interests are in CMOS and bipolar implementations of low-noise, high-linearity wireless communications receivers.

**Arvin R. Shahani**, for a photograph and biography, see this issue, p. 2041.

**S. S. Mohan** (S'98) received the B.S. and M.S. degrees in electrical engineering from Stanford University, Stanford, CA, in 1992 and 1993, respectively, where he currently is pursuing the Ph.D. degree.

During the summers of 1992 and 1993, he was with Acuson, Inc., characterizing ultrasound transducers for medical applications. At Stanford, he explores radio-frequency integrated-circuit design in CMOS technologies. His thesis focuses on the design and optimization of on-chip spiral inductors and transformers for both broadband and narrowband applications. He has been a Teaching Assistant in many undergraduate and graduate lecture and laboratory classes.

Mr. Mohan received a graduate fellowship from IBM in 1996.

**Hirad Samavati** (S'98) for a photograph and biography, see this issue, p. 2041.
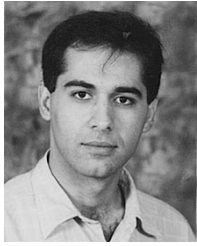
**Hamid R. Rategh** (S'98) was born in Shiraz, Iran, in 1972. He received the B.S. in electrical engineering from Sharif University of Technology, Iran, in 1994. He received the M.S. degree in biomedical engineering from Case Western Reserve University, Cleveland, OH, in 1996. He currently is pursuing the Ph.D. degree in the electrical engineering department at Stanford University, Stanford, CA.

During the summer of 1997, he was with Rockwell Semiconductor System, Newport Beach, CA, where he was involved in the design of a CMOS dual-band, GSM/DCS1800, direct-conversion transceiver. His current research interests are in low-power RF integrated-circuit designs for wireless applications.

**Maria del Mar Hershenson** (S'98) was born in Barcelona, Spain. She received the B.S.E.E. degree from the Universidad Pontificia de Comillas, Madrid, Spain, in 1995 and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, in 1997, where she currently is pursuing the Ph.D. degree in electrical engineering.

In 1994, she was an Intern with Linear Technology Corporation, Milpitas, CA, where she worked on low-power voltage regulators. Her research interests are RF power amplifiers and convex optimization techniques applied to the automated design of analog integrated circuits.

Ms. Hershenson received a graduate fellowship from IBM in 1998.

**Min Xu** (S'97) received the B.S. degree in physics from the University of Science and Technology of China in 1994 and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, in 1997, where she currently is pursuing the Ph.D. degree in the Department of Electrical Engineering.

Her research interests include substrate noise in mixed-signal circuits.
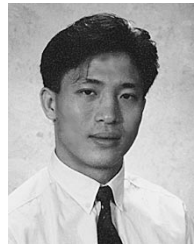
**C. Patrick Yue** (S'93) received the B.S. degree in electrical engineering (with highest honor) from the University of Texas at Austin in 1992 and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1994 and 1998, respectively.

His present research interests include design and characterization of RF passive components and interconnects at high frequencies.

Dr. Yue is a member of Tau Beta Pi.

**Daniel J. Eddleman** (S'98) received the B.S. degrees in electrical engineering and computer engineering from the University of California (UC), Davis, in 1995 and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, in 1998.

During the summers of 1994–1996, he was with the Telemetry Department at Sandia National Laboratories, Livermore, CA. In the summer of 1997, he was with Hewlett-Packard Co.'s Integrated Circuits Business Division, Palo Alto, CA. Currently, he is with Linear Technology Co., Milpitas, CA.

Mr. Eddleman received a UC Regents Scholarship at UC Davis and while at Stanford University was supported by the Solid State Industrial Affiliates Program.

**Thomas H. Lee** (S'87–M'87), for a photograph and biography, see this issue, p. 2041.