A Fully Integrated Low-IF CMOS GPS Radio With On-Chip Analog Image Rejection

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***Abstract*—A fully integrated Global Positioning System (GPS) radio is presented. Low-IF architecture was used for a high level of integration and low power consumption. An on-chip analog image-reject filter provides 18 dB of image-noise rejection to prevent noise figure (NF) degradation. With image rejection performed in the analog radio, a single-path (nonquadrature) output was used. The integrated synthesizer only requires an off-chip phase-locked loop-filter to function. Implemented in a 0.35-μm 2P4M CMOS process, the integrated radio has a chip area of 9.5 mm^2. The radio operates over a wide range of voltage and temperature, from 2.2 to 3.6 V and from $-40\,^{\circ}$C to $+85\,^{\circ}$C and consumes 27 mW from a 2.2-V supply. The receiver has 4 dB NF.**

***Index Terms*—CMOS radio, Global Positioning System (GPS), image rejection, receiver, VCO.**

I. Introduction

THE MARKET for Global Positioning System (GPS) radios is rapidly growing. Soon, GPS radios will be standard equipment for cars. The FCC has mandated location finding for cell phones with GPS as the prevailing technology. Manufacturers of other portable devices, e.g., portable digital assistants, have plans to integrate GPS receivers in their systems. The main requirements for all these systems are low cost, low power consumption, and minimum footprint. Only a single-chip solution can meet those requirements.

Typically, GPS radios are implemented in bipolar or BiCMOS processes and cannot be integrated with the digital signal processor chip due to higher cost. Furthermore, they use multi-downconversion receiver architectures that require off-chip filters, adding to the footprint and cost. This paper describes a highly integrated CMOS GPS radio with minimum off-chip components, which is the gating factor for the ultimate single-chip solution.

Section II describes the nature of GPS systems and signals. Sections III and IV explain the details of receiver and synthesizer design, respectively. Measurement results are presented in Section V.

II. GPS System

The GPS is a satellite-based location/time finding system with 24 satellites orbiting the earth. It is a direct sequence spread spectrum system functioning at two bands: L1 (1575.42 MHz) and L2 (1227.6 MHz) [1]. All satellites transmit at both frequencies and their signals are distinguished by different Gold codes used to spread the signal, where most commercial GPS receivers use the L1 signal only. The system is based on time-of-arrival (TOA) of signals from the visible satellites. Using the location and time information sent by satellites and TOA from at least four visible satellites, four equations can be solved for altitude, latitude, longitude, and time.

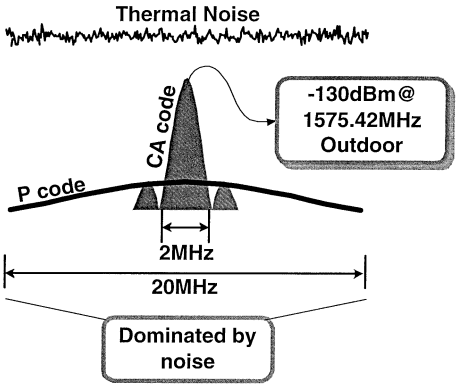

Fig. 1. GPS signals.

The GPS has two sets of codes in the L1 band, Coarse-Acquisition (C/A) and Precision (P). The original 50-b/s data is spread over a 2-MHz bandwidth (BW) for the C/A code (Fig. 1). With a -130-dBm received signal, the power spectral density (PSD) is about -193 dBm/Hz and is lower than the thermal noise level. On the other hand, the P code has a 20-MHz BW with a PSD even lower than the C/A code and is mainly used for military applications. Across the P code 20-MHz band, the signal is dominated by the thermal noise and no other signal is present. This characteristic was used to choose the optimum architecture for this GPS receiver.

III. Receiver Path

A. Architecture

This radio was designed for the L1 band and C/A code. A low-IF architecture with 1.023 MHz IF was chosen for minimum off-chip components and low power consumption (Fig. 2). The choice of 1 MHz low-IF results in an image frequency within the P-code 20 MHz BW. Thermal noise dominates the 20 MHz P-code band (Fig. 1). With IF of 1 MHz, since the image frequency of the C/A code lies in the P-code band, no other strong signals are present in this band and only

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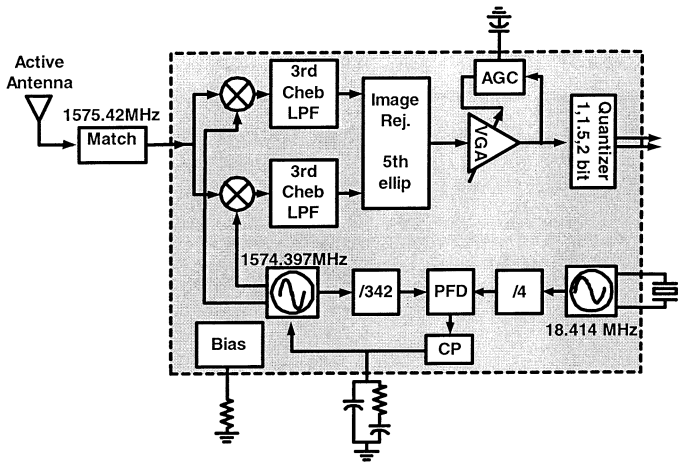

Fig. 2. Radio block diagram.

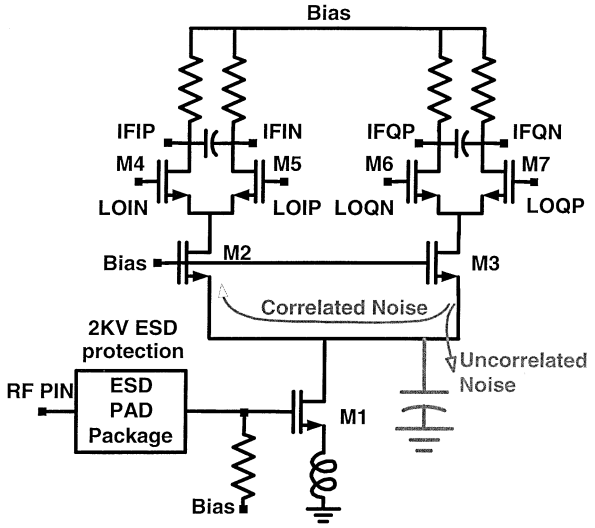

Fig. 3. Low-noise mixer.

15 dB image rejection is needed to limit the noise figure (NF) degradation due to image noise to less than 0.15 dB [2], [3].

An active antenna comprising an LNA and a filter receives the GPS signal from the satellites. After a matching circuit, the signal is input to the on-chip low-noise mixers and is downconverted to a quadrature IF of 1.023 MHz. The third-order Chebychev filters following the mixers are used for channel selection. Then, the signal passes through a fifth-order complex elliptic filter that rejects the image noise by an average of 18 dB and further attenuates out-of-band interferers. A chain of variable gain amplifiers (VGAs) then provides up to 80 dB of gain for the filtered noise and signal and sets the noise level for quantizer input. The quantizer is programmable to provide 1-, 1.5-, or 2-b outputs. The following sections describe the main building blocks of the receiver path in detail.

B. Low Noise Mixer

Fig. 3 shows the low-noise mixer [4]. M1 is an inductively degenerated CS stage at the input, designed in the same way as for an LNA [5]. The voltage amplification in the matching circuit de-emphasizes the input referred noise and improves the NF. A specially designed ESD structure provides more than 2 kVof ESD protection, without noticeable NF degradation. The series resistance usually found in an ESD structure is not used here. The output current of M1 is divided into I and Q branches (by M2 and M3, respectively) and goes to the switching devices of these two single-balanced mixers (M4–M5 and M6–M7). M2 and M3 isolate the two mixers as well as improving the LO-to-RF isolation. M2 and M3 each provides a relatively low impedance path, looking from the source of the other cascode. This increases the noise contribution of the cascode MOSFETs compared to a simple LNA.

The image reject filter rejects correlated image noise at the output of the mixers, while the uncorrelated image noise increases the NF. Here, the image noise of M1 is correlated at the output and cancelled. M2 and M3 have partly correlated noise contributions at the output.

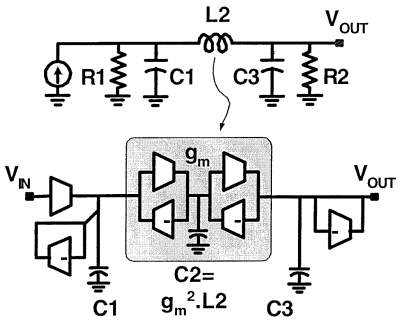

Fig. 4. Third-order Chebychev g_m/C implementation.

C. Channel Select Filter

The low-noise mixer is followed by a third-order Chebychev channel select filter with a 3-MHz BW. This filter provides the first step of out-of-band interference rejection and relaxes the linearity requirement on the image-reject filter. The filter uses a g_m/C implementation of a ladder structure. As shown in Fig. 4, the floating inductor in the LPF is replaced by a Gyrator block and the resistors are implemented using g_m stages in feedback. The filter is fully scaled for amplitude and noise [6]. A loop is used to control the g_m/C and, therefore, the bandwidth of the filter.

D. Image Reject Filter

The quadrature low-noise mixer provides quadrature signals at its output. The IF image-reject filter provides an average of 18 dB in band image rejection, without any trimming. It limits the NF degradation to below 0.07 dB.

The frequency response of a real system is symmetric around dc, as shown in Fig. 5. It passes both the positive frequencies (desired signal) and negative frequencies (image signal). An ideal image-reject filter is single-sided and only passes positive or negative frequencies. A complex frequency-shift operation converts a real low-pass function into the required complex function, as Fig. 5(a) shows [7]. The shift frequency is

$$\omega \rightarrow \omega - \omega_0. \tag{1}$$

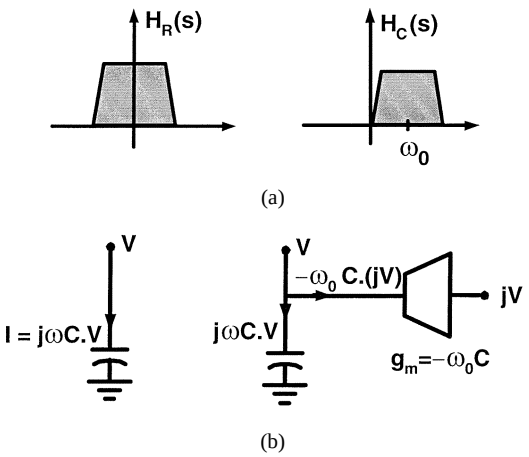

Fig. 5. (a) Conversion of a real LPF frequency response to a complex BPF by frequency shifting. (b) Capacitor transformation to implement frequency shifting in an g_m/C filter.

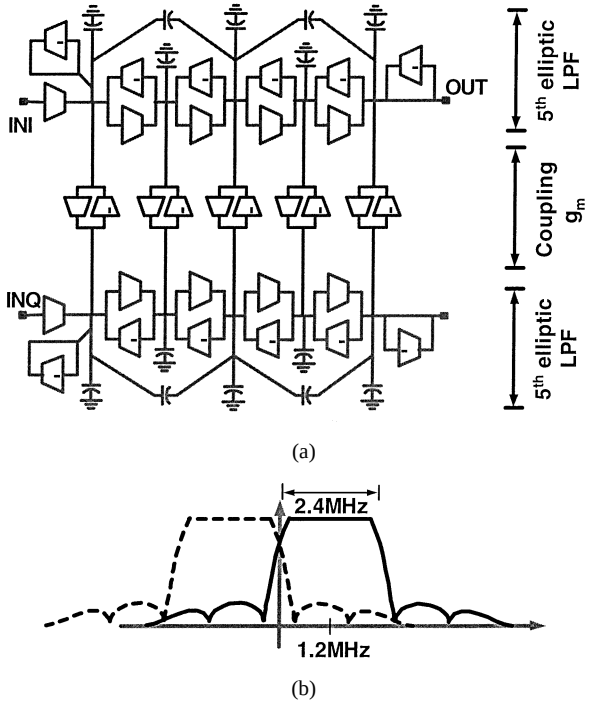

Fig. 6. (a) Implementation of the image-reject filter using two coupled fifth-order elliptic low-pass filters. (b) Complex frequency response.

Applying this operation to the current equation of a grounded capacitor yields

$$I = V.(j\omega C) \rightarrow I = V(j\omega C) - (jV)\omega_0 C \qquad (2)$$

In a quadrature system, both V and jV are available. This can be easily implemented by adding a coupling transconductor of which the input is connected to the quadrature node, as shown in Fig. 5(b). This technique was used to implement the analog polyphase image-reject filter.

Fig. 6 shows the image-reject filter. It has two fifth-order elliptic LPFs with a 1.2-MHz BW for the I and Q paths. The coupling transconductors shift the low-pass frequency response by 1.2 MHz and create the complex image-reject frequency response required for image rejection. Elliptic filters were used to provide a sharp transition close to dc and limit the in-band image noise.

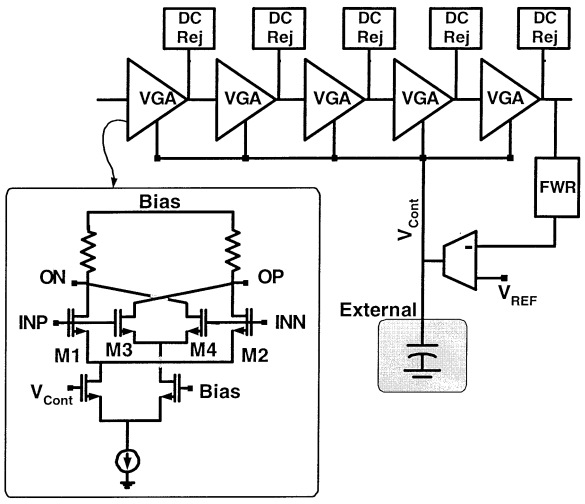

Fig. 7. VGA blocks and AGC loop.

At the output of the image reject filter, image noise is sufficiently attenuated. Since the main signal at this point is real, the quadrature path is no longer required.

E. VGA and AGC

VGA stages amplify the filtered noise and GPS signal to optimally fit the input dynamic range of the ADC. Their gain is set by the automatic-gain-control (AGC) loop (Fig. 7). The VGAs provide up to 80 dB of gain with 70 dB of gain variation. These stages have process-dependant biasing to minimize their gain variation. This gain range was implemented to accommodate different gain levels in the off-chip active antenna. Each of the VGA stages has a frequency-dependent load that reduces the gain at dc and keeps the stage gain at dc less than 1. They are implemented using a transconductor with a first-order LPF in its feedback path. This prevents the dc offset from being amplified and saturating the amplifier stages.

The output of VGA stages is full-wave rectified and compared to the desired level. The output is filtered by an off-chip capacitor and controls the gain of the VGA stages.

The VGA stages are implemented using two cross-coupled parallel amplifiers. When the control voltage ($V_{\rm Cont}$) is high, all of the current passes through the main amplifier (M1 and M2) and provides the maximum gain. By lowering the control voltage, some bias current passes through the cross-coupled amplifier (M3 and M4) and the generated signal will be subtracted from the output, reducing the total gain.

F. Quantizer

Most available GPS baseband chips available have a 1-, 1.5-, or 2-b quantized output signal. A programmable quantizer provides these three options and is implemented using three comparators. For 1-b operation, a single comparator is used. It simply compares the VGA output to "0" and generates the 1-b output. For 1.5-b operation, two comparators are used to compare the VGA output with optimum threshold levels for the GPS signal [8]. For 2-b operation, all three comparators

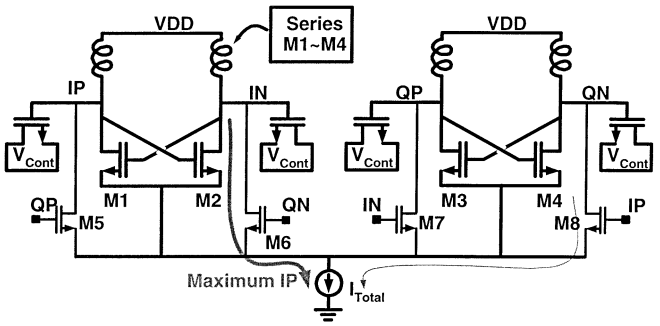

Fig. 8. The quadrature VCO.

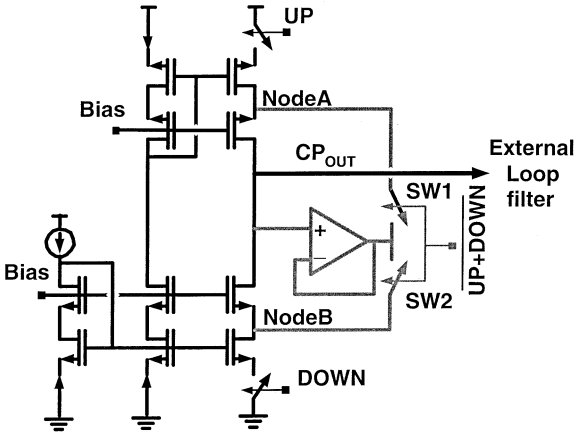

Fig. 9. The charge pump.

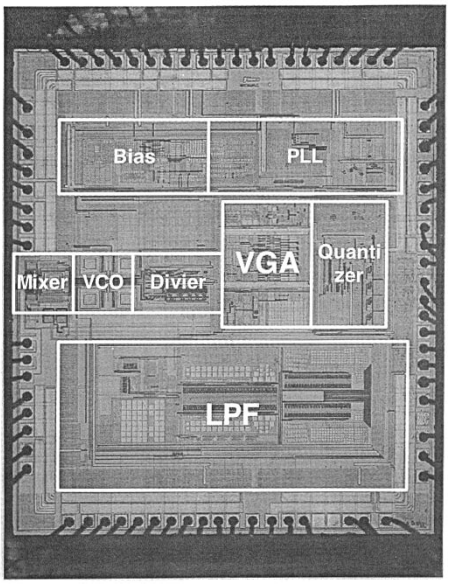

Fig. 10. Chip micrograph.

are used to generate four levels. A simple digital coder is used to convert the comparator outputs to the quantizer output bits. To accommodate different types of baseband signal processing chips, the output is provided in both CMOS full swing level and differential limited swing (with signal level of VDD and VDD-0.8 V).

The 1-b quantizer acts as a limiter. As the in-band noise dominates the signal, such a limiter is captured by the noise. This results in a signal-to-noise ratio (SNR) loss of about 2.2 dB [1].

IV. Synthesizer

A. Structure

The synthesizer is comprised of a crystal oscillator that generates the 18.414-MHz reference frequency using an off-chip crystal. Its output is divided by four and used as the comparison frequency. The VCO generates the quadrature local oscillator (LO) signals for the receiver mixers. The LO signal is divided by 342 and input to the PFD along with the comparison frequency. The PFD has a delay element in its feedback loop to prevent a dead- zone region in the charge pump. The resulting filtered charge-pump output controls the VCO. Here, an off-chip second-order filter was used (Fig. 2). GPS is a single-frequency system and a start-up time of less than 5 mS is acceptable. Therefore, synthesizer-settling time was not an important design factor.

B. VCO

Two coupled VCOs generate the quadrature LO (Fig. 8). Coupling devices are sized at 25% of the main MOSFETs to limit their power consumption and noise contribution, while providing the required coupling factor. Then, 17-nH inductors are implemented by four layers of metal in series and have a Q of 3.5. NMOS transistors are used as varactors.

Most of the published coupled quadrature VCOs use separate current sources for I and Q VCOs [9], [10]. This design shares one current source for both I and Q VCOs, resulting in higher output swing with the same total bias current. This effect can be explained in the following way. For simplicity, lets assume that coupling MOSFETs (M5–M8) drain negligible current. When one quadrature node is at its peak (e.g., IP), its voltage is higher than the other three output nodes (IN, QP, QN). One core MOSFET (M2) carrying all the tail current at its peak current would be I_{Total}. However, when using two separate current sources, the maximum current would be $I_{\mathrm{Total}}/2$. Therefore, the peak current is higher compared to a circuit using separate current sources with half of the current for each differential VCO. This provides a higher swing for the same total bias current. Current in the coupling MOSFETs exists in both cases of shared current source and separate current sources and does not affect the estimated conclusion. This VCO has 15% frequency range to cover 4% frequency variation due to temperature and 11% process variation.

C. Charge Pump

Source switching current sources are used for the charge pump (Fig. 9). In the steady state, the output current sources are off most of the time and have no power consumption. When current sources turn off, charge trapped at nodes A and B leaks to the output and increases the PLL spurs. The auxiliary circuit discharges these nodes to prevent leakage to the output. When both current sources go off, SW1 and SW2 connect nodes A and B to a buffered version of the output voltage. With a

TABLE I
RADIO PERFORMANCE SUMMARY

Supply voltage	2.2 ~ 3.6V
Supply Current @ 2.2V	12.3mA
Total Voltage Gain	~130dB
Input S11	<-10dB
NF (Quantizer input)	4dB
1dB Desensitization	-20dBm
IIP3 (tones @ 8,14MHz offset)	-15dBm
PLL spurs	-63dB
VCO PN @ 1MHz offset	-107dBc/Hz
PLL In-band PN	-72dBc/Hz

zero voltage drop across the output cascode MOSFETs, their leakage current is eliminated. In practice, very small leakage current still exists due to the opamp offset voltage.

V. MEASUREMENT RESULTS

This radio was implemented in 2P4M 0.35-μm CMOS with a total chip area of 9.5 mm^2. A 48-pin TQFP package was used. Fig. 10 shows the chip micrograph. Radio performance is summarized in Table I. This radio operates over a wide range of supply voltages, from 2.2 to 3.6 V and over a wide range of temperature from -40 °C to 85 °C. It drains 12.3 mA from a 2.2-V supply. It needs very few off-chip components to function, namely the active antenna, the matching circuit, the AGC cap, crystal, phase-locked loop (PLL) filter, and bias reference resistor. The single-ended input was matched to 50 Ω using a simple T network. It provided better than -10 dB S11 over the supply, temperature, and component variation range.

As was explained before, the natural condition for a GPS receiver is for its output to be dominated by the in-band noise. The same condition was reproduced during all measurements. With about 3-MHz approximate noise BW and assuming the NF to be around 4 dB, the equivalent input referent integrated noise level is about -105 dBm. Therefore, a -120-dBm tone was chosen as the desired in-band signal for measurements, which is at least 15 dB below the in-band noise level.

To measure the NF, a -120-dBm tone was applied at 1575 MHz to the input of the receiver and the SNR was measured. The output was monitored on a spectrum analyzer with 100-Hz resolution BW (RBW), which limited the integrated noise referred to the input of the receiver to about -150 dBm. The resulting 30 dB SNR can then be easily measured on the spectrum analyzer. The NF was calculated from the SNR using the following equation:

$$\mathrm{NF} = [-120\ \mathrm{dBm} - (-174\ \mathrm{dBm/Hz} + 20\ \mathrm{dBHz})] - \mathrm{SNR}(100\ \mathrm{HzBW}). \quad (3)$$

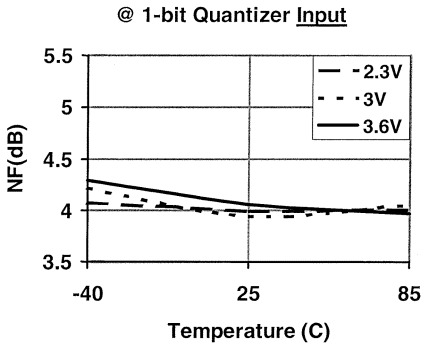

Fig. 11. NF of the RX excluding the quantizer.

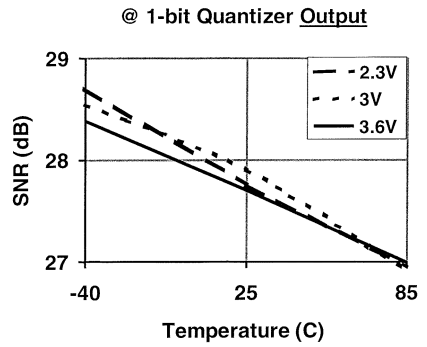

Fig. 12. SNR at the output of the 1-b quantizer.

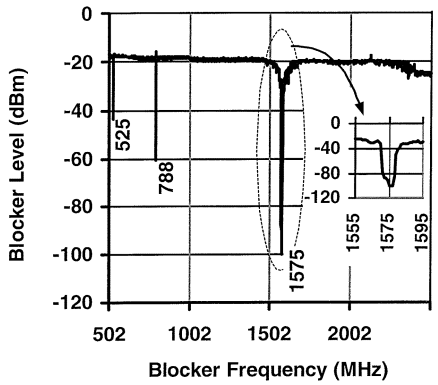

Fig. 13. The 1-dB blocker desensitization level.

A 1-b limiter captured by noise degrades the SNR. In order to separate this effect from the radio performance, the output was measured at the VGA output/quantizer input, which includes the whole RX chain except the quantizer. Fig. 11 shows that the NF is about 4 dB and is fairly constant over the temperature and supply voltage range.

In practice, 1-b digital signal processors experience SNR degradation from a 1-b quantizer. Therefore, SNR at the output of the 1-b quantizer was measured here with the same setup of a -120-dBm tone at 1575 MHz, the input, and 100-Hz resolution BW for the spectrum analyzer. Fig. 12 shows that the SNR is about 27.7 dB. This corresponds to about 2 dB SNR degradation by the quantizer.

Another important characteristic of a GPS radio is its sensitivity to the blocker signals. The 1-dB desensitization of this radio was measured in the following way: the same desired

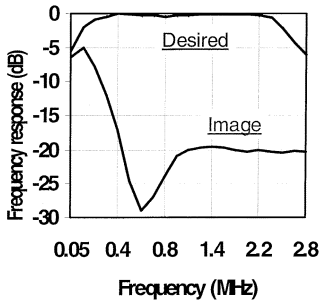

Fig. 14. Image-rejection response.

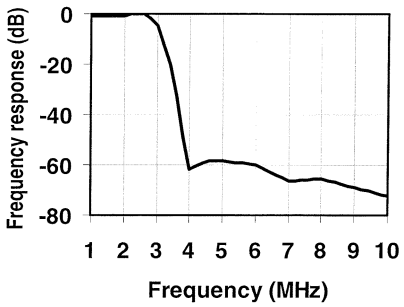

Fig. 15. IF chain frequency response.

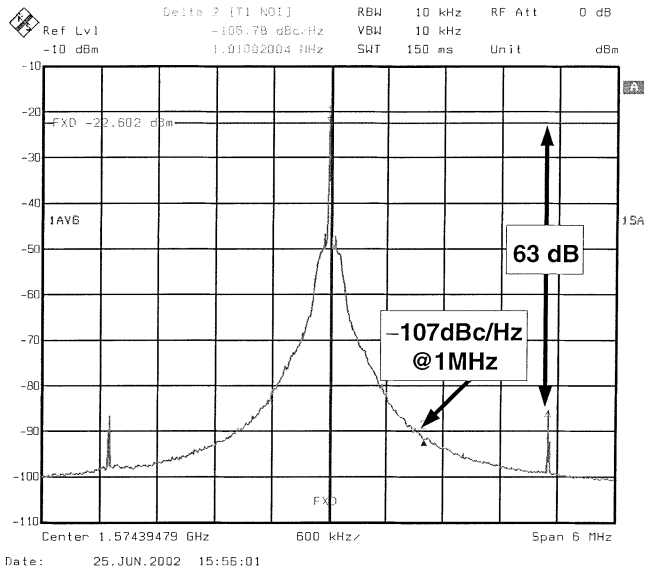

Fig. 16. Phase noise and spurs at the output of the synthesizer.

signal was applied at the input and the SNR was measured at the output of the quantizer. An interferer tone was applied at the input over a wide range of frequencies and its power was ramped up to the point that the SNR for the desired signal is decreased by 1 dB. Fig. 13 shows the results. Thanks to the filtering very early in the RX chain, this radio can tolerate a high level of −20-dBm out-of-band interference, without any off-chip filtering. The lower interference tolerance at 535 and 788 MHz is due to the in-band harmonics. The IIP3 of the radio was measured using two tones at 8 and 14 MHz to be −15 dBm.

Fig. 14 shows the on-chip image rejection frequency response. Since the signal extends from dc to 2 MHz and the image from dc to −2 MHz, there is no room for a transition band in the image rejection response at dc. Therefore, we have a transition band from dc to about 400 kHz for the image rejection to get to −18 dB. The average image noise rejection is 18 dB. The frequency response droop close to dc is caused by the dc rejection. The IF filter section provides more than 60 dB of attenuation for out-of-band signals, as shown in Fig. 15.

With a 70-kHz PLL BW, the spurs level was measured to be −63 dBc and the in-band PLL phase noise floor was −72 dBc. The main potential contributor to the output spurs level is the mismatch between the output PMOS and NMOS current sources. The VCO phase noise was −107 dBc/Hz measured at a 1-MHz offset (Fig. 16).

VI. Conclusion

A low-IF GPS radio with very few off-chip components was implemented in a pure 0.35-μm CMOS process consuming 27 mW from a 2.2-V supply. It comprises a complete receiver chain and a fully integrated synthesizer. Image noise is rejected using an on-chip analog image-reject filter. This filter was implemented by coupling two low-pass filters in the quadrature paths and converting them to a complex filter.

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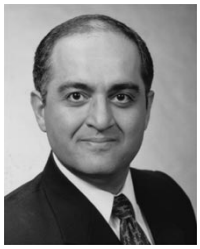

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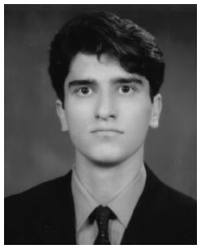
He has been with Valence Semiconductor, Inc., Irvine, CA, since 1999 as a Senior Design Engineer. His main research interests are wireless transceivers and CMOS mixed-signal circuits.



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Saket Bhatia, photograph and biography not available at the time of publication.