A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18-μm CMOS

David J. Cassan, *Member, IEEE*, and John R. Long, *Member, IEEE*

***Abstract*—A low-noise amplifier (LNA) uses low-loss monolithic transformer feedback to neutralize the gate–drain overlap capacitance of a field-effect transistor (FET). A differential implementation in 0.18-μm CMOS technology, designed for 5-GHz wireless local-area networks (LANs), achieves a measured power gain of 14.2 dB, noise figure (NF, 50 Ω) of 0.9 dB, and third-order input intercept point (IIP3) of $+0.9$ dBm at 5.75 GHz, while consuming 16 mW from a 1-V supply. The feedback design is benchmarked to a 5.75-GHz cascode LNA fabricated in the same technology that realizes 14.1-dB gain, 1.8-dB NF, and IIP3 of $+4.2$ dBm, while dissipating 21.6 mW at 1.8 V.**

***Index Terms*—Feedback amplifier, low-noise amplifier (LNA), low-voltage design, monolithic transformer/inductor, neutralization, RF CMOS, wireless LAN.**

I. Introduction

AS THE supply voltage of digital circuitry shrinks with technology scaling, RF circuit topologies that operate at voltages at or below 1 V are required. This is because integration of analog/RF and digital circuitry on the same die is desirable from both cost and packaging considerations. As operating frequencies increase, amplifier designers can no longer neglect the effects of the field-effect transistor (FET) gate–drain overlap capacitance C_{gd} on performance since it is comparable in magnitude to the gate–source capacitance in deep-submicron CMOS technologies.[1] Feedback via C_{gd} is reduced using a cascode configuration, which is arguably the most widely used topology for RF low-noise amplifiers (LNAs) in CMOS technology [1]–[4]. Particularly, all CMOS LNAs reported to date for 5-GHz wireless local-area networks (LANs) employ cascode topologies [5], [6]. Although these implementations meet wireless LAN performance requirements, a two-transistor stack is not optimal for operation at the lowest possible supply voltage. The feedback amplifier presented in this paper employs reactive negative feedback through an on-chip transformer to neutralize C_{gd}, while also allowing a drain–source bias voltage equal to the supply voltage (i.e., $V_{DS} = V_{DD}$). As a result, gain and dynamic range are not compromised when only a single active device is used.

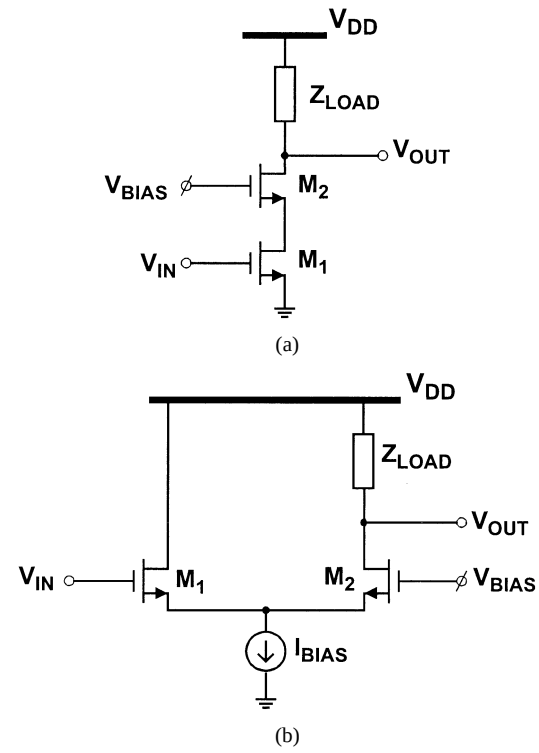

Fig. 1. Unilateralization circuit techniques. (a) Telescopic cascode technique. (b) Source-coupled technique.

Section II of this paper introduces the concept of C_{gd} neutralization in the context of RF amplifier design. Section III presents a theoretical analysis of the transformer feedback amplifier topology and derives the condition required for neutralization. Design of a conventional differential cascode LNA to meet comparable RF specifications is then presented in Section IV. Implementation of both feedback and cascode amplifiers in the same technology allows for a direct comparison of experimental results, which are presented in Section V.

II. RF Amplifier Unilateralization and Neutralization

FET gate–drain overlap capacitance C_{gd} is an unavoidable parasitic for CMOS technologies caused by lateral diffusion of the drain dopant under the polysilicon gate material. C_{gd} adds a (noninverting) signal path which reduces amplifier forward gain and feedback via C_{gd} reduces amplifier output to input (i.e., reverse) isolation. C_{gd} also decreases device f_t (i.e., $f_t = g_m/2\pi(C_{gs}+C_{gd})$) and its effect on the input capacitance is multiplied by the Miller effect (i.e., $C_{\rm eq} = C_{gd}(1 + A_v)$)

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[1] $C_{gd}/C_{gs} \approx 0.3$ for the 0.18-μm CMOS technology used in this work.

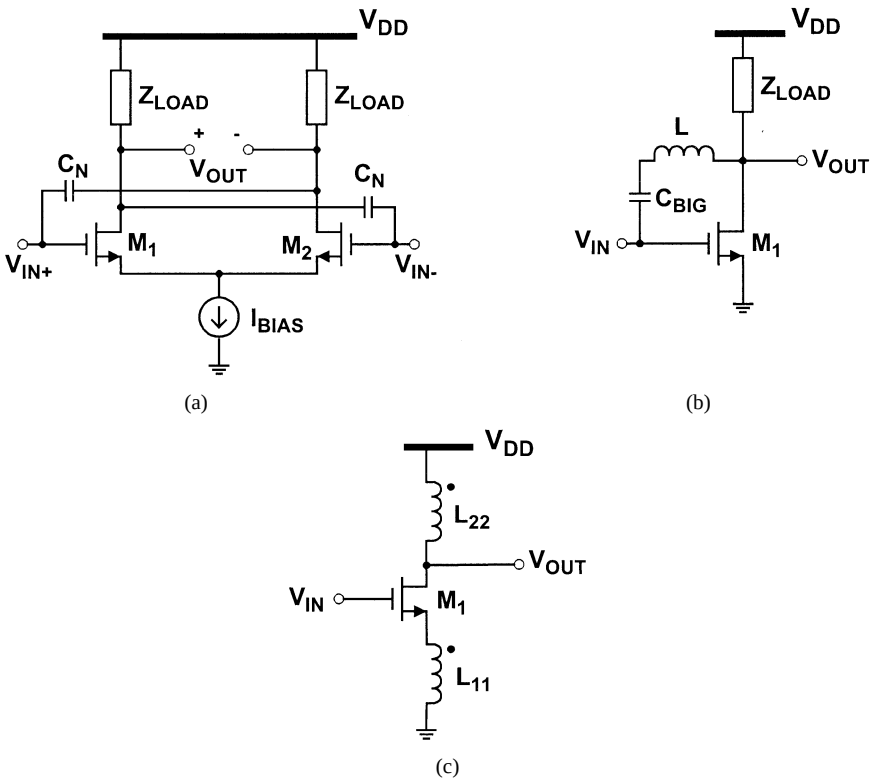


Fig. 2. Neutralization circuit techniques. (a) Differential neutralization technique. (b) Inductor-tuned technique. (c) Transformer-feedback technique.

in a common-source configuration. Since C_{gd} degrades amplifier performance, it is natural to look for ways to reduce its effects. Circuit techniques that mitigate the effect of C_{gd} are usually grouped into two categories: unilateralization and neutralization.

Unilateralization decreases reverse signal flow and, thus, coupling between output and input ports of an amplifier. Cascoding of a common-source and common-gate stage [Fig. 1(a)] is a common unilateralization technique. Another possible unilateralization topology is the source-coupled amplifier, which is a cascode of source–follower and common-gate stages as shown in Fig. 1(b). Both the cascode and source-coupled amplifiers reduces the voltage swing across C_{gd} by concentrating the amplifier's voltage gain across a common-gate stage. Miller multiplication of C_{gd} seen at the common-source input and its adverse affects on bandwidth are thereby reduced. A two-stage design also improves reverse isolation, which increases stability and allows for simpler matching network design in an RF application [7]. However, the second stage occupies voltage headroom, introduces additional noise, and is potentially unstable if the gate of the second stage is not at small-signal ground.

Neutralization cancels signal flow through C_{gd} by adding additional signal paths around the amplifier so that the net signal flow through C_{gd} and the additional signal path is zero. This increases forward gain and reverse isolation for a given power consumption, but does not necessarily reduce the effect of C_{gd} on the input capacitance. Three examples of C_{gd} neutralization are shown in Fig. 2. Fig. 2(a) uses neutralizing capacitors C_N to cancel the signal flow through C_{gd} [8]. Since the drain voltages of the differential pair are 180° phase shifted, the current through C_N is equal in magnitude and opposite in phase to the current flowing through C_{gd} (if $C_N = C_{gd}$), which achieves neutralization. This topology requires differential drive of the amplifier and relies on precise matching of C_N and C_{gd}. Furthermore, signal flow through C_N is actually positive feedback that can cause instability if C_N does not exactly equal C_{gd} (i.e., a net positive feedback can result for $C_N > C_{gd}$). Neutralizing capacitors C_N also double the effective capacitance at the input and drain nodes by C_{gd}, which adversely affects gain, bandwidth, and terminal impedances.

The circuit of Fig. 2(b) uses an inductor L to resonate with C_{gd}. This technique is usually impractical for monolithic implementations because the required value of inductance is too large to be integrated (i.e., $L = 38$ nH for a 6×10 μm/0.18 μm FET at 5.75 GHz). Furthermore, the bottom-plate parasitic capacitance of the required dc-block capacitor [$C_{\rm BIG}$ in Fig. 2(b)] severely loads the gate and drain nodes, which reduces the forward gain through the transistor transconductance. This, combined with the low quality factor Q of a monolithic inductor, increases the amplifier noise figure.

III. Transformer-Feedback LNA

An alternative approach to neutralization uses transformer feedback, which introduces magnetic coupling between drain and source inductors of a common-source transistor, as shown in Fig. 2(c). Feeding back a portion of the output signal via the transformer can effectively cancel the feedback from output to input through the Miller capacitance (C_{gd}) and neutralize the amplifier. The circuit parameters that define this condition are derived in Sections III-A and B.

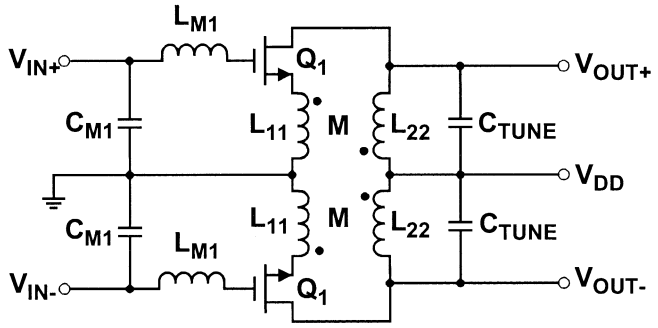


Fig. 3. Differential transformer-feedback LNA schematic.

A. Analysis

Magnetic coupling between the input and output using a transformer as shown in Fig. 2(c) adds negative feedback, which can be appreciated by applying a small positive test voltage at node $V_{\rm IN}$. The increased drain current lowers $V_{\rm OUT}$ or, equivalently, increases the ac voltage drop across L_{22}. This causes the voltage across the primary L_{11} to also increase but in the opposite direction due to the inverting wiring configuration (indicated by the dots). Therefore, V_{gs} decreases, which is negative feedback. Note that this is in addition to the reduction of V_{gs} by inductive degeneration alone.[2] The benefits of negative feedback in amplifier design are well known, for example, transformer feedback has been shown to increase the linearity of a common-emitter LNA in [9].

A simplified schematic of the differential transformer-feedback LNA is shown in Fig. 3. The differential design reduces the effect of ground path parasitics and increases common-mode rejection. Primary and secondary inductances L_{11} and L_{22} implement a differential transformer with magnetic coupling M. Elements C_{M1} and L_{M1} implement an L-section input-matching network and $C_{\rm TUNE}$ resonates with the secondary inductance of the transformer at the operating frequency. For the following analysis, these components can be neglected.

Since the amplifier is excited differentially, the half-circuit concept can be applied, resulting in the single-ended small-signal equivalent circuit of Fig. 4(a). An h-parameter transformer representation [Fig. 5(a)] is used to allow for varying levels of complexity in transformer modeling. The transformer h parameters are given by

$$h_{11} = s(1-k^2)L_{11} \approx 0 \quad h_{12} = \frac{-k}{n} \approx \frac{-1}{n} \tag{1}$$

$$h_{21} = \frac{k}{n} \approx \frac{1}{n} \quad h_{22} = \frac{1}{sL_{22}} \approx 0 \tag{2}$$

where the equality in (1) and (2) applies for nonideal magnetic coupling and the approximation for an ideal transformer. The transformer turns ratio is given by $n = \sqrt{L_{22}/L_{11}}$ and the transformer coupling coefficient by $k = M/(\sqrt{L_{11}L_{22}})$ [10]. In later stages of design, S parameters from electromagnetic simulation or measurement can be converted into h parameters. Impedances Z_{gs} and Z_{gd} represent FET capacitances C_{gs} and C_{gd}, respectively. Source impedance $Z_{\rm src}$ is the impedance seen looking toward the generator from the FET gate, and is equal to the complex conjugate of the impedance seen looking into the FET gate when the input is impedance matched to the generator. Z_L represents a composite load impedance (i.e., $Z_L = 1/(sC_{\rm TUNE})\|r_{ds}\|1/(sC_{db})$) that models loading on the output node. The approximation that r_{ds} is connected between drain and ground is used to include its loading effect on the output node but neglects the signal flowing into the FET source node. Since the impedance at the source terminal is relatively small, this results in minimal loss of accuracy.

The forward signal-flow graph, derived from the small-signal model, is shown in Fig. 4(b). The input signal is the FET gate voltage V_g and the error signal is taken as the gate–source voltage V_{gs}. The signals are taken to sum at node V_{gs}. The primary active path consists of a voltage divider between the gate and gate–source voltage of the transistor (path G_i), which excites the FET voltage-controlled current source and results in a voltage at the output node via active path G_a. Feedforward through the transformer is represented by path G_x and feedback through the transformer by H_x. Since h_{12} is a negative quantity (i.e., inverting transformer), the feedback path subtracts from the signal applied at the input. This is the desired negative feedback signal; it reduces the transistor gate-source voltage, thereby reducing amplifier gain. The remaining path is a passive feedforward path via the FET gate–drain overlap capacitance G_C. Since the overlap capacitance connects directly to an independent voltage source V_g, feedback through C_{gd} does not affect the forward signal-flow graph.

The voltage gain A_V, can be computed either by signal-flow graph simplification or by using Mason's rule [10]

$$\begin{aligned} A_V =& \frac{V_{\rm out}}{V_g} = \frac{G_C + G_i(G_a + G_x)}{1 - H_x(G_a + G_x)} \\ =& \frac{-(Z_L\|Z_{gd})\beta(s) - (Z_L\|Z_{gd})\left(\frac{\beta(s)+1}{n}\right) + Z_L\|Z_{gd}}{Z_{gs} + \frac{\beta(s)(Z_L\|Z_{gd})}{n} + \frac{(\beta(s)+1)(Z_L\|Z_{gd})}{n^2}} \end{aligned} \tag{3}$$

where an ideal transformer is assumed and $\beta(s) = g_m Z_{gs}$ is the FET current gain. The numerator in (3) consists of the amplifier gain referred to the gate current of the FET (i.e., $V_{\rm out} = N(s)i_g$) and the denominator defines the impedance seen looking into the gate of the FET (i.e., $V_g = D(s)i_g \Rightarrow D(s) = V_g/i_g$). The numerator consists of three components: the active gain through the transistor transconductance, passive feedforward through the transformer, and passive feedforward through C_{gd}, respectively. From this result, it is clear that bilateral signal flow through the transformer complicates the operation of the transformer-feedback LNA, even when considering an ideal transformer. However, the feedforward signal through the transformer does not subtract from the amplifier voltage gain, but feedforward through C_{gd} does, suggesting that these signal paths can be designed to cancel. The condition required for amplifier neutralization, however, is not obvious from these results.

The condition required for neutralization is derived from the reverse signal-flow graph of Fig. 4(c). When considering the reverse signal flow, output voltage $V_{\rm out}$ is an independent variable and the voltage at the FET gate V_g a dependent variable. Any impedance connecting the independent variable to ground

[2]Note that the addition signal path in Fig. 2(c) is between drain and source instead of between drain and gate as in Fig. 2(a). This allows negative feedback rather than positive feedback to be used to achieve amplifer neutralization.

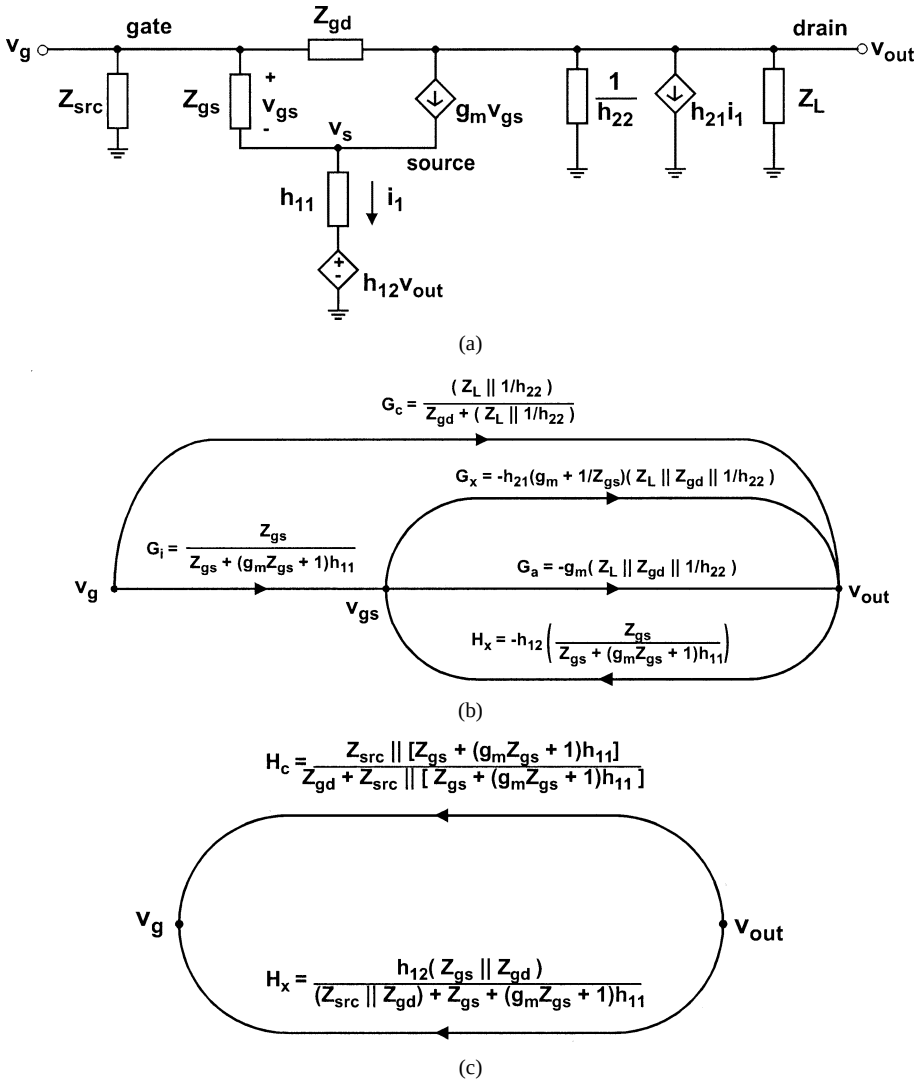


Fig. 4. Signal flow analysis. (a) Small-signal model. (b) Forward signal-flow graph. (c) Reverse signal-flow graph.

[i.e., Z_L and $1/h_{22}$ from Fig. 4(a)] has no effect on the reverse signal flow and does not appear in the flowgraph. The signal-flow graph has been simplified using signal-flow graph reduction rules [7] to eliminate the intermediate node V_s. From Fig. 4(c), we can see that there are two reverse signal paths through the amplifier: path H_x represents reverse signal flow through the transformer and path H_C represents reverse signal flow through the gate–drain capacitance C_{gd}. Since h_{12} is a negative quantity, these two paths can be designed to cancel to neutralize the amplifier. Setting $H_C = -H_x$ results in

$$\frac{n}{k} \approx \frac{C_{gs}}{C_{gd}} \tag{4}$$

using nonideal magnetic coupling transformer h parameters. Therefore, neutralization is achieved when the effective transformer turns ratio n/k is set equal to capacitance ratio C_{gs}/C_{gd}.[3] For the 0.18-μm CMOS technology used in this work, $C_{gs}/C_{gd} \approx 3$, so a transformer turns ratio of 2.4 and coupling coefficient of 0.8 can be used. These values can be attained using a monolithic transformer, making the neutralization technique practical for monolithic implementations in submicron CMOS technology.

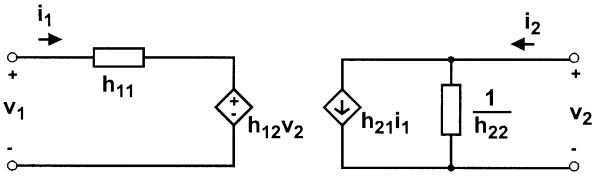
Equation (4) shows close agreement with simulation results. Note also that there is no frequency dependence in the neutralization condition, implying that transformer feedback can be used as a wide-bandwidth neutralization technique restricted only by the bandwidth of the transformer. For a given LNA design, the transformer turns ratio n is often constrained by linearity, gain, and noise specifications. In these cases, the coupling coefficient k is the extra degree of freedom that can be adjusted to achieve amplifier neutralization. This can be accomplished by adjusting the spacing between the transformer primary and secondary windings.

B. Design

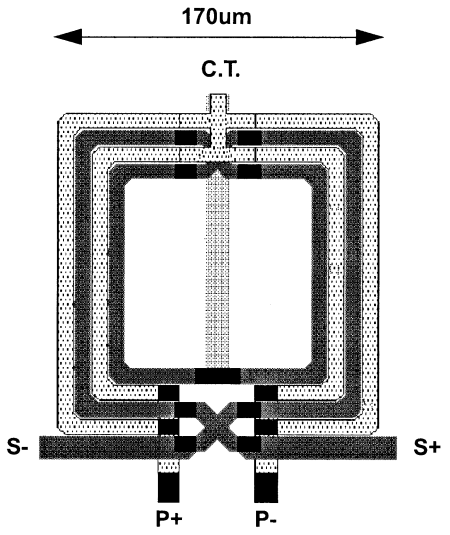
The transformer feedback LNA is designed to adhere to performance specifications required for an IEEE 802.11a wireless LAN receiver operating between 5–6 GHz. The proposed LNA performance specifications are listed in Table I [11], [12].

Because of the low supply voltage ($V_{DD} = 1.0$ V) and velocity saturation, linearity is constrained by the maximum signal swing before waveform clipping. [Note that $P_{\text{lin,max}}$

[3]The impedance seen looking toward the generator (Z_{src}) factors out of the resulting expression, which indicates that it affects both signal paths equally.



(a)



(b)

Fig. 5. Monolithic transformer. (a) h parameter representation. (b) Layout.

TABLE I
PROPOSED 5-GHZ WIRELESS LAN LNA PERFORMANCE SPECIFICATIONS

Center Frequency	5.75 GHz
Gain (S_{21})	15 dB
Reverse Isolation (-S_{12})	≥ 20 dB
Noise Figure (NF)	≤ 2 dB
Input IP3 (IIP3)	≥ 0 dBm
Input and Output Impedances	50 Ω
Input and Output Return Loss	≥ 10 dB
3-dB Bandwidth	≥ 150 MHz

is roughly 10 dB below the third-order intercept point (IP3) for a third-order nonlinearity.] This allows a load line analysis to be used when designing for linearity, as shown in Fig. 6. Load R_L is ac coupled at the output by capacitor $C_{\rm BIG}$, where R_L is the impedance of the tuned load at resonance (i.e., $R_L = Q_{\rm sec}\omega_o L_{22}$). For simplicity, the dc voltage drop across both transformer primary and secondary windings is assumed zero. The maximum linear output power then is given by

$$P_{\rm lin,max} = (V_{DD} - V_{ds,\rm sat})\frac{I_D}{2} \tag{5}$$

a value that is achieved by choosing

$$R_L = \frac{(V_{DD} - V_{ds,\rm sat})}{I_D} \tag{6}$$

which is the load impedance that ensures maximum voltage and current swing simultaneously at the drain node. Note that $P_{\rm lin,max}$ is directly proportional to the bias current and that more increases linearity and lowers the optimal load resistance. This result helps to explain why FETs used in RF applications require relatively large bias currents to achieve sufficient linearity. A bias current of $I_D = 8$ mA is required to achieve an input IP3 > 0 dBm ($P_{\rm lin,max} = 5$ dBm) from a 1-V supply.

The noise figure of an amplifier depends on the impedance presented at its input port, and minimum noise figure is achieved only for the optimum source impedance ($Z_{\rm src,opt}$). Unfortunately, this impedance is usually not equal to the complex conjugate of the amplifier input impedance $Z_{\rm in}$ required for an impedance match. This suggests a tradeoff between noise performance and power transfer unless these impedances can be made equal. For a common-source transistor, $X_{\rm src,opt} \approx -X_{\rm in}$ [8], so this simplifies the design problem to matching only the real components. For interdigitated FETs, $R_{\rm src,opt}$ scales inversely with the number of fingers [13] while $R_{\rm in}$ can be set by inductive degeneration [14]. Because of the complexity of the RF circuit models and magnetic coupling through the transformer, optimizations using computer simulations are required to accurately set $R_{\rm src,opt} = R_{\rm in}$. A FET width of 20×5 μm and transformer primary inductance of 0.16 nH result in $R_{\rm src,opt} \approx R_{\rm in} = 12\ \Omega$ for the 0.18-μm CMOS technology used in this work. Since this does not equal to the desired input impedance of 50, an L-section matching network precedes the LNA.[4] This matching network is not implemented on chip since the loss of a monolithic inductor in series with the gate would degrade noise performance, and also because in practical implementations a bondwire inductor could be used to implement all or part of L_{M1}. The impedance-matching bandwidth is determined solely by the impedance transformation ratio (i.e., $Q = \sqrt{50/12 - 1} = 1.8$) [8]. The low Q factor ensures a broad input impedance match.

The monolithic transformer is designed following the procedure outlined in [10] to achieve neutralization [as per (4)] and the transformer physical layout shown in Fig. 5(b). The transformer employs a symmetric (i.e., Rabjohn) winding style and both the primary and secondary winding are implemented in top metal to reduce series resistance and capacitance to substrate. A turns ratio of approximately 2 is realized by using two turns in series for the transformer secondary and two turns in parallel for the primary. The transformer secondary is shaded in Fig. 5(b) for easier visualization. The symmetric layout allows bias to be applied at the winding center taps as they appear as a virtual ground when the transformer is differentially excited. Transformer parameters $L_{11} = 0.16$ nH, $L_{22} = 0.70$ nH, $k = 0.59$, and $Q_{\rm sec} = 6.1$, result from transformer dimensions: outer diameter $= 170$ μm, conductor width $= 8$ μm, and conductor spacing $= 1$ μm. A good 50-Ω output impedance match is attained by adding only a capacitor in parallel with the transformer secondary $C_{\rm TUNE}$ to resonate at the operating frequency. The inherently low output impedance of the topology results in a low-Q resonance and allows the amplifier to have sufficient gain when directly driving a low-impedance load (i.e., 50 Ω).

[4]The L-section matching network also provides the conjugate input impedance to the FET gate when looking toward the generator.

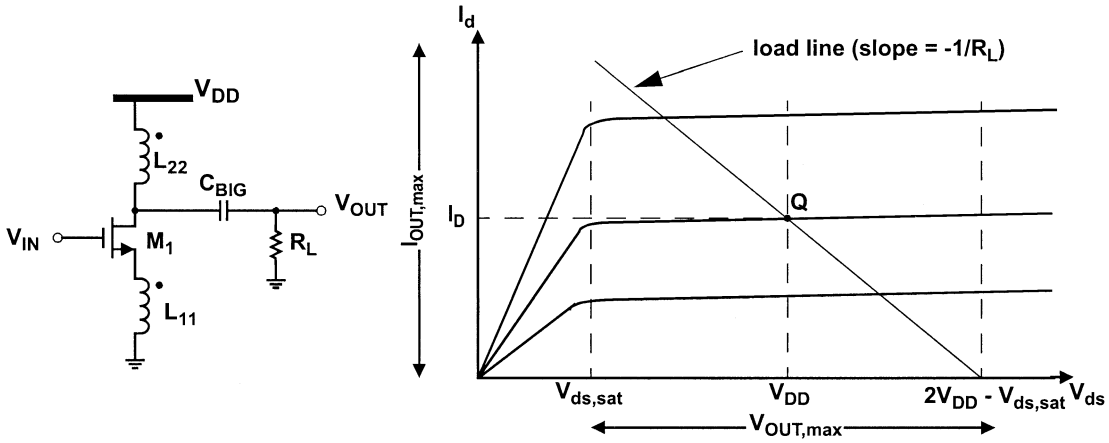


Fig. 6. Load-line analysis of transformer-feedback LNA.

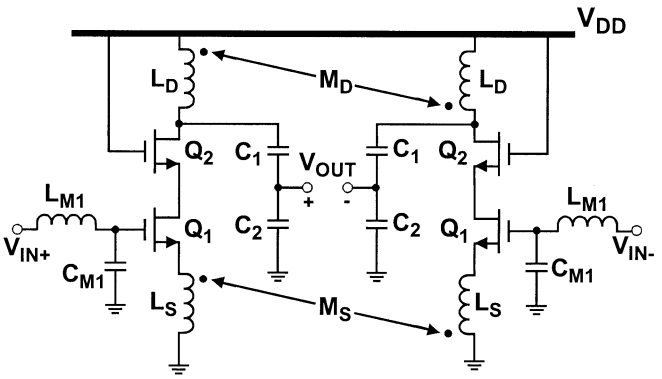


Fig. 7. Differential cascode LNA schematic.

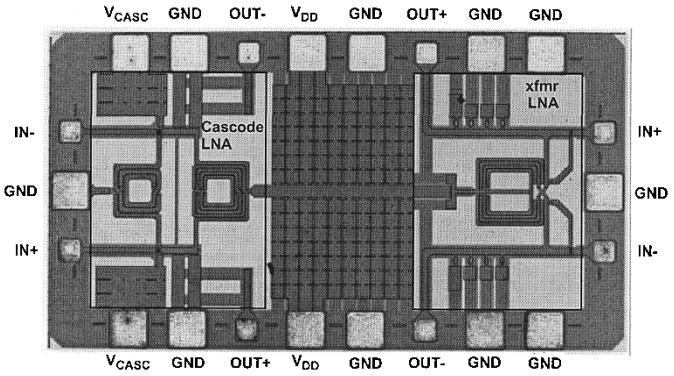


Fig. 8. Chip micrograph.

IV. Differential Cascode LNA Design

A 1.8-V differential cascode LNA is also implemented in 0.18-μm CMOS as a benchmark to allow a direct comparison with the transformer-feedback topology. A simplified schematic of the differential cascode LNA is shown in Fig. 7.

A 6-mA drain current is required to achieve an input IP3 > 0 dBm from a 1.8-V supply. Initially, a 1-V design was attempted, but simulation results indicated insufficient gain and linearity at 5.75 GHz. Inductor L_s and the width of transistor Q_1 are optimized for minimum noise figure. The minimal magnetic coupling between drain and source inductors results in the input impedance more closely matching the equations for inductor degeneration [14], simplifying the design for minimum noise figure. A FET width of 6×10 μm and $L_s = 0.51$ nH results in $R_{\mathrm{src,opt}} \approx R_{\mathrm{in}} = 100\ \Omega$. An L-section matching network (L_{M1} and C_{M1}) is again required to provide the required 50-Ω input impedance with an input Q factor of 3.8. All elements are implemented on-chip except for the input-matching network inductor L_{M1}.

Inductor $L_D = 1.6$ nH, along with tapped capacitors ($C_1 = 412$ fF and $C_2 = 863$ fF), implements a tuned load and impedance matches the LNA output to 50 Ω. The gate of cascode transistor Q_2 is connected to V_{DD} to maximize the drain–source voltage (and, hence, f_T) of drive transistor Q_1. The gate of Q_2 is kept at small-signal ground by both the differential topology and decoupling capacitance implemented on and off chip. Q_2 and Q_1 have equal widths and a dual-gate layout reduces parasitic capacitance at the common node. Minimum gate length is used for all devices to maximize device f_T.

Magnetic coupling between half-coils of L_D and L_S (M_D and M_S) is used to indicate the use of differentially excited symmetric inductors [15]. The use of differential inductors in this design decreases chip area and increases performance as differential excitation results in an increase of approximately 50% in the peak Q factor. This improvement in Q translates directly into higher gain or lower power consumption for the cascode LNA.[5]

A chip micrograph of the LNAs is shown in Fig. 8. Both amplifiers are placed in the same pad frame and the transformer and cascode LNA occupy an active area of 0.4×0.6 mm^2 and 0.3×0.5 mm^2, respectively. The physical layout is pad frame limited, which allows 35 pF of decoupling between V_{DD} and ground. Note that the cascode LNA requires two monolithic microstrip spirals while the transformer-feedback LNA requires only one.

V. Experimental Results

All measurements were made under the same bias conditions and the same input matching (i.e., S_{11} condition) to

[5]The differential-mode inductance is $L_{\mathrm{eff}} = (1 + k)L$ while the common-mode inductance is $L_{\mathrm{eff}} = (1 - k)L$, which also improves common-mode rejection of the cascode LNA.

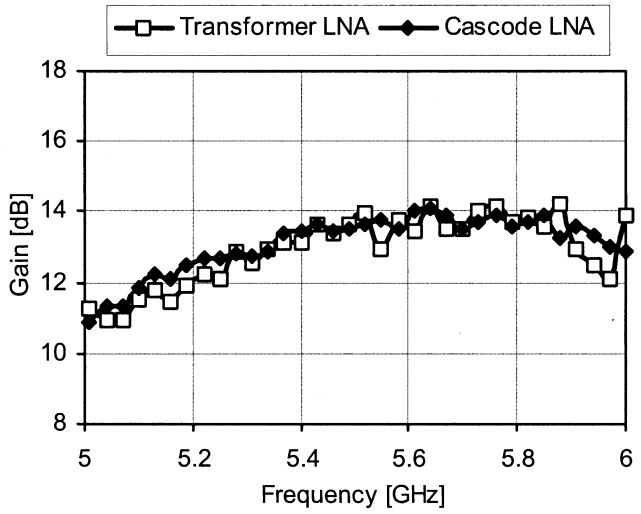


Fig. 9. Measured gain.

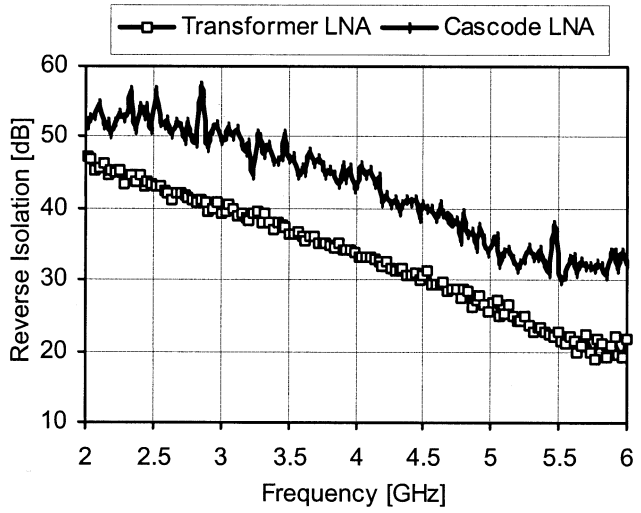


Fig. 10. Measured reverse isolation.

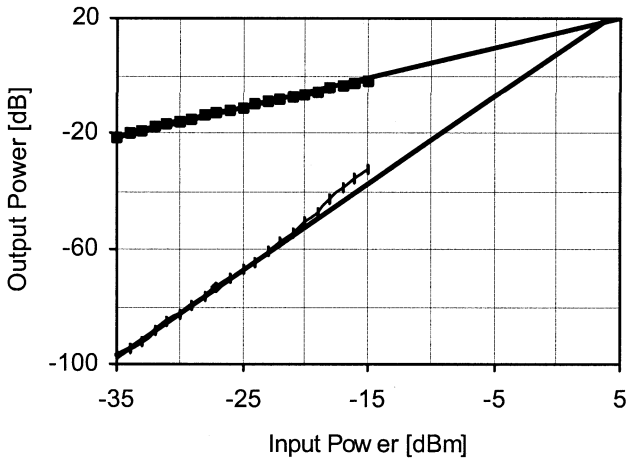


Fig. 11. Two-tone intermodulation distortion test on cascode LNA.

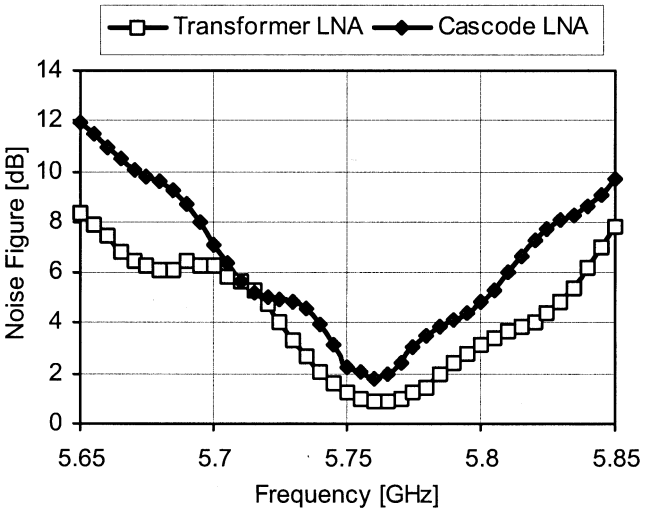


Fig. 12. Measured noise figure with input conjugate matched.

obtain a conjugate input impedance match. The small-signal performance of the LNAs was characterized on-wafer from four-port S-parameter measurements. Input port matching was accomplished using postprocessing of the measured data. On-chip output matching is sufficient to realize a minimum return loss of 8 and 11 dB for the transformer and cascode LNA, respectively, over a 150-MHz bandwidth centered at 5.75 GHz.

The differential-mode gain is plotted in Fig. 9. Both amplifiers achieve a maximum gain of approximately 14 dB. This is 1 dB less than the original specifications, but is still adequate for wireless LAN. The relatively flat response (-3 dB bandwidth >1 GHz) indicates suitability for wide-band applications between 5–6 GHz. Gain rolloff at lower frequencies is due to low-Q resonant tuning at the input and output ports. The lower -3 dB frequency is approximately 5 GHz for both amplifiers, while the upper -3 dB corner lies above the 6-GHz limit of the four-port S-parameter test set.

The reverse isolation is shown in Fig. 10. The plot is taken over a large frequency range to show the high out-of-band reverse isolation. The minimum isolation of the transformer LNA is 19 dB and the cascode LNA achieves 32 dB. The cascode LNA shows an isolation approximately 10 dB greater than the transformer LNA over the entire frequency range examined. From a system perspective, the local oscillator frequency and its second harmonic are frequencies at which poor reverse isolation can compromise system performance. For a heterodyne receiver, these frequencies are far outside the intended radio band, where both LNAs show an isolation greater than 30 dB. Furthermore, measurements of a common-source 100-μm-wide transistor give a reverse isolation of 13 dB at 5.75 GHz, validating the wide bandwidth C_{gd} neutralization technique using a monolithic transformer.

Third-order intercept (IP3) measurements were performed using $0^\circ/180^\circ$ microwave hybrids for differential excitation and coaxial sliding screw tuners for input port matching. Results from the two-tone intermodulation distortion test for the cascode LNA are shown in Fig. 11, as a representative example. Intersection of the two regression lines defines an input referred IP3 point of $+4.2$ dBm. Similarly, the transformer LNA achieves an input IP3 of $+0.9$ dBm.

TABLE II
LNA PERFORMANCE SUMMARY

Parameter	**Measured Differential Transformer LNA**	**Measured Differential Cascode LNA**	SiGe single-ended Transformer LNA [16]	CMOS Differential Cascode LNA [5]
Frequency	**5.75GHz**	**5.75GHz**	2.4GHz	5.15GHz
Transducer Power Gain ($\|S_{21}\|$)	**14.2dB**	**14.1dB**	10.5dB	16dB
Noise Figure	**0.9dB**	**1.8dB**	0.95dB	2.5dB
IIP3	**0.9dBm**	**4.2dBm**	-4.5dBm	-11.3dBm*
Supply Voltage	**1.0V**	**1.8V**	1.0V	3.0V
Power Dissipation	**16mW**	**21.6mW**	2.5mW	48mW
Technology	**0.18μm CMOS**	**0.18μm CMOS**	0.50μm SiGe HBT	0.25μm CMOS

* Value quoted for receive path (LNA + mixer). LNA linearity must be at least this value.

Noise figure was measured using an HP-8970 noise figure meter and input noise matching was accomplished using coaxial sliding screw tuners. The tuners were adjusted to provide a conjugate impedance to the LNA input (i.e., the same condition under which gain was measured). The resulting noise figure for both LNAs is plotted in Fig. 12. The minimum noise figure of the transformer LNA is 0.9 dB and the cascode LNA achieves 1.8 dB.[6] The transformer LNA shows lower noise than the cascode since the noise added by the cascode devices increases the noise figure of the cascode LNA.

A summary of the measured performance of both LNAs appears in Table II. For comparison, results of a transformer-feedback LNA implemented in a SiGe technology [16] and a 5-GHz differential CMOS cascode LNA [5] are also included in the table. The SiGe LNA outperforms both the implemented transformer and cascode LNA in terms of power consumption. This can be attributed to the single-ended design, the lower center frequency, and the technology improvement of 0.5-μm SiGe over 0.18-μm CMOS. The measured cascode LNA, however, shows better performance than [5]. This can be partly attributed to the improvements in technology between 0.18- and 0.25-μm CMOS.

Both the transformer LNA and the cascode LNA show less than 2 dB noise figure and greater than 0 dBm input-referred IP3. Overall, the transformer and cascode designs show similar measured performance, but the transformer LNA accomplishes this while running from a lower supply voltage and consuming less power. Also, when the transformer LNA is compared with the differential cascode LNA in [5], the transformer LNA shows better overall performance while reducing both the supply voltage and power dissipation by a factor of three. This indicates that the transformer-feedback LNA topology offers competitive performance to the cascode while significantly reducing both the supply voltage and power dissipation.

[6]The narrow-band nature of this plot is due to the narrow-band frequency response of the tuners.

VI. CONCLUSION

A negative feedback transformer neutralization technique has been shown to be practical for monolithic implementations. An implemented 0.18-μm CMOS transformer-feedback LNA offers competitive performance to a cascode topology while reducing supply voltage and power dissipation. Differentially excited symmetric inductors are used for the cascode LNA to increase performance and reduce die area.

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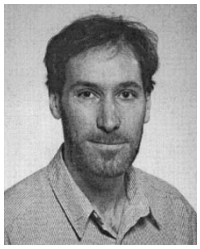

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