A 2.4-GHz-Band 1.8-V Operation Single-Chip Si-CMOS T/R-MMIC Front-End with a Low Insertion Loss Switch

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***Abstract*—This paper describes the design and experimental results of a 1.8-V single-chip CMOS MMIC front-end for 2.4-GHz band short-range wireless communications, such as Bluetooth and wireless LANs. The IC consists of fundamental RF building circuits—a power amplifier (PA), a low-noise amplifier (LNA), and a transmit/receive-antenna switch (SW), including almost all on-chip matching elements. The IC was fabricated using a 0.18-μm standard bulk CMOS technology which has no extra processing steps to enhance the RF performances. Two new circuit-design techniques are introduced in the IC in order to minimize the insertion loss of the SW and realize a higher gain for the PA and LNA despite the utilization of the standard bulk CMOS technology. The first is the derivation of an optimum gate width of the SW to minimize the insertion loss based on small-signal equivalent circuit analysis. The other is the revelation of the advantages of interdigitated capacitors (IDCs) over conventional polysilicon to polysilicon capacitors and the successful use of the IDCs in the LNA and PA. The IC achieves the following sufficient characteristics for practical wireless terminals at 2.4 GHz and 1.8 V: a 5-dBm transmit power at a -1-dB gain compression, a 19-dB gain, an 18-mA current for the PA, a 1.5-dB insertion loss, more than 24-dB isolation, an 11-dBm power handling capability for the SW, a 7.5-dB gain, a 4.5-dB noise figure, and an 8-mA current for the LNA.**

***Index Terms*—Front-end, low-noise amplifier, monolithic microwave integrated circuit, power amplifier, Si-CMOS, switch, wireless communications.**

I. Introduction

MOTIVATED by the growing need for low-power and low-cost wireless transceivers, various mainstream IC technologies are competing to integrate more RF functions onto a single chip as well as to construct discrete RF building blocks [1]–[19]. GaAs, Si-bipolar, and Si-BiCMOS monolithic microwave integrated circuits (MMICs), as is well known, currently dominate the practical integration in the frequency range from 1.0 to 6.0 GHz [20]–[25]. As recent studies have demonstrated, CMOS ICs are also becoming a contender in this frequency range due to the steady scaling-down of the gate length [3], [19], [26], [27]. Some of the Si-RF ICs reported to date utilize circuit designs and fabrication processes to overcome the drawbacks resulting from Si substrate loss—for example, silicon on insulator (SOI) or silicon on sapphire (SOS) [1], [2], [4], [8]–[10], [15], [16], high resistivity substrate [4]–[6], [10], [15], [18], thick metallization [5], [6], thick interconnects on a thick, low dielectric constant passivated film such as polyimide [26], and so on. From the viewpoint of low-cost and high-level integration with baseband LSIs, however, it is considered that the standard bulk CMOS technology without extra processing steps is the best candidate for realizing RF transceivers for use in short-range wireless communications such as Bluetooth and wireless LANs.

The standard bulk CMOS technology often provides an RF front-end with significant degradations in RF performance—especially the large insertion loss of a transmit/receive(T/R)-switch (SW) and low small-signal gain for a power amplifier (PA) and a low-noise amplifier (LNA). The reason for these performance degradations is that bulk CMOS utilizes a low-resistivity substrate of 0.01 to 10 Ωcm and has no extra processing steps as previously mentioned, thereby degrading the quality factors (Q-factors) of on-chip matching elements such as spiral inductors and polysilicon to polysilicon capacitors (PPCs). Therefore, the circuit-design techniques applicable even to the standard bulk CMOS processes are essential for implementing fundamental RF building circuits of the front-end.

This paper describes the design and experimental results of a 1.8-V operation single-chip CMOS T/R-MMIC front-end for 2.4-GHz-band short-range wireless communications such as Bluetooth and wireless LANs. The IC contains a PA, a T/R-SW, and an LNA, integrating almost all matching elements on the chip. We have introduced two new circuit-design techniques into the IC in order to improve the RF performances as much as possible even in the case when the IC is fabricated using the standard bulk CMOS processes. One is the derivation of the optimum gate width of the SW to minimize the insertion loss based on small-signal equivalent circuit analysis. The analytical expression to calculate the optimum gate width is derived and then its validity is verified with the simulation or experiments. The other is the experimental revelation of the advantages of

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interdigitated capacitors (IDCs) over conventional PPCs and the successful application of the IDCs to the LNA and PA. It is demonstrated that in CMOS processes of 0.18 μm or less, the IDCs are feasible matching elements and suitable for realizing a higher gain.

The prototype IC, intended for the Bluetooth Class III specifications, was fabricated using a standard 0.18-μm bulk CMOS technology. The IC achieves the following sufficient characteristics for practical wireless terminals: a 5-dBm transmit power, a 19-dB associated gain, an 18-mA operating current for the PA, a 1.5-dB insertion loss, more than 24-dB isolation, an 11-dBm power handling capability for the SW, a 4.5-dB noise figure, a 7.5-dB associated gain, and an 8-mA operating current for the LNA.

The organization of the paper is as follows. Section II provides a brief description of the chip architecture and FET characteristics. Section III describes the design and experimental results for the SW, LNA, and PA while focusing on the switch gate-width optimization and a comparison between the IDCs and PPCs RF characteristics.

II. Chip Architecture and FET Characteristics

A chip micrograph of the single-chip T/R-MMIC front-end with its functional layout is shown in Fig. 1. The IC consists of a PA, an SW, and an LNA, and was designed to meet the target specifications (Table I) based on 2.4-GHz-band Bluetooth Class III standards. In Table I, the measured electrical properties of the Si-CMOS T/R-MMIC front-end fabricated in this study are also summarized. The primary purpose of this study is to prove the validity of the circuit-design techniques introduced into the IC by the simulation or experiments. Therefore, as a detailed description appears in Section III, each circuit consists of only fundamental RF circuits including the on-chip matching elements and does not include additional bias circuits for implementing temperature compensation. Because transmit and receive slots in turn switch in the Bluetooth system, transmit and receive paths are activated alternately. Therefore, an isolation level of more than 20 dB in the SW provides a steady operation for the MMIC. The target output power of the PA was set at 5 dBm taking into account the estimated insertion loss across the SW and bandpass filter (BPF). Regarding the LNA, the target gain and noise figure can meet easily the overall receiver sensitivity of -70 dBm required in the Bluetooth specification. This sensitivity is much more insensitive than that required in current cellular phone systems. Under the condition of a 2-dB switch loss and a 3-dB BPF loss, an overall receiver's sensitivity of -74 dBm can be realized using a down-mixer having a gain of 7 dB and a noise figure of 20 dB. This is because in the Bluetooth system the gain of an IF receiver including a G_m -C BPF, which is usually designed so as to have high gain, dominates the overall receiver sensitivity. The supply voltage for the IC is a 1.8-V single supply due to the maximum drain-to-source voltage limitation of the 0.18-μm MOSFETs. The input/output terminals of each circuit are made available to off-chip and are matched to 50 Ω for conducting independently accurate RF measurements. The chip size including all bonding pads is 2.5 mm$\times$1.0 mm, and the occupied areas of each circuit are as follows: 1.25×1.0 mm^2 for the PA, 0.45×1.0 mm^2 for the SW, and 0.80×1.0 mm^2 for the LNA.

The 0.18-μm bulk CMOS technology used for the IC includes four-level Aluminum (Al) interconnects and PPCs. In addition to the PPCs, the IDCs comprising the interconnect lines are employed as matching elements. The substrate resistivity is less than 10 Ωcm, and each Al interconnect-layer thickness is as thin as 0.5 or 0.6 μm. The typical dc characteristics of n-MOS are a 0.6-V threshold voltage, a 450-mS/mm maximum transconductance, and a 1.8-V maximum operating drain-to-source voltage. Biased with a 1-V drain-to-source voltage and a 20-mA drain current, a 100-μm gate-width n-MOSFET exhibits a 50-GHz transition frequency and a 18.5-dB maximum stable gain at 2.0 GHz.

III. Circuit Designs and Experimental Results

A. T/R-Switch

A T/R-switch (SW) is one of fundamental RF front-end building circuits for realizing a wireless transceiver. Both the insertion loss and isolation are very important characteristics to determine the switch transfer performances. GaAs SWs are often used in practical wireless transceivers because the insertion loss of GaAs SWs is much lower than that of Si-CMOS ones [20], [21]. The large insertion loss of the Si SWs is mainly due to the low-resistivity substrate and large on-state resistance of the MOSFETs [3], [14], [15].

Two typical circuit configurations for Si-CMOS SW, the series- and shunt/series-type SWs, are shown in Fig. 2(a) and (b). In this figure, the FETs, M_1 and M_2, form the series arms and M_5 and M_6 form the shunt arms. The FETs, M_3 and M_4, comprising the control circuit, work in a complementary fashion, consuming no drain current. In the case of the GaAs-SWs, the substrate parasitics can be neglected in the 2.4-GHz band. Therefore, enlarging the gate width of M_1 and M_2 leads to a tradeoff between the reduction of the on-state resistance and the increase in the off-state capacitance. In other words, a tradeoff exists between the reduction of the insertion loss and the degradation of isolation.

In contrast, in the case of Si-SWs fabricated on a low-resistivity substrate, enlarging the gate width of M_1 and M_2 reduces the on-state resistance, thus improving the insertion loss. On the other hand, the enlargement increases the substrate parasitics of M_1 and M_2, leading to the degradation of the insertion loss as well as the isolation. This property implies that a proper gate width can provide the minimum insertion loss for the Si-SWs on the low-resistivity substrate. In the Si-switch design, it is, therefore, essential to determine the optimum gate width which provides the minimum insertion loss and sufficient isolation level. This subsection first describes the small-signal equivalent analysis of the SW and the analytical expression to calculate the optimum gate width based on the analysis. The validity of the analysis is subsequently verified by simulated and experimental results.

The circuit schematics and their on- and off-state equivalent circuits for series and shunt arms used for the SW are illustrated

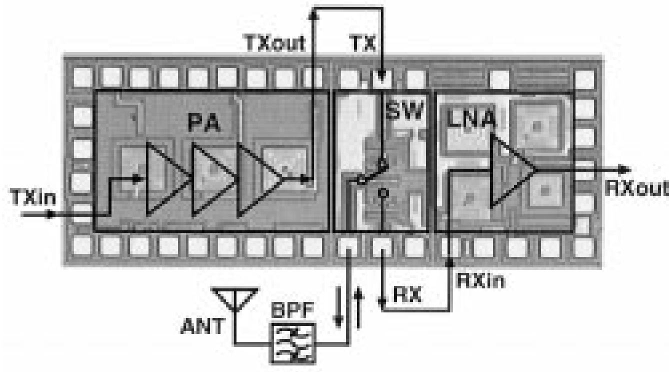


Fig. 1. Chip micrograph of the single-chip T/R-MMIC front-end with its functional layout.

in Fig. 3. In this figure, the resistances R_s and R_{s2} and capacitances C_s and C_{s2} represent parasitic resistances and capacitances resulting from a low-resistivity substrate. The resistances R_a and R_{a2} and inductances L_a and L_{a2} are the on-state resistances and parasitic inductances. The resistances R_b and R_{b2} and capacitances C_b, C_{b0}, C_{b1}, and C_{b2} denote the off-state resistances and capacitances. Table II lists an example of the equivalent circuit parameters derived from the measured S parameters for the 200-μm gate-width series and shunt arms.

Fig. 4(a) and (b) shows the small-signal equivalent circuits for the series- and the shunt/series-type SWs comprising the circuit schematics of Fig. 3. Both figures represent the equivalent circuits in transmit mode. As shown in Table II, a low-resistivity substrate produces an R_s of 165 Ω and a $1/\omega C_s$ of about 390 Ω for the 200-μm gate width series arm at 2.4 GHz. These parasitics cannot be neglected for the usual 50-Ω system because they cause a relatively large loss. Therefore, it is easily predicted that the shunt/series-type SW basically has a larger insertion loss than the series-type one, as will be described later.

To calculate the transfer characteristics for the series-type SW and determine the optimum gate width, we can simplify the circuit schematics shown in Fig. 4(a) under the conditions that $1/\omega C_b$, $1/\omega C_{b0} \gg Z_o\ (= 50\ \Omega)$, and $\omega L_a \ll Z_o$. The resultant schematics are shown in Fig. 4(c) and (d). Based on the simplified schematics, we can calculate both the insertion loss between the TX and ANT ports and the isolation level between the TX and RX ports. From Fig. 4(c), the insertion loss, $I_{\rm L}$, for the series-type SW is expressed by (1), shown at the bottom of the page, where $Q = 1/\omega C_s R_s$ and $Z_o = 50\,\Omega$.

We should note that approximations such as $\omega C_s R_s \ll 1$ or $\omega C_s R_s \gg 1$ [14] are not appropriate for the derivation of this equation. The reason is that the parasitics, R_s and $1/\omega C_s$, on the low-resistivity substrate are comparable with Z_o, and the proper balance between these parasitics and on-state resistance yields the minimum insertion loss. Assuming that R_s and R_a are inversely proportional to the gate width W for M_1 and M_2, and C_s is proportional to W, $I_{\rm L}$ is rewritten as follows:

$$I_{\rm L} = \frac{2Z_o\left(1+Q_s^2\right)}{\mathrm{sqrt}\left(AW^2+\frac{B}{W^2}+CW+\frac{D}{W}+E\right)} \tag{2}$$

$$A = \left(\frac{Z_o^2}{K_2}\right)^2 \left\{(2K+3)^2+9Q_s^2\right\} \tag{3}$$

$$B = K_1^2\left(1+Q_s^2\right)^2 \tag{4}$$

$$C = 2\left(\frac{Z_o^2}{K_2}\right)Z_o\Big[(2K+3)\left\{2(1-Q_s^2)+3K\right\} + 3Q_s(3K+4)\Big] \tag{5}$$

$$D = 2Z_oK_1\Big[\left(1-Q_s^2\right)\left\{2\left(1-Q_s^2\right)+3K\right\} + 2Q_s^2(3K+4)\Big] \tag{6}$$

$$E = Z_o^2\Big[\left\{2\left(1-Q_s^2\right)+3K\right\}^2+2K(2K+3)\left(1-Q_s^2\right) + Q_s^2(3K+4)+12Q_s^2K\Big] \tag{7}$$

where K_1 and K_2 are constants, $R_a = K_1/W$, $R_s = K_2/W$, and $K = K_1/K_2$. In the denominator of (2), the following relationship is satisfied over a practical parameter range such as listed in Table II:

$$A\cdot W^2+\frac{B}{W^2} \ll C\cdot W+\frac{D}{W}. \tag{8}$$

The optimum gate width W_m is approximately derived from the right term of (8) using the relationship between the arithmetic and geometric means

$$W_m \approx \mathrm{sqrt}\left(\frac{D}{C}\right). \tag{9}$$

Thus, (9) reveals that there is a proper gate width W_m, which provides the minimum insertion loss for the Si-switch on the low-resistivity substrate.

Based on Fig. 4(d), the isolation level $I_{\rm so}$ for the series-type SW is also expressed by the following equations:

$$I_{\rm SO} = \left|\frac{-4Z_o\omega C_bR_s^2Q_s - j2Z_oR_s^2\omega C_b(1-Q_s^2)}{F}\right| \tag{10}$$

$$\begin{aligned} F = {} & 2R_s^2(1-Q_s^2)+5Z_oR_s+3Z_o^2 \\ & + 2\omega C_bZ_oR_sQ_s(R_s+2Z_o) \\ & - jR_sQ_s(4R_s+5Z_o)+j\omega C_bZ_oR_s \\ & \times\left\{R_s(1-Q_s^2)+Z_o\right\}. \end{aligned} \tag{11}$$

$$I_{\rm L} = \left|\frac{2Z_oR_s^2\left\{\left(1-Q_s^2\right)-j2Q_s\right\}}{2Z_o^2R_a+3Z_o(R_a+Z_o)R_s+(R_a+2Z_o)R_s^2\left(1-Q_s^2\right)-jR_sQ_s\{3Z_o(R_a+Z_o)+2(R_a+2Z_o)R_s\}}\right| \tag{1}$$

TABLE I
TARGET SPECIFICATIONS AND ELECTRICAL PROPERTIES FOR SINGLE-CHIP T/R-MMIC FRONT-END

		Target spec.	Measured results
Operating frequency		2.4 GHz-band	2.4 GHz-band
Supply voltage		1.8 V (single)	1.8 V (single supply)
T/R-switch	Insertion loss	< 2dB	1.5 dB (TX and RX modes)
	Return loss	> 10 dB	11 dB (TX and RX modes)
	Isolation	> 20dB	24 dB (TX-RX in TX mode) 24 dB (ANT-TX in RX mode)
	Power handling capability	> 5dBm	11 dBm (Vcnt = 0 V)
	Current	≈ 0 mA	≈ 0 mA
PA	Output power(=P_{-1dB})	≥5 dBm*	5 dBm
	Power gain	> 18dB	19 dB
	Current	< 20mA	18 mA
LNA	Small-signal gain	> 7dB	7.5 dB
	NF	< 6dB	4.5 dB
	Current	< 10mA	8 mA

*: Target output power is determined taking into account a 2-dB switch loss and a 3-dB BPF loss.

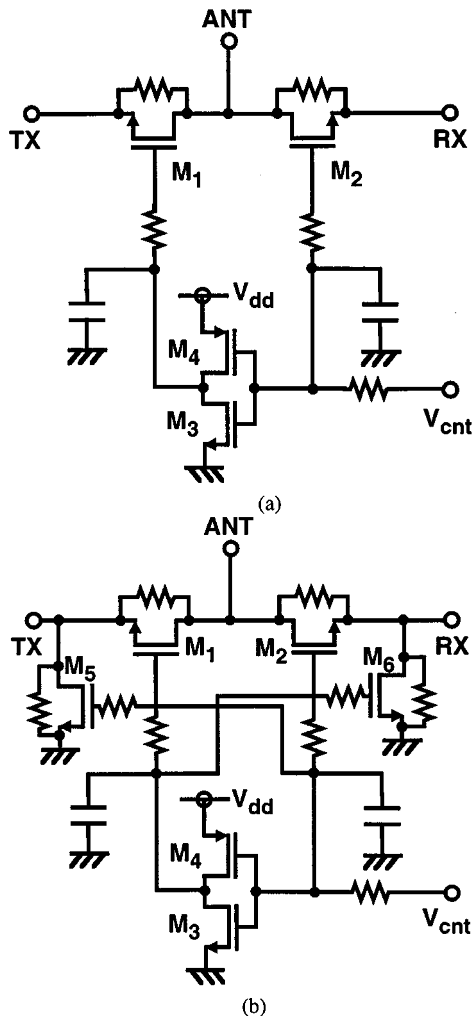


Fig. 2. Circuit configurations for T/R-switches: (a) series type and (b) shunt/series type.

The simulated and measured transfer characteristics for the series-type SW are shown in Fig. 5. The calculated insertion loss and isolation for the series-type SW, based on (2), are plotted in this figure. The simulated characteristics of the shunt/series-type SW are also compared with those of the series-type SW. The simulation was implemented using a commercial microwave simulator, Agilent-ADS. The measured transfer characteristics were obtained from the series-type SW fabricated as stand-alone circuits. The insertion loss of the series-type SW is lower than that of the shunt/series-type one, as previously predicted, while the isolation of the shunt/series-type SW is much higher than that of the series-type one. The calculated result shows good agreement with the simulated one, indicating that the approximation used for the derivation of the equations is valid. The insertion loss is minimized at $W = 200$ μm, and this gate width is almost equal to the gate width of 188 μm calculated from (9). For the 200-μm gate width, the simulated insertion loss and isolation level are -1.5 and -24 dB, respectively. Moreover, these characteristics at $W = 200$ μm adequately satisfy the target specifications listed in Table I. Based on these results, we integrated the series-type SW with a gate width of 200 μm on the single-chip IC. As can be seen in this figure, both the simulated and measured characteristics for the series-type SW are in good agreement with each other, proving that the simple equations (1)–(11) are useful for predicting the transfer characteristics of the series-type SW.

Fig. 6(a) and (b) shows the measured frequency response and power handling capability, respectively, for the series-type SW incorporated into the IC in transmit mode. The SW delivers a -1.5-dB insertion loss, an -11-dB return loss, and a -24-dB isolation at 2.4 GHz. The successful optimization yields a 1.5-dB lower insertion loss than that of the 0.8-μm MOS switch [14], and 3.7 dB lower than that of the 0.25-μm MOS switch [3], though the loss is slightly higher than that of the 0.2-μm SOI/SIMOX switch with a high resistivity substrate [15]. In the receive mode, the same characteristics as those in transmit mode are obtained. As shown in Fig. 6(b), biased with a 1.8-V control voltage, the SW achieves a power handling capability of 11 dBm at a 0.2-dB gain compression point ($P_{-0.2\text{dB}}$),

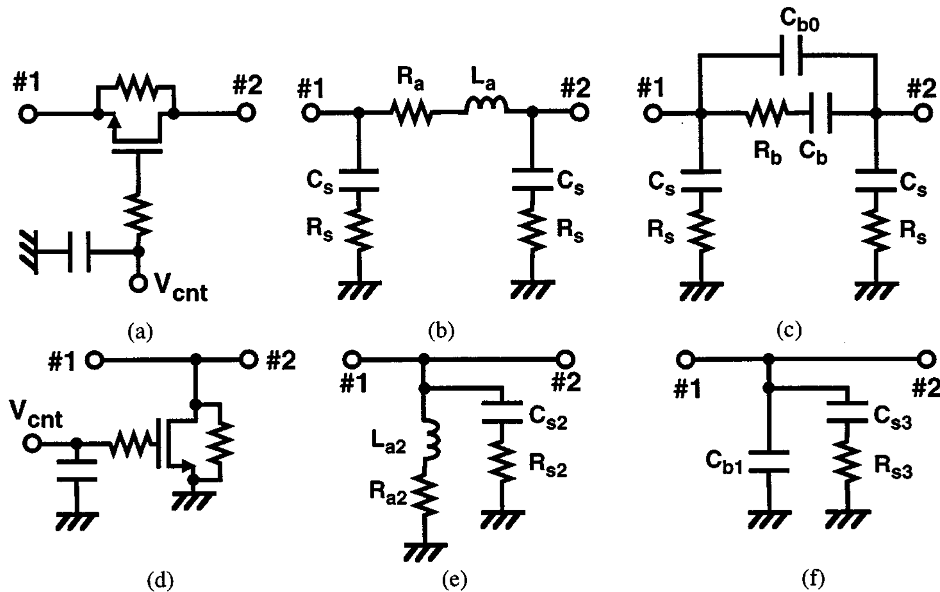


Fig. 3. Circuit schematics and their on- and off-state equivalent circuits for series and shunt arms: (a) circuit schematic, (b) on-state circuit, (c) off-state one for series arm, and (d) circuit schematic, (e) on-state circuit, and (f) off-state one for shunt arm.

TABLE II
EXAMPLE OF THE EQUIVALENT CIRCUIT PARAMETERS DERIVED FROM THE MEASURED S PARAMETERS FOR THE 200-μm GATE WIDTH SERIES AND SHUNT ARMS

Series arm					Shunt arm			
ON		OFF			ON		OFF	
R_a [Ω]	6.5	R_b [Ω]	10^5		R_{a2} [Ω]	4.5	R_{a3} [Ω]	165
L_a [nH]	0.07	C_b [pF]	0.1		L_{a2} [nH]	0.08	C_{s3} [pF]	0.20
R_s [Ω]	165	C_{b0} [pF]	2.0		R_{s2} [Ω]	7.0	C_b [pF]	6.5
C_s [pF]	0.17	R_s [Ω]	165		C_{s2} [pF]	0.80		
		C_s [pF]	0.17					

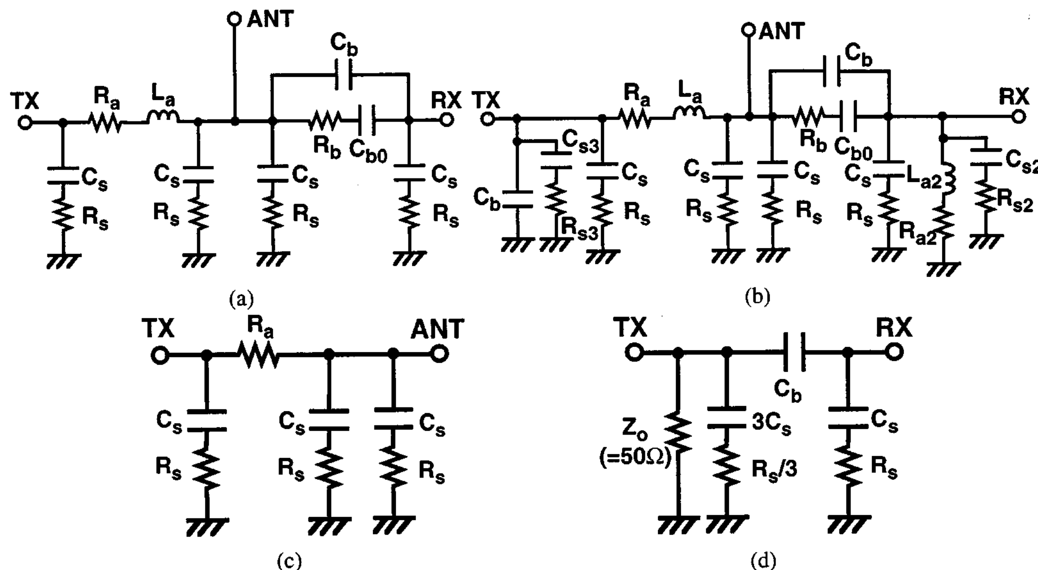


Fig. 4. Equivalent circuits for T/R-switch in transmit mode: (a) series-type and (b) shunt/series-one, and simplified equivalent circuits for the series-type switch to calculate transfer characteristics in transmit mode: (c) insertion loss between TX and ANT ports and (d) isolation between TX and RX ports.

and this is almost equal to the value of 11.5 dBm predicted by the formula mentioned in [29] and [30]. Thus, all the measured transfer characteristics sufficiently cover the target specifications in Table I.

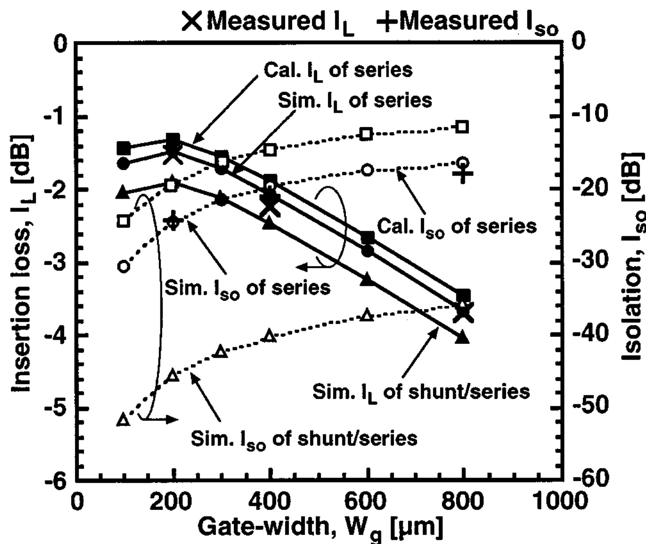
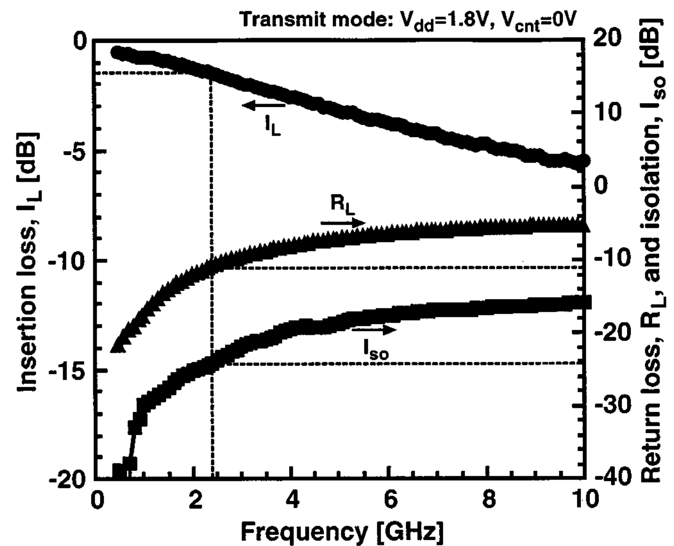
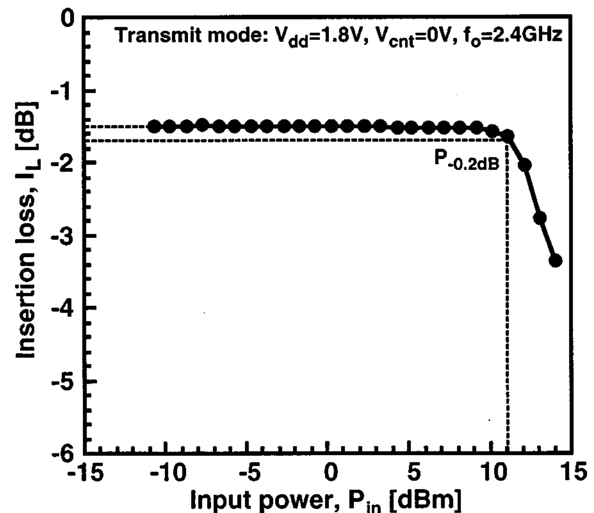


Fig. 5. Simulated and measured transfer characteristics for a series-type T/R-switch. In the figure, the characteristics calculated using (2) are plotted. Simulated characteristics of the shunt/series-type switch are also compared with those of the series-type switch.



(a)



(b)

Fig. 6. Measured frequency response for a T/R-switch incorporated into the IC in transmit mode. (a) Frequency response. (b) Power handling capability.

B. Interdigitated Capacitors

Si-MMICs often use spiral inductors and PPCs as typical lumped matching elements. It seems very difficult to improve the Q-factors of spiral inductors in the standard bulk CMOS processes which have no extra processing steps and use a low-resistivity substrate. For example, a 5-turn, 10-μm-line-wide, 2-μm -line space inductor with the dimensions of 200 μm × 200 μm exhibits the low Q-quality factor of 3–4 in the 2-GHz band. This low Q-factor results from the low-resistivity substrate. On the other hand, the scaling-down of the design rule, for example, from 0.35 μm to 0.18 μm, allows the substitution of IDCs for PPCs as capacitive lumped elements, thereby leading to an improvement in the small-signal gain for the LNA and the PA. In this subsection, we describe the advantages of IDCs over conventional PPCs and experimentally demonstrate that IDCs are feasible matching elements in CMOS processes of 0.18 μm or less.

The layout schematics and their equivalent circuits for an IDC and a PPC are shown in Fig. 7(a) and (b). In each figure, a cross section is illustrated below its top view. The IDC consists of three layer interconnects (AL1 to AL3) and thru-hole arrays. The interconnect linewidth and space are laid out using the minimum design rule of the 0.18-μm CMOS processes. The PPC comprises a silicided polysilicon layer (upper conductor), a non-silicided polysilicon one (lower conductor), and interconnect lines with thru-holes. The dielectric film between the polysilicon layers is as thin as a few hundred ångströms. The high resistivity of the polysilicon layers causes a significantly large loss in the matching circuit with the PPCs, though this loss may be considerably reduced in the case where both polysilicon layers of the PPC are silicided or one polysilicon layer is silicided for a metal to silicided-polysilicon capacitor, such as MIM capacitors, as made available in some CMOS processes. With regard to the occupied area, on the other hand, the PPC occupies a relatively smaller area than the IDC for the same capacitance. We deem that the large area of the IDC is not significant, because in a Si RF circuit design the performance is often more important than the occupied chip area.

To compare the RF characteristics of an IDC with those of a PPC, we laid out and tested several different kinds of IDCs and PPCs. In the layout, the aspect ratio of L and W shown in Fig. 7 was kept constant for the IDCs and PPCs so as to compare the equivalent series resistance as precisely as possible. The equivalent circuits shown in Fig. 7(a) and (b) were used for modeling the IDC and PPC. An example of the extracted circuit parameters for the IDC and PPC, which correspond to about 2-pF capacitors, is listed in Table III. The extraction was carried out as follows. The bonding pad parasitics were first deembedded from the measured S-parameters of the IDC and PPC test patterns by using an open bonding pad pattern, and then the equivalent circuit parameters were fit to the deembedded measured data using Agilent-ADS. Therefore, the measured results presented in this subsection, including Table III, do not include basically the ef-

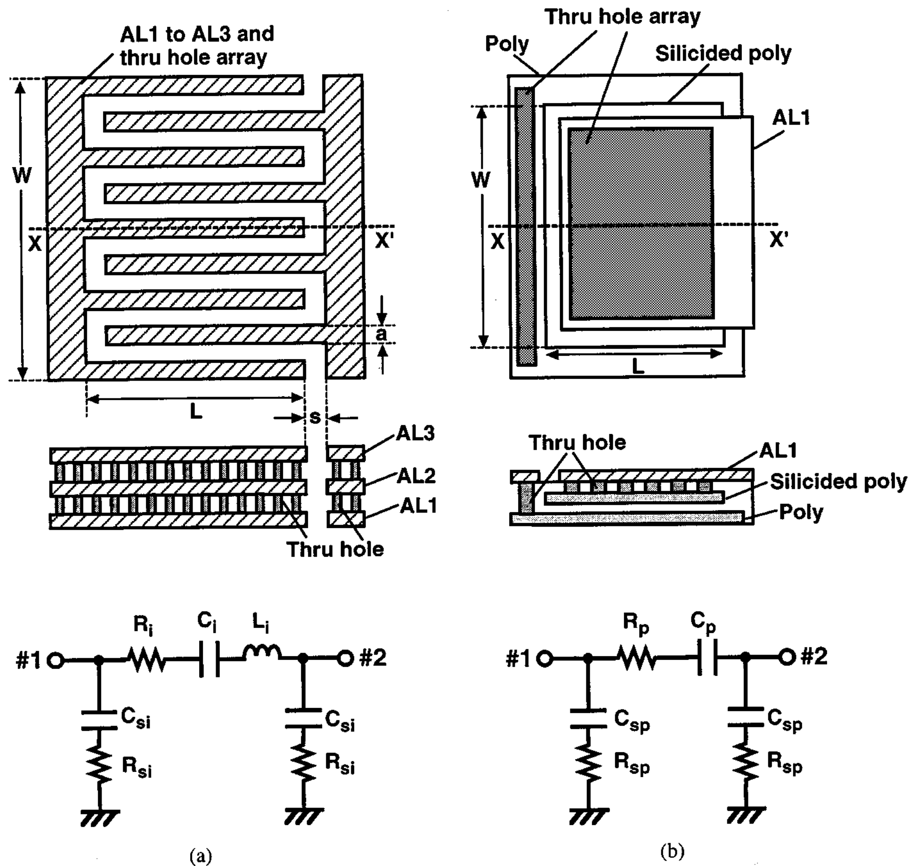


Fig. 7. Layout schematics and their equivalent circuits for: (a) an IDC and (b) a PPC. In each figure, a cross section is shown together with its top view.

TABLE III
EXAMPLE OF THE EXTRACTED CIRCUIT PARAMETERS FOR THE IDC AND PPC

	IDC		PPC
Area [μm^2]	3600	Area [μm^2]	1085
C_i [pF]	2.1	C_p [pF]	2.2
R_i [Ω]	1.5	R_p [Ω]	15.5
L_{si} [nH]	0.12		
R_{si} [Ω]	800	R_{sp} [Ω]	1318
C_{si} [pF]	0.052	C_{sp} [pF]	0.03

fect of the bonding pad parasitics. Fig. 8 compares the equivalent series capacitance and resistance of the IDCs with those of the PPCs. As can be seen in Table III and Fig. 8, the series resistance of the IDCs is about one-tenth as low as that of the PPCs under the same capacitance condition, while the occupied area of the IDCs are approximately three times larger than that of the PPC. This low series resistance is very effective in building low-loss on-chip matching circuits. The dispersion of the IDC's equivalent capacitance due to process fluctuations is less than 10%, indicating that the IDCs are sufficiently applicable to an RF matching element.

The measured transfer characteristics, maximum available gain (MAG) and S_{21}, for the IDC and PPC are depicted in Fig. 9(a) and (b), respectively. In Fig. 9(a) and (b), a small dip in the 2–4-GHz band merely results from the fact that the unexpected resonance of the open bonding pad pattern used for the PPC could not be completely deembedded from the measured S-parameters. Therefore, this resonance is not related to the intrinsic characteristics of the PPC. As depicted in Fig. 9, the IDC produces a lower loss than that of the PPC by more than 0.5 dB over a frequency range from 2 to 6 GHz. Thus, it

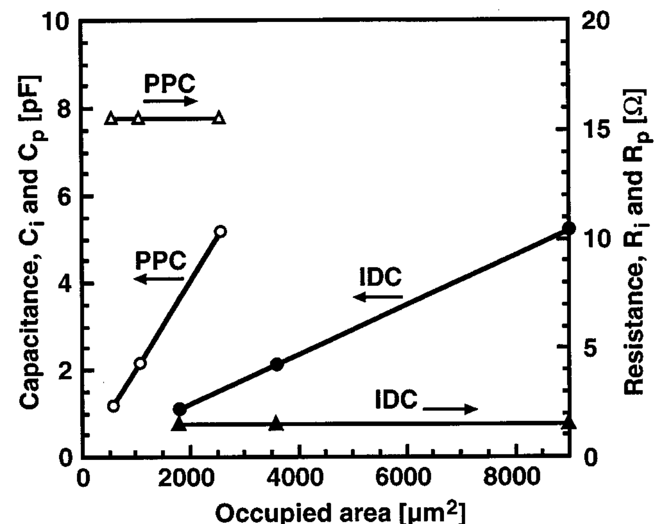
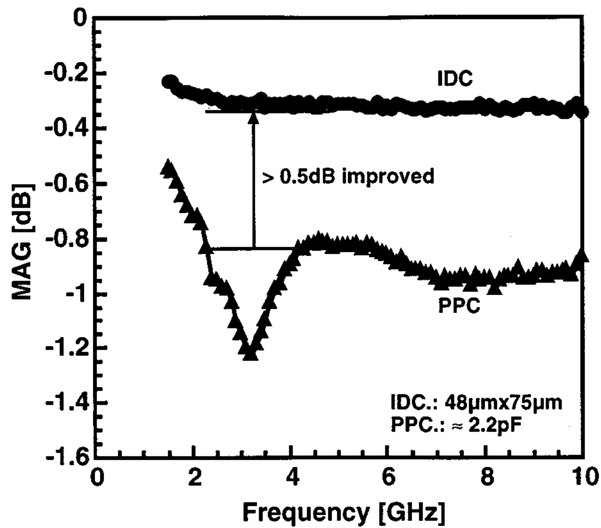
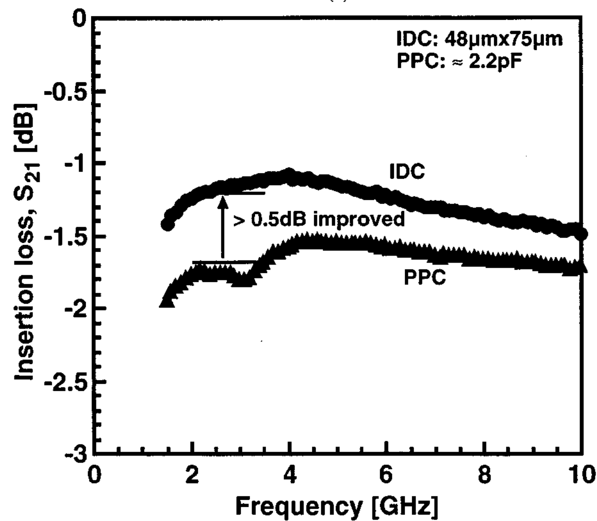


Fig. 8. Comparison of the equivalent series capacitance and resistance between the IDCs and PPCs.



(a)



(b)

Fig. 9. Measured transfer characteristics for the IDC and PPC. (a) MAG versus frequency and (b) S_{21} versus frequency.

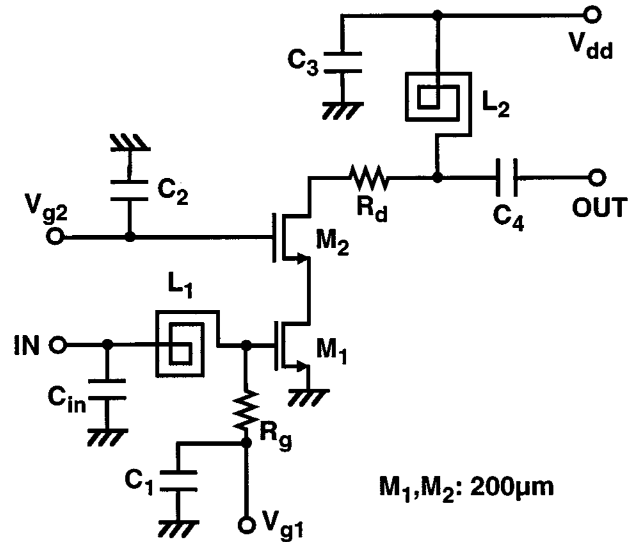


Fig. 10. Circuit schematic for the LNA.

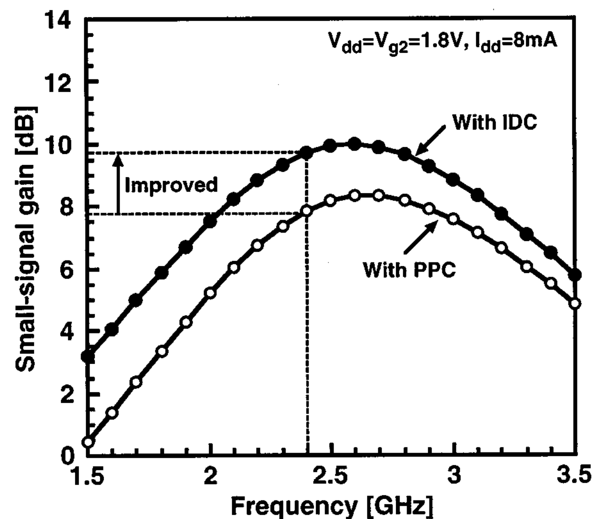


Fig. 11. Simulated frequency response comparison between the LNA with the IDC (solid circles) and the PPC (open circles).

is expected that the low loss characteristics of the IDC reduces the matching loss in practical circuits, thereby improving the overall small-signal gain.

C. Low-Noise Amplifier

The LNA employs cascode topology to realize the high gain in the high-frequency band of 2.4 GHz, as shown in Fig. 10. The gate widths of the FETs, M_1 and M_2, are both 200 μm. All the matching elements are formed on-chip, and all of the capacitors, C_1 to C_4, are formed using the IDCs. The spiral inductors, L_1 and L_2, utilize a patterned ground shield structure [31]. The resistance R_d is added to the output line for more stable operation.

A simulation was performed to investigate the gain characteristics of the LNA with the IDCs and those with the PPCs. The simulated result shown in Fig. 11 indicates that the gain of the LNA with the IDCs is about 2 dB higher than that with the PPCs, which reveals the effectiveness of the IDCs in the matching circuits. The influence of the IDCs dispersion to the overall gain was also investigated. As a result, we found that the IDCs capacitance dispersion of less than 10% causes only gain dispersion of less than ± 0.1 dB at 2.4 GHz, thus proving that the IDCs are sufficiently applicable to an RF matching element, as previously expected. One of the major reasons why the LNAs gain characteristics are less affected by the IDCs capacitance dispersion may be due to the fact that low Q-spiral inductors dominate the LNAs frequency response.

Based on the simulated result, we designed and fabricated only an MMIC front-end incorporating the LNA with the IDCs onto the MMIC chip. Fig. 12(a) and (b) shows the measurement results of the LNA in the IC. As shown in this figure, the LNA exhibits good input and output return losses of -10 dB and -16 dB at 2.4 GHz. A 4.5-dB noise figure and a 7.5-dB associated gain are achieved at 2.4 GHz when biased with 1.8 V and 8 mA. The noise figure and gain are sufficient for the target specifications shown in Table I and allow practical operation in short-range wireless applications. In the case where this LNA is employed for other applications such as cellular systems, an

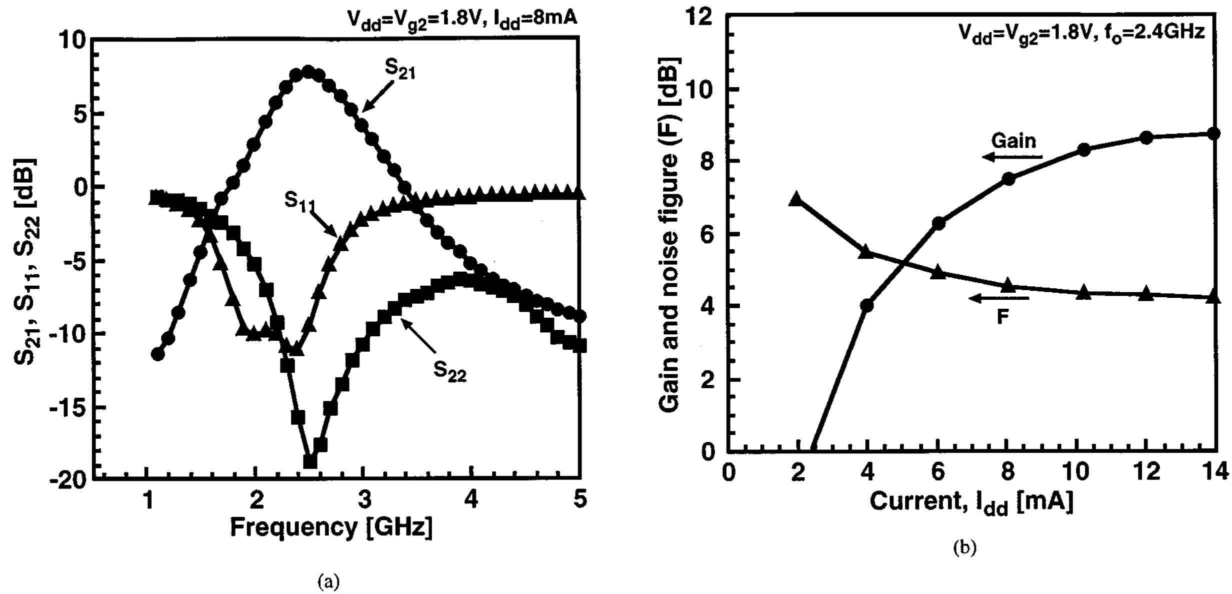


Fig. 12. Measured characteristics for the LNA in the IC. (a) Frequency response. (b) Noise figure and associated gain versus drain current.

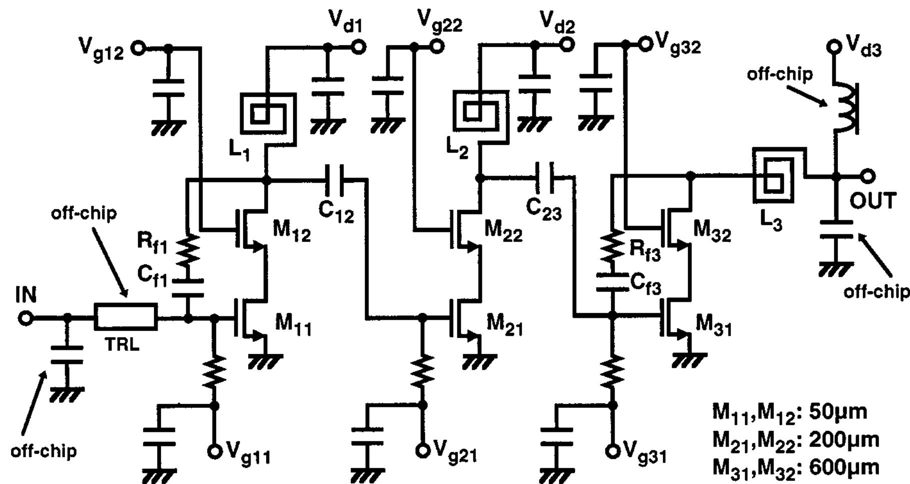


Fig. 13. Circuit schematic for PA.

off-chip input matching circuit may be required for achieving better noise figure with lower current consumption, because the minimum noise figure of the FETs, M_1 and M_2, is as low as 1.5 dB and the relatively large loss occurs in the spiral inductor of the on-chip input matching circuit.

D. Power Amplifier

During a gain compression operation, the maximum drain-to-source voltage of a PA often reaches about twice the dc drain-to-source voltage, even in the case of class A operation. The maximum operating drain-to-source voltage of the 0.18-μm FETs is also as low as 1.8 V, the same as the supply voltage. To suppress the maximum drain-to-source voltage within 1.8 V on a 1.8-V single voltage supply and realize a higher gain in the high-frequency band of 2.4 GHz, cascode topology is employed for each stage, as shown in Fig. 13. The PA utilizes a three-stage configuration and includes almost all matching and decoupling elements on the chip. The patterned ground shield structure is used for the spiral inductors, L_1 to L_3 [31], and IDCs are used for all of the on-chip capacitors including the interstage capacitors, C_{12} and C_{23}. The input matching circuit and a few elements comprising the output matching circuit are fabricated off the chip to reduce the chip size and matching loss. This topology produces flexibility between the output power and efficiency matching conditions as well as chip-size reduction. The FET gate widths of the final stage, M_{31} and M_{32} as large as 600 μm, are adopted for delivering an output power of more than 5 dBm at a 1-dB gain compression point $(P_{-1\text{dB}})$. The *RC* feedback circuits, (R_{f1}, C_{f1}) and (R_{f3}, C_{f3}), attached on the first and final stages can offer easy input matching and enhance the overall circuit stability.

In order to verify the gain enhancement of the IDCs, the frequency response of a PA using IDCs was compared to that of one using PPCs by simulation. The simulated result is shown in Fig. 14, indicating that the gain of the PA with the IDCs is about 3.5 dB higher than that with the PPCs, as expected in the previous subsection. We also investigated the deviations

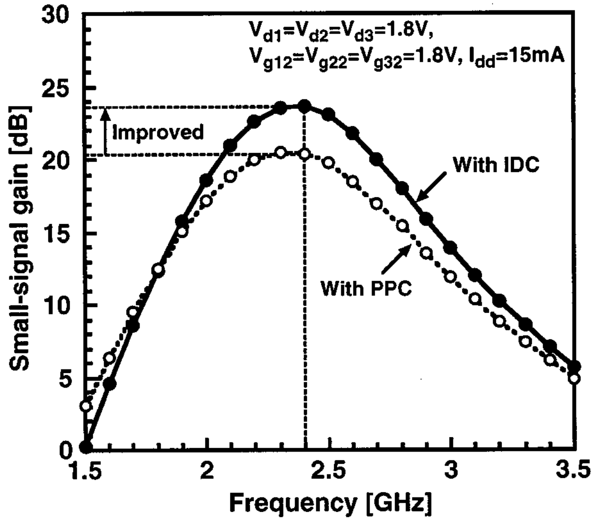


Fig. 14. Simulated frequency response comparison between the PA with IDC and PPC.

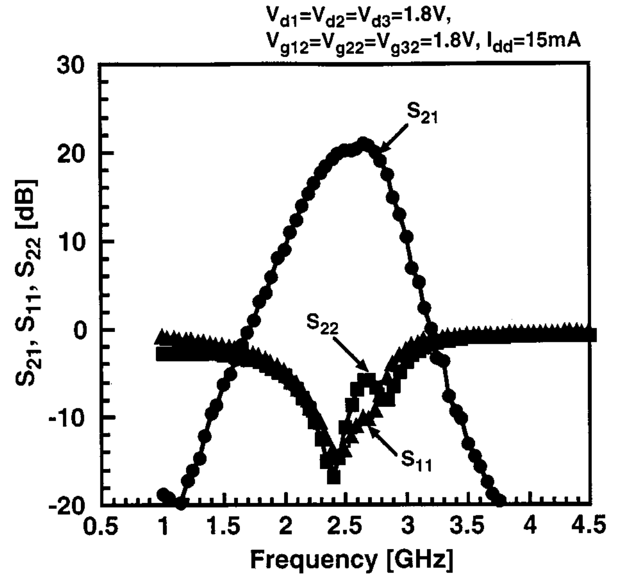
of the overall gain and $P_{-1\mathrm{dB}}$ caused by the IDCs dispersion. The simulation results showed that a gain deviation is less than ± 0.2 dB and a $P_{-1\mathrm{dB}}$ deviation is less than ± 0.05 dBm under the condition of less than 10% IDCs capacitance dispersion and a 2.4-GHz operating frequency. These deviations are sufficiently small, because low Q-spiral inductors mainly dominate the PAs characteristics.

Based on the simulated result, only the PA with the IDCs was incorporated into the single-chip IC. Fig. 15(a) shows the measured frequency response of the PA in the IC, where the bias condition was a 1.8-V voltage supply and a 15-mA drain quiescent current (class AB operation). The PA offers good input and output return losses of -14 dB at 2.4 GHz. The measured power characteristics for the PA is also shown in Fig. 15(b) at 2.4 GHz and 1.8 V. The PA delivers a 5-dBm $P_{-1\mathrm{dB}}$, with an associated gain of 19 dB and a current consumption of 18 mA. A power-added efficiency (PAE) of about 10% is obtained at a $P_{-1\mathrm{dB}}$, while at a 5-dB gain compression point the PA is capable of delivering an output power of more than 9 dBm and a PAE of more than 16%. The transmit power, power gain, and current consumption are sufficient for such short-range wireless applications, as listed in Table I.

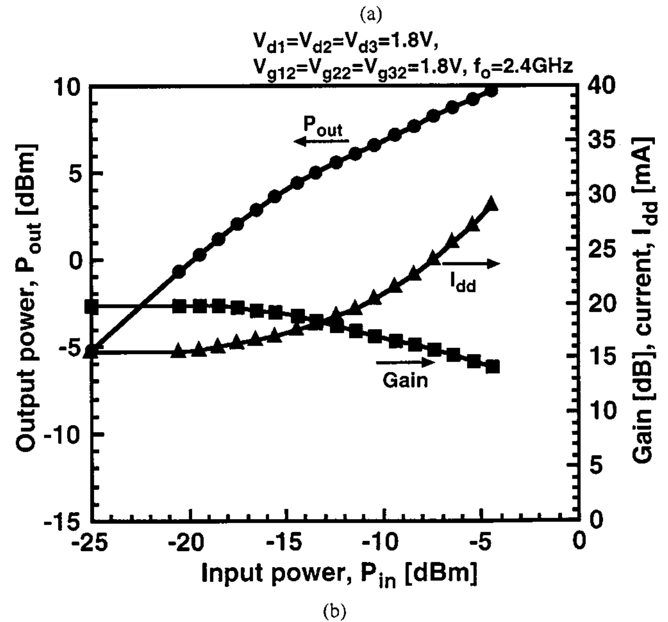
Finally, the main electrical properties of the Si-CMOS T/R-MMIC front-end are summarized in Table I, as previously shown in Section II. Both the analytical optimization of the SW and successful use of the IDC in the PA and LNA enable the IC to deliver sufficient performances for 2.4-GHz-band wireless applications, despite the fact that it was fabricated using standard bulk CMOS technology. To our knowledge, this MMIC including a T/R-switch and a PA is the first to be reported in a 2.4-GHz-band Si-MMIC front-end fabricated using 0.18-μm standard bulk CMOS technologies which use a low-resistivity substrate and need no extra processing steps.

IV. Conclusion

We have demonstrated the design and experimental results for a 1.8-V operation, single-chip CMOS MMIC front-end



(a)



(b)

Fig. 15. Measured characteristics for the PA in the IC: (a) frequency response and (b) output power characteristics.

for 2.4-GHz-band short-range wireless communications such as Bluetooth and wireless LANs. To improve the RF performances, we have incorporated the new circuit-design techniques into the IC—analytical optimization of the T/R-switch and successful application of the IDCs to the PA and LNA. The resultant insertion loss of the T/R-switch is the lowest of the switches ever reported which were fabricated using standard bulk Si-CMOS processes. In addition, it is experimentally demonstrated that IDCs are suitable for realizing low-loss on-chip matching elements. Thus, it is verified that these techniques enable the IC to deliver sufficient performances for practical short-range wireless applications, despite the fact that it was fabricated using standard bulk CMOS technology.

We expect that the circuit-design techniques presented here will help with Si-RF front-end circuit design and will contribute to the realization of low-cost, small-size wireless terminals for personal communications.

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REFERENCES

[1] M. Harada and T. Tsukahara, "Monolithic 2 GHz and 4–6 GHz low noise amplifiers fabricated on SIMOX wafer," in *Extended Abstract of the 1997 Int. Conf. on Solid State Devices and Materials*, 1997, pp. 132–133.

[2] ——, "Low dc power Si-MOSFET L- and C-band low noise amplifiers fabricated by SIMOX technology," *IEICE Trans. Electron.*, vol. E82-C, no. 3, pp. 553–558, March 1999.

[3] M. Madihian, L. Desclos, and T. Drenski, "CMOS RF IC's for 900 MHz-2.4 GHz band wireless communication networks," in *IEEE RFIC-S Dig.*, 1999, pp. 13–16.

[4] P. Rodgers, M. Megahed, C. Page, J. Wu, and D. Staab, "Silicon UTSi® CMOS RFIC for CDMA wireless communications systems," in *IEEE RFIC-S Dig.*, 1999, pp. 181–184.

[5] M. Ono, N. Suematsu, S. Kubo, Y. Iyama, T. Takagi, and O. Ishida, "1.9-GHz/5.8-GHz-band on-chip matching Si-MMIC low noise amplifiers fabricated on high resistive Si substrate," in *IEEE RFIC-S Dig.*, 1999, pp. 189–192.

[6] C. S. Kim, M. Park, C.-H. Kim, H. K. Yu, K. Lee, and D. Y. K. Cho, "Thick metal CMOS technology on high resistivity substrate for monolithic 900 MHz and 1.9 GHz CMOS LNA's," in *IEEE MTT-S Dig.*, 1999, pp. 573–576.

[7] B. Razavi, "A 2.4-GHz CMOS receiver for IEEE 802.11 wireless LAN's," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1382–1385, Oct. 1999.

[8] M. Harada, T. Tsukahara, and J. Yamada, "0.5-1 V 2 GHz RF front-end circuits in CMOS/SIMOX," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2000, pp. 378–379.

[9] H. Komurasaki, H. Sato, K. Yamamoto, K. Ueda, S. Maeda, Y. Yamaguchi, N. Sasaki, T. Miki, and Y. Horiba, "A Sub 1-V L-band low noise amplifier in SOI CMOS," *IEICE Trans. Fundamentals*, vol. E83-A, no. 2, pp. 220–227, Feb. 2000.

[10] J. Kodate, H. Harada, and T. Tsukahara, "2 GHz 1 V low noise amplifier fabricated in high resistivity SIMOX wafer" (in Japanese), in *Proc. 2000 IEICE General Conf.*, Mar. 2000, p. C-2-46.

[11] K. Runge, D. Pehlke, and B. Schiffer, "On-chip matched 5.2 GHz and 5.8 GHz differential LNA's fabricated using 0.35 μm CMOS technology," *Electron. Lett.*, vol. 35, no. 22, pp. 1899–1900, Oct. 1999.

[12] T.-P. Liu, E. Westerwick, N. Rohani, and R.-H. Yan, "5GHz CMOS radio transceiver front-end chipset," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2000, pp. 320–321.

[13] H. Samavati, H. R. Rategh, and T. H. Lee, "A 5-GHz CMOS wireless LAN receiver front end," *IEEE J. Solid-State Circuits*, vol. 35, pp. 765–772, May 2000.

[14] Y. Iyama, N. Suematsu, T. Shigematsu, T. Moriwaki, and T. Ikeda, "L-band SPDT swtich using Si-MOSFET," *IEICE Trans. Electron.*, vol. E79-C, no. 5, pp. 636–643, May 1996.

[15] J. Kanda and M. Muraguchi, "A Si RF switch MMIC for cellular frequency band using SOI-CMOS technology" (in Japanese), in *Proc. 2000 IEICE General Conf.*, Mar. 2000, p. C-2-10.

[16] M. Kumar, Y. Tan, J. Sin, L. Shi, and J. Lau, "A 900 MHz SOI fully-integrated RF power amplifier for wireless transceivers," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2000, pp. 382–383.

[17] Y. J. E. Chen, M. Hamai, D. Heo, A. Sutono, S. Yoo, and J. Laskar, "RF power amplifier integration in CMOS technology," in *IEEE MTT-S Dig.*, 2000, pp. 545–548.

[18] A. Giry, J.-M. Fournier, and M. Pons, "A 1.9 GHz low voltage CMOS power amplifier for medium power RF applications," in *IEEE RFIC-S Dig.*, 2000, pp. 121–124.

[19] J. C. Rudell, J. -. Ou, T. B. Cho, G. Chien, F. Brianti, J. A. Weldon, and P. R. Gray, "A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2071–2088, Dec. 1997.

[20] K. Yamamoto, K. Maemura, N. Kasai, Y. Yoshii, Y. Miyazaki, M. Nakayama, N. Ogata, T. Takagi, and M. Otsubo, "A single-chip GaAs RF transceiver for 1.9-GHz digital mobile communication systems," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1964–1973, Dec. 1996.

[21] K. Yamamoto, T. Moriwaki, T. Fujii, J. Otsuji, M. Miyashita, Y. Miyazaki, and K. Nishitani, "A 2.2-V Operation, 2.4-GHz single-chip GaAs MMIC transceiver for wireless applications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 502–512, Apr. 1999.

[22] E. C. Low, H. Nakamura, H. I. Fujishiro, and K. T. Yan, "A plastic package GaAs MESFET 5.8 GHz receiver front-end with on-chip matching for ETC system," in *IEEE RFIC-S Dig.*, 1999, pp. 43–47.

[23] H. Sato, K. Kashiwagi, K. Niwano, T. Iga, T. Ikeda, K. Mashiko, T. Sumi, and K. Tsuchihashi, "A 1.9-GHz single-chip IF transceiver for digital cordless phones," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1974–1980, Dec. 1996.

[24] R. G. Meyer, W. D. Mack, and J. J. E. M. Hageraats, "A 2.5-GHz BiCMOS transceiver for wireless LAN's," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2097–2104, Dec. 1997.

[25] A. Pèrssinen, J. Jussila, J. Ryynènen, L. Sumanen, and K. A. I. Halonen, "A 2-GHz wide-band direct conversion receiver for WCDMA applications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1893–1903, Dec. 1999.

[26] H. Yano, Y. Nakahara, T. Hirayama, N. Matsuno, Y. Suzuki, and A. Furukawa, "Ku-band Si MOSFET monolithic amplifiers with low-loss on-chip matching networks," in *IEEE RFIC-S Dig.*, 1999, pp. 127–130.

[27] M. Steyaert, M. Borremans, J. Janssens, B. D. Muer, N. Itoh, J. Craninckx, J. Crols, E. Morifuji, H. S. Morose, and W. Sansen, "A single-chip CMOS transceiver for DCS-1800 wireless communications," in *IEEE ISSCC Dig. Tech. Papers*, 1998, pp. 48–49.

[28] F. Behbahani, J. Leete, W. Tan, Y. Kishigami, A. Karimi-Sanjanni, A. Roithmeier, K. Hoshino, and A. Abidi, "An adaptive 2.4GHz low-IF receiver in 0.6 μm CMOS for wideband wireless LAN," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2000, pp. 146–147.

[29] M. B. Shifrin, P. J. Katzin, and Y. Ayasli, "Monolithic FET structure for high-power control component applications," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 2134–2141, Dec. 1989.

[30] K. Yamamoto, T. Moriwaki, Y. Yoshii, T. Fujii, J. Otsuji, M. Miyashita, Y. Miyazaki, and K. Nishitani, "A 1.9-GHz-band single-chip GaAs T/R-MMIC front-end operating with a single voltage supply of 2V," *IEICE Trans. Electron.*, vol. E81-C, no. 7, pp. 1112–1121, July 1998.

[31] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," in *IEEE 1997 Symp. on VLSI Circuits Dig. of Tech. Papers*, pp. 85–86.

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