A Low-Power 2.4-GHz Transmitter/Receiver CMOS IC

Alireza Zolfaghari, *Member, IEEE,* and Behzad Razavi, *Fellow, IEEE*

***Abstract*—A 2.4-GHz CMOS receiver/transmitter incorporates circuit stacking and noninvasive baseband filtering to achieve a high sensitivity with low power dissipation. Using a single 1.6-GHz local oscillator, the transceiver employs two upconversion and downconversion stages while providing on-chip image rejection filtering. Realized in a 0.25-μm digital CMOS technology, the receiver exhibits a noise figure of 6 dB and consumes 17.5 mW from a 2.5-V supply, and the transmitter delivers an output power of 0 dBm with a power consumption of 16 mW.**

***Index Terms*—Bluetooth, channel-select filters, IEEE 802.11b, low-noise amplifiers, noninvasive filtering, power amplifiers, RF transceivers.**

I. Introduction

THE DEMAND for low-power wireless transceivers operating in the 2.4-GHz band has led to extensive research on RF architecture and circuit design. The use of standards such as Bluetooth and IEEE 802.11b becomes more attractive as low-cost low-power solutions emerge, pointing to CMOS technology as an important contender. A number of low-power 2.4-GHz transceivers have been reported [1]–[4], but it is desirable to achieve even lower power levels.

This paper describes the design of a 2.4-GHz CMOS receiver/transmitter (RX/TX) incorporating low-power circuit and architecture techniques. Compared to prior art, the principal challenge here is to reduce the power consumption while obtaining better sensitivity in a standard digital CMOS process that provides no high-quality resistors or capacitors. Based on a dual-conversion architecture, the RX/TX employs a single local oscillator (LO) to simplify the frequency planning and the design of the building blocks. A "noninvasive" filtering concept is also introduced that relaxes the noise–linearity tradeoffs in the receiver baseband filters.

Section II presents the RX/TX architecture, and Sections III and IV describe the front–end circuit details. Section V introduces an example of channel-select filter design, and Section VI summarizes the experimental results.

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A. Zolfaghari was with the Department of Electrical Engineering, University of California, Los Angeles, CA 90095-1594 USA. He is now with RF Micro Devices, Newport Beach, CA 92660 USA.

B. Razavi is with the Department of Electrical Engineering, University of California, Los Angeles, CA 90095-1594 USA (e-mail: razavi@icsl.ucla.edu).

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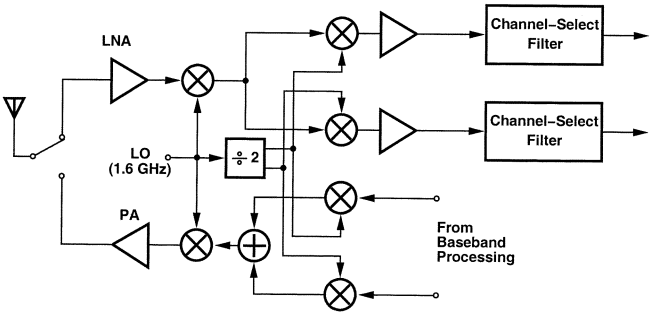


Fig. 1. Transceiver architecture.

II. Architecture

The receiver employs two downconversion stages using a first LO frequency of 1.6 GHz and a second LO frequency of 800 MHz, translating the input spectrum from 2.4 GHz to an intermediate frequency (IF) of 800 MHz and subsequently to zero. The baseband signals are then applied to channel-select low-pass filters (LPFs). The transmitter upconverts baseband quadrature waveforms (for either linear or nonlinear modulation) to an IF of 800 MHz and subsequently to 2.4 GHz.

The architecture of Fig. 1 offers several advantages over typical homodyne or heterodyne counterparts.

1) The LO emission produced by the receiver is well out of the band and heavily suppressed by the selectivity of the antenna.
2) The pulling of the LO by the power amplifier (PA) is negligible.
3) The system requires a single frequency synthesizer operating at 1.6 GHz, relaxing the requirements of the voltage-controlled oscillator (VCO) and the prescaler.
4) The LO frequency of 1.6 GHz allows addition of a low-IF global positioning system (GPS) path to the receiver (the GPS L_1-band signal is at 1.575 GHz).
5) Quadrature LOs at 800 MHz are generated by a divide-by-two circuit, avoiding power-hungry polyphase filters.
6) Since the downconversion to zero occurs with an LO frequency of 800 MHz, matching between the quadrature phases is more accurate and the flicker noise of mixers is lowered [5].

The use of a 1.6-GHz LO in the first downconversion reduces the image frequency to 800 MHz (with a bandwidth equal to one third of the desired signal band), allowing substantial filtering of the image on the chip, 41 dB in this design. Furthermore, the antenna and the preselect filter can provide tens of decibels of image rejection. For example, two small monopole 2.4-GHz antennas operating as a transmitter and

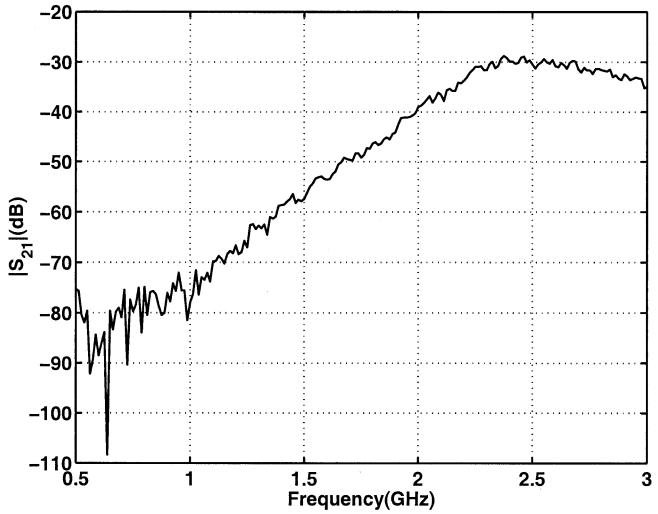


Fig. 2. Measured characteristic of two antennas operating back to back.

a receiver exhibit the measured gain characteristic shown in Fig. 2, providing a total rejection of about 50 dB (25 dB each) at 800 MHz. (The antenna can even be designed to provide a notch at 800 MHz with little compromise in the 2.4-GHz band.) With a typical preselect filter rejection of 35 dB, the overall image rejection can exceed 100 dB.

With the signal band of 2.400–2.480 GHz, the image lies in the range of 800–827 MHz, exhibiting a 3-MHz overlap with GSM800 and IS54 transmit bands. If, in some applications, the rejection of this band by 100 dB is insufficient, the LO frequency can be shifted down by a few megahertz, resulting in a low-IF output. Except for the baseband filter, the RX/TX design need not be altered.

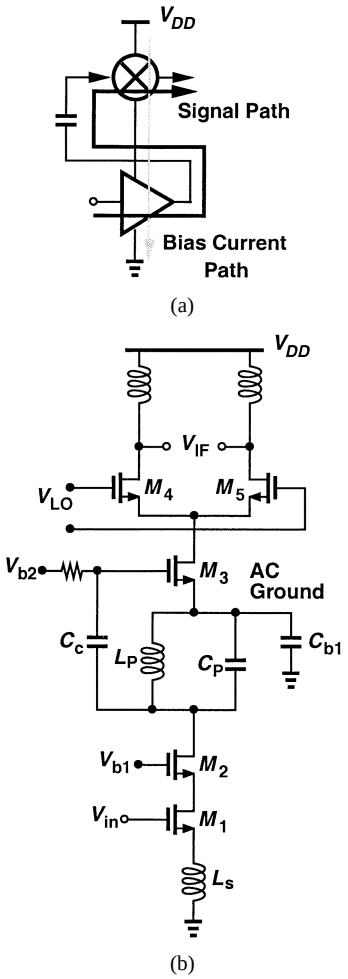


Fig. 3. (a) Stacking the LNA on top of the mixer. (b) Transistor implementation.

III. Receiver Front-End

A. First Downconversion

As two of the power-hungry building blocks, the front-end low-noise amplifier (LNA) and mixer play a critical role in the sensitivity, linearity, and image rejection of the receiver. In order to save power, the supply voltage can be lowered but the minimum is dictated by the headroom issues in the baseband section and the prescaler in the synthesizer as well as the tuning range required of the VCO. For this reason, the supply is set at 2.5 V and stacking techniques are employed to reuse the bias currents.

As conceptually illustrated in Fig. 3(a), the first mixer is stacked on top of the LNA, with the transistor implementation depicted in Fig. 3(b). The stacking is possible owing to the high IF and, hence, the use of inductive (rather than resistive) loads in the mixer. The circuit still suffers from two drawbacks. First, due to the low quality factor Q of L_P, the image rejection is limited to about 20 dB. Second, since the mixer load tanks cannot sufficiently attenuate the LO feedthrough, the following stages are desensitized.

In order to increase the image rejection of the circuit, the circuit is modified to that in Fig. 4(a), where the tank consisting of L_i and C_i resonates at 800 MHz, degenerating M_3 at the image frequency and boosting the overall image rejection to more than 40 dB. Finally, to resolve the LO feedthrough problem, the mixer is converted to a double-balanced topology (with one RF input at ac ground) as shown in Fig. 4(b).

The circuit of Fig. 4(b) incorporates a number of passive components such as inductors and capacitors. To implement large inductance values while occupying minimal chip area, stacked spirals are employed [6]. Fig. 5 shows the inductors used in the first downconversion circuit. The RF inductor at the output of the LNA is a two-layer 7-nH stacked spiral and the IF and image-rejection inductors are four-layer 50-nH stacked spirals. The inductors exhibit a Q of approximately 3 at the frequency of interest.

Two other passive components in the LNA/mixer circuit are the coupling and bypass capacitors. Limited by the digital CMOS process, the former (C_c) is made of a three-layer metal sandwich to reduce both the area and the bottom-plate capacitance. The connection of the coupling capacitor is such that the bottom-plate capacitance is resonated out by the LNA load inductor. The bypass capacitor C_{b1} must be large enough to avoid current coupling to the source of the mixer input device. To implement large capacitance values with a reasonable chip area, MOS transistors with the source and drain connected to

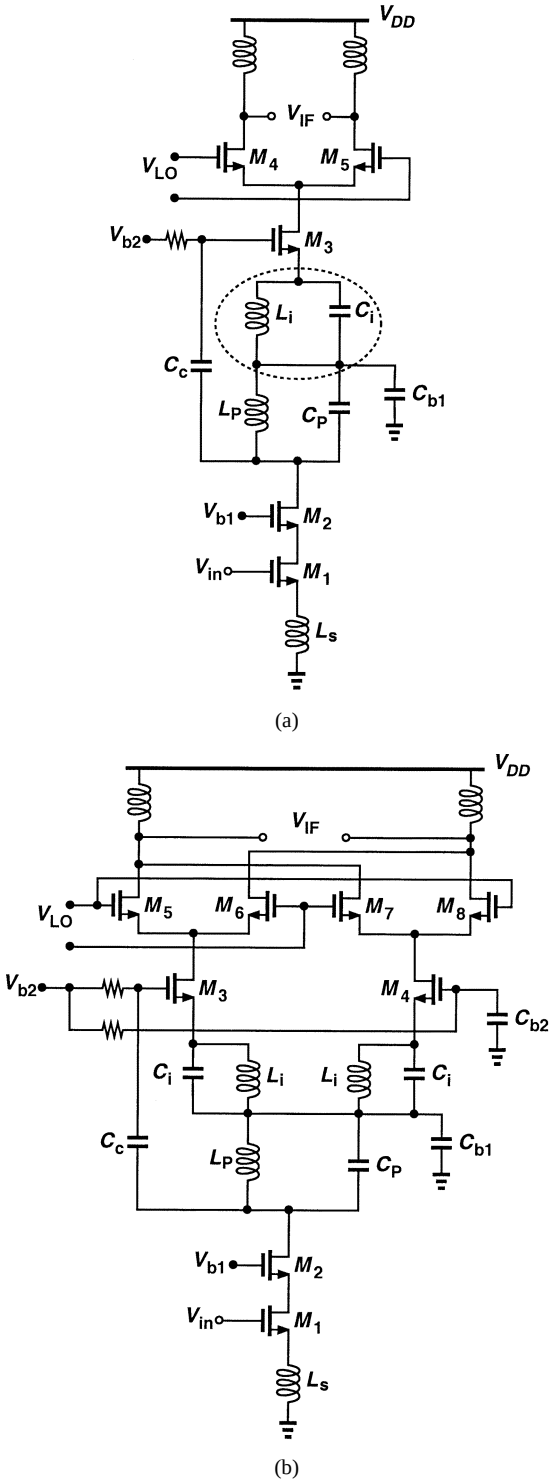


Fig. 4. (a) Improving the image rejection. (b) First downconversion circuit.

ground are used. Proper choice of device dimensions ensures a high Q at RF, thus providing a low impedance to ground.

Simulation results suggest that, with a supply current of 2.5 mA, the LNA/mixer combination achieves a noise figure of 3 dB, an input IP_3 of -16 dBm, and a total gain of 29 dB. In this simulation, the thermal noise of transistors is lumped into the channel noise with a γ of 2.5 ($\overline{I_n^2} = 4kT\gamma g_m$).

To accommodate high input levels, the front-end must employ automatic gain control. For example, the gate voltage of the cascode device in the LNA can serve as a means of reducing the gain while making the input more linear.

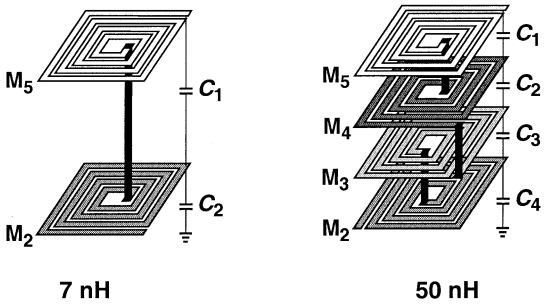


Fig. 5. Inductors used in downconversion.

B. Second Downconversion

The choice of the IF mixers is determined primarily by their linearity, power dissipation, and flicker noise. Passive mixers typically outperform active implementations in all three aspects, but they do require large LO swings. Fig. 6(a) depicts the second downconversion circuit, which consists of a double-balanced passive mixer and common-source (CS) pMOS baseband amplifiers. Coupling capacitors C_1 and C_2 also act as degenerative impedances in series with the switches, thereby improving the linearity. With the large gain provided by the LNA and the RF mixer, the linearity of the CS stages limits the IP_3 of the overall receiver. For this reason, these stages (used both in I and Q paths) consume a notable fraction of the receiver's power.

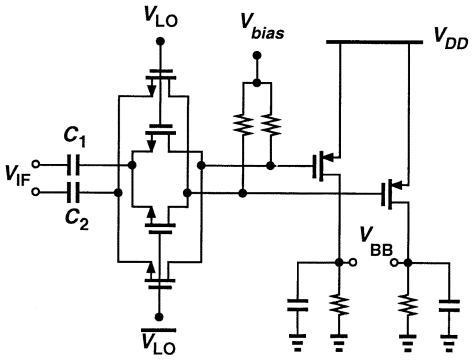
In order to drive the mixer switches by large swings, the divide-by-two circuit of Fig. 1 incorporates the rail-to-rail latch shown in Fig. 6(b). Each latch draws an average current of 0.75 mA from the supply.

IV. Transmitter

As shown in Fig. 1, the I and Q baseband signals are first upconverted to 800 MHz and then added together. Since the distortion of the first stage is critical, passive mixers similar to those in the receiver are used to upconvert the baseband I and Q signals. Fig. 7 shows the second upconversion circuit. Here, the IF I and Q signals are first converted to current by M_1–M_4 and are added together. The result is then upconverted to RF by M_5–M_8. The mixer of Fig. 7 employs a tail current source to allow direct coupling to the preceding stage, but it utilizes a bypass capacitor C_b to suppress the third-order nonlinearity.

The limited voltage headroom and high center frequency make it difficult to use a current mirror to convert the differential output current of the mixer to a single-ended signal suited to the PA. The output is, therefore, sensed at one output, but with a large load inductance to avoid signal loss. Note that the selectivity of the resonant loads in the mixer and the PA suppresses the second harmonic of the LO considerably. The second upconversion stage draws 1.5 mA from the supply and the RF inductor is realized as a two-layer stacked structure.

After two upconversions, the RF signal drives the power amplifier. To achieve enough drive capability, the PA consists of two tapered stages: a driver and an output stage. Fig. 8(a)



(a)

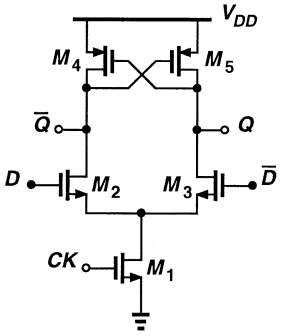


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Fig. 6. (a) Second downconversion circuit. (b) D-latch circuit.

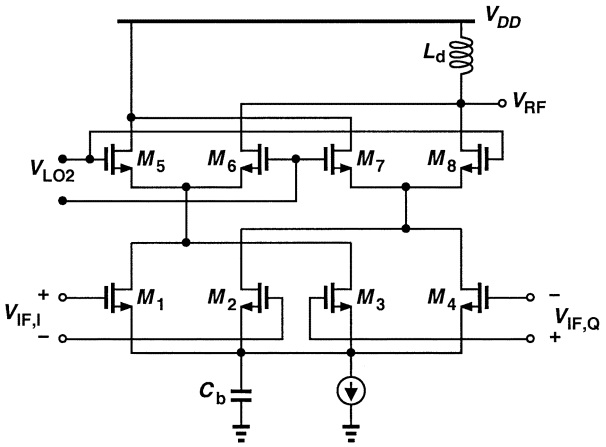
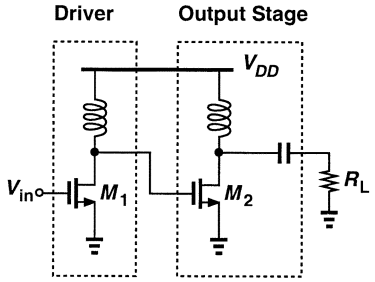


Fig. 7. Second upconversion in the transmitter.



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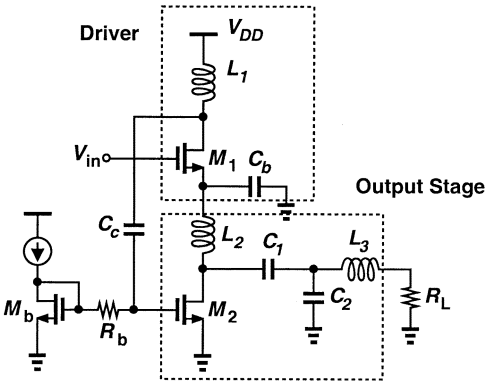
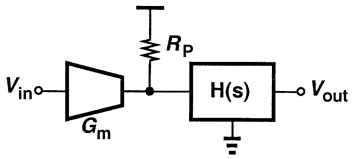


(b)

Fig. 8. (a) Two-stage power amplifier. (b) Power amplifier circuit.



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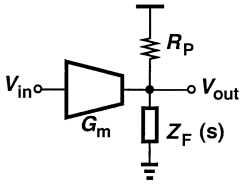


(b)

Fig. 9. (a) Conventional filtering. (b) Noninvasive filtering.

depicts an example. This circuit, however, suffers from three important drawbacks. First, with two current paths from V_{DD} to ground, the circuit consumes a high power. Second, large output swings at the drain of M_2 degrade the long-term reliability of the device. Third, in order to deliver 1 mW to a 50-Ω load (R_L), the output stage requires a peak-to-peak current $(I_{\rm PP})$ of 12.6 mA $(P = I_{\rm PP}^2 R_L/8)$. For M_2 to operate as a class-A amplifier, the absolute minimum bias current is half of $I_{\rm PP}$, but to achieve reasonable linearity, the bias current must be higher, leading to high power consumption.

To resolve these issues, the design is modified as shown in Fig. 8(b). In this circuit, the driver is stacked on top of the output stage, and the bypass capacitor C_b provides an ac ground at the source of M_1. Capacitor C_c couples the driver to the output stage. Stacking both reduces the power consumption and protects M_2 from excessive drain–gate voltage.

In order to increase the output current of M_2, a matching network is employed. The network consists of two metal-sandwich capacitors C_1 and C_2 and the wirebond inductor L_3, transforming $R_L = 50\ \Omega$ to a load resistance of 500 Ω presented to M_2.

Simulation results indicate that, with a bias current of 3 mA, the circuit delivers 0 dBm to a 50-Ω load with a third-order intermodulation of -28 dBc.

V. Channel-Select Filter

This section presents the concept of noninvasive filtering and applies the technique to a baseband filter for Bluetooth applications.

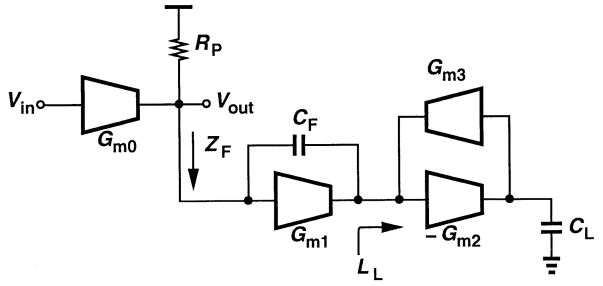


Fig. 10. Second-order noninvasive filter topology.

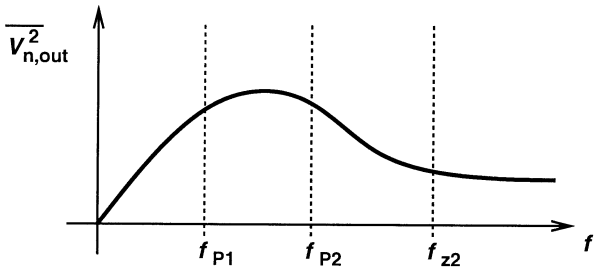


Fig. 11. Output noise of the filter produced by transconductor stages.

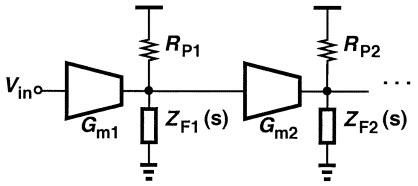


Fig. 12. Higher order noninvasive filtering.

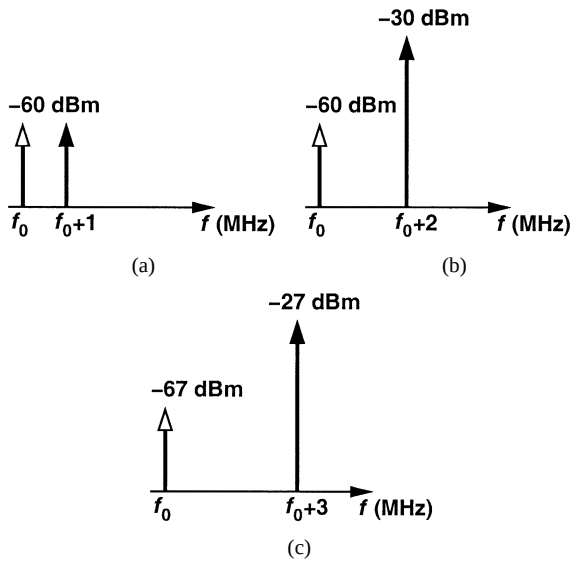


Fig. 13. Interferers (black arrows) and the desired signal(white arrow) levels in Bluetooth. (a) Adjacent channel interferer as strong as the signal. (b) Alternate channel interferer 30 dB higher than the signal. (c) Second alternate interferer 40 dB higher than the signal.

A. Noninvasive Filtering

The conventional approach to filtering requires that both the signal and the interferers travel through a circuit that provides the desired transfer function [Fig. 9(a)]. However, such a filter introduces significant noise and intermodulation in the signal band. It is, therefore, advantageous to seek a method that applies filtering to only interferers without "invading" the signal band. For example, as illustrated in Fig. 9(b), a complex impedance $Z_F(s)$ can be placed in *parallel* with the signal path such that it operates as an open in the signal band while shunting the interferers to ground. As a result, $Z_F(s)$ provides selectivity with negligible additional noise, a critical advantage in view of the high $1/f$ corner frequency in modern CMOS devices. Furthermore, $Z_F(s)$ creates only a small intermodulation current through R_P because its Thevenin equivalent is relatively high in the signal band. Nevertheless, some linearity is still necessary if $Z_F(s)$ is to operate as an effective shunt at interferer frequencies.

Fig. 10 shows a second-order G_m-C implementation of $Z_F(s)$. Here, transconductors G_{m2} and G_{m3} form a gyrator that converts capacitor C_L to an emulated inductor $L_L = C_L/(G_{m2}G_{m3})$ [8]. As a result, as the frequency rises, the voltage across C_F increases, giving a second-order $Z_F(s)$. The transfer function is given by

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = G_{m0}R_P \times \frac{1+\dfrac{C_FC_L}{G_{m2}G_{m3}}s^2}{1+R_PC_Fs+\dfrac{C_FC_L}{G_{m2}G_{m3}}(R_PG_{m1}+1)s^2}. \quad (1)$$

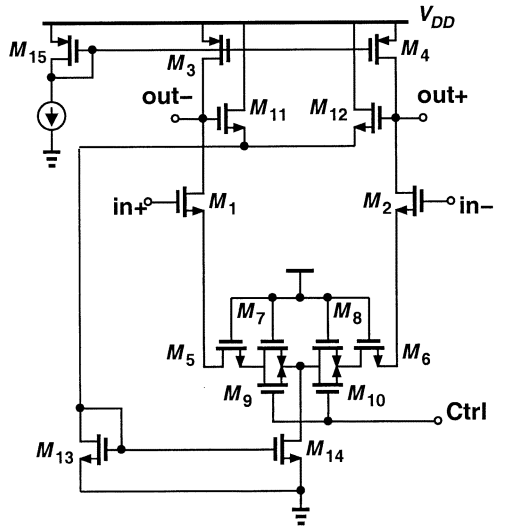
The zero results from the resonance of C_F with L_L and can be chosen to create a notch in the stop band, (e.g., an elliptic filter). In practice, the depth of the notch is limited by the output impedance of the G_m stages and the Q of the capacitors. In applications where no zero is required (such as Butterworth filters), a buffer can be placed in series with C_F to block the feedforward current.

The noise performance of the circuit is revealed by

$$\overline{v^2_{n,G_m}} = 4kT\Gamma R_P^2\left(\frac{C_FC_L}{G_{m2}G_{m3}}\right)^2 \times \frac{\omega^2\left[\omega^2(G_{m1}+G_{m3})+\dfrac{G_{m3}^2G_{m1}}{C_L^2}\right]}{\left[1-\dfrac{C_FC_L}{G_{m2}G_{m3}}(R_PG_{m1}+1)^2\omega^2\right]^2+R_P^2C_F^2\omega^2} \quad (2)$$

where the noise of each transconductor is expressed as $4kTG_m\Gamma$ and only the noise of G_{m1}–G_{m3} is included. This transfer function exhibits the same poles as (1), but as expected, it also provides a zero at dc, thereby suppressing the effect of flicker noise. The other zero is typically higher than the poles, resulting in the noise-shaping function shown in Fig. 11. The key observation is that the area under this plot is typically much less than the noise contributed by G_{m0} and R_P.

The topology of Fig. 10 may prove inadequate in some applications. In an RF receiver, for example, the circuit may not provide enough rejection beyond the signal channel and the adjacent channel. This issue can be resolved by increasing the order of $Z_F(s)$ or using cascaded biquad sections as shown in Fig. 12. The choice depends on the application and is explained in Section V-B.



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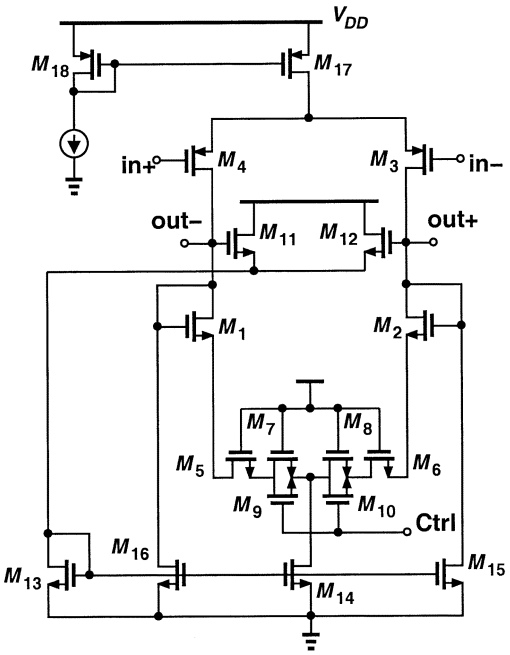

(b)

Fig. 14. (a) Transconductor circuit. (b) Input transconductor and parallel resistor.

B. Filter Design

The filter designed here serves to suppress interferers in a Bluetooth receiver. Illustrated in Fig. 13, scenarios where the filter selectivity becomes critical include 1) an adjacent channel interferer as strong as the signal; 2) an alternate channel interferer 30 dB higher than the signal; and 3) a second alternate interferer 40 dB higher than the signal [9]. With 40 dB of receiver gain preceding the filter, the interferers applied to the filter exhibit large amplitudes, requiring a high linearity. To determine the maximum tolerable noise and nonlinearity of the filter as well as its minimum order, a Matlab program was written that includes a Gaussian frequency-shift keying (GFSK) detector and, hence, a means of calculating the bit-error rate. This study indicates that a cascade of two second-order sections yields sufficient selectivity if they introduce deep notches in the adjacent

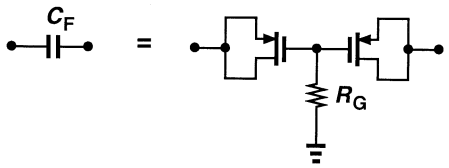

Fig. 15. Floating capacitors realized by back-to-back pMOS devices.

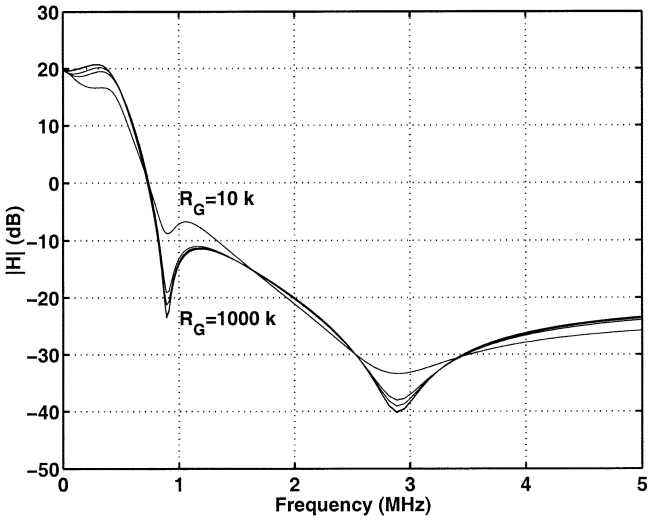

Fig. 16. Simulated filter characteristic for $R_G = 10, 50, 100, 500,$ and $1000\,\mathrm{k}\Omega$.

channels. To achieve the selectivity required for Bluetooth, the overall filter consists of two cascaded sections, one yielding a notch at 1 MHz and the other at 3 MHz to suppress the adjacent channels. Note that a fourth-order elliptic realization achieves comparable suppression but at the cost of greater sensitivity to the element values. For this reason, cascaded biquads are preferred.

C. Filter Realization

With four transconductors per section, the filter can potentially consume a high power. Fig. 14(a) depicts a low-power tunable implementation of the transconductor, where the amount of degeneration is partially controlled by varying the on-resistance of M_9 and M_{10}. With their gates tied to V_{DD}, M_7 and M_8 "soften" the variation as the control voltage falls. This topology is used for G_{m1}–G_{m3} in Fig. 10. The unit-cell transconductor consumes 34 μW to provide a transconductance of 25 $\mu\Omega^{-1}$. As with conventional $G_m - C$ filters, the prototype can be tuned using a phase-locked loop.

The implementation of the filter in a digital technology mandates a MOS realization for R_P in Fig. 10. To achieve process and temperature tracking, G_{m0} and R_P are designed as shown in Fig. 14(b). Here, diode-connected transistors M_1–M_2 and triode devices M_5–M_{10} form the load resistor and are tuned along with the other transconductors. Note that, as predicted by (1), the transconductance of this circuit does not affect the shape of the transfer function. This suggests the possibility of using the stage as a variable-gain amplifier as well.

The lack of high-density linear capacitors in this technology makes the implementation of C_F and C_L in Fig. 10 difficult. In particular, with a cutoff frequency of 400 kHz and two

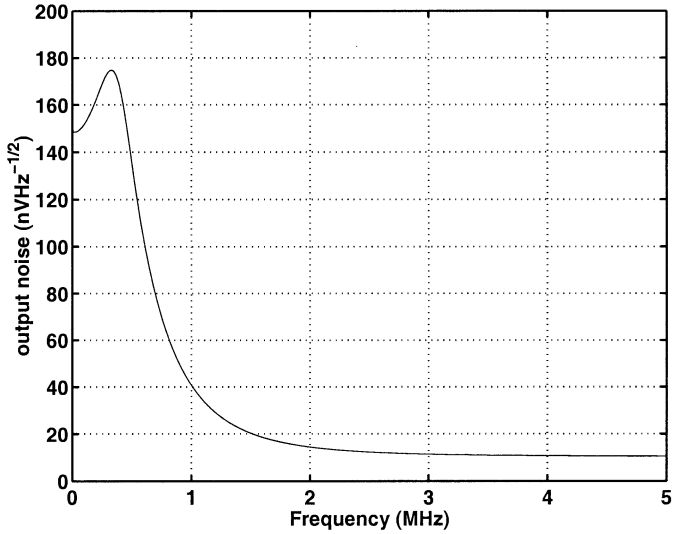

Fig. 17. Simulated output noise of the noninvasive filters.

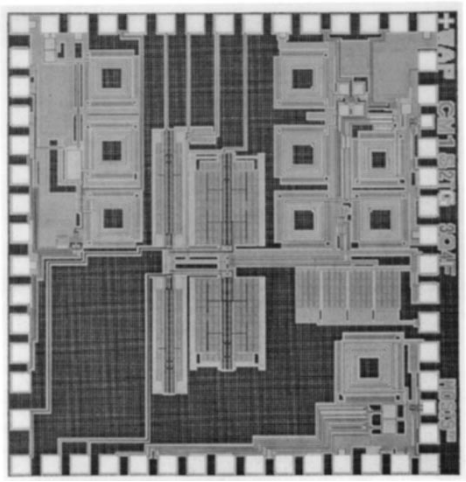

Fig. 18. Die micrograph.

second-order sections, the filter demands a total capacitance of approximately 100 pF, which translates to a large area even for lateral flux capacitors. This is overcome through the use of back-to-back pMOS devices as shown in Fig. 15. Here, the gates of the devices are connected to ground through an n-well resistor so as to ensure operation in strong inversion. The value of R_G must be high enough to affect the transfer function negligibly. Fig. 16 plots the overall filter transfer function for different values of R_G, indicating that $R_G \approx 500$ kΩ is adequate.

Fig. 17 shows the simulated output noise of the filter, indicating a total integrated noise of approximately 1 μV (across 5-MHz bandwidth). Note that the low-frequency noise density is equal to 147 nV/$\sqrt{\text{Hz}}$, i.e., that of the input transconductors G_{m0} and parallel resistors R_P. The peaking contributes approximately 10% to the total root-mean-square (rms) noise voltage, confirming that noninvasive filtering contributes negligible noise in the passband.

TABLE I
MEASURED PERFORMANCE OF RX/TX

Receiver	
Noise Figure	6 dB
Voltage Gain	50 dB
Image Rejection Ratio	41 dB
Input Return Loss	12 dB
Signal/Intermodulation Ratio	26 dB
Power Dissipation	
LNA and Mixers	6.25 mW
Divider	3.75 mW
Baseband Amplifiers	3.5 mW
Baseband Filters	4 mW
Total	17.5 mW
Transmitter	
Output Power	0 dBm
Sidebands	–30 dBc
Power Dissipation	12 mW
Technology	0.25–um CMOS
Supply Voltage	2.5 V
Area	1.83 mm x 2 mm

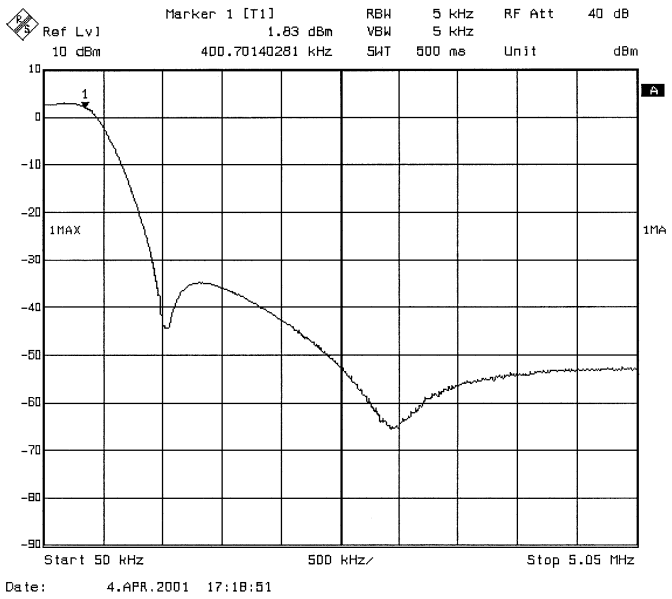

Fig. 19. Measured receiver characteristic.

VI. EXPERIMENTAL RESULTS

An experimental prototype of the RX/TX has been fabricated in a 0.25-μm CMOS technology. Fig. 18 shows the die, which measures 1.83×2 mm^2. Unwanted coupling between the inductors is maintained below a few percent by proper spacing.

Table I summarizes the measured performance. The receiver noise figure is obtained by the hot–cold method [10], yielding a value of 6 dB at 200 kHz.

To test the linearity of the receiver based on Bluetooth specifications, two interferers located in channels 3 and 6 are applied [9]. With an input level of -39 dBm for each interferer and a desirable signal level of -64 dBm, the signal-to-intermodulation ratio measured at the output of the baseband filters

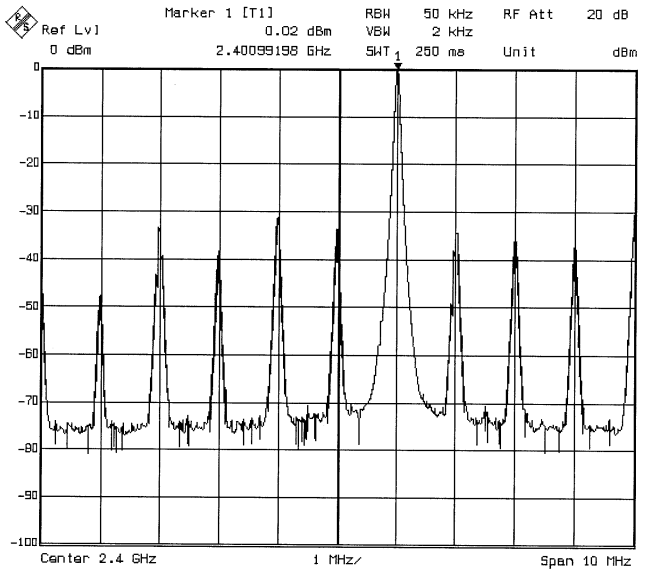

Fig. 20. Measured transmitter spectrum.

is equal to 26 dB, well above the level required for proper detection. The receive path, including the divide-by-two circuit, consumes 17.5 mW from a 2.5-V supply with an overall gain of 50 dB. Fig. 19 plots the transfer function from the RF input to the output of the channel-select filters, exhibiting deep notches at 1 and 3 MHz.

The transmitter delivers 0 dBm with a power consumption of 16 mW, including the divide-by-two circuit. Fig. 20 shows the output spectrum of the transmit path. All unwanted components are 30 dB below the desired signal.

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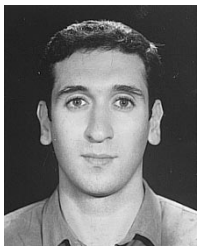
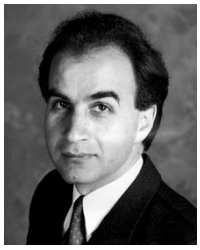


Alireza Zolfaghari (S'99–M'02) was born in Tehran, Iran, in December 1971. He received the B.S. and M.S. degrees in electrical engineering from Sharif University of Technology, Tehran, in 1994 and 1996, respectively, and the Ph.D. degree from the University of California, Los Angeles, in 2001.

In 1998, he was with TIMA laboratory, Grenoble, France. During the winter of 2001, he was a Consultant with Prominent Communications, San Diego, CA. Subsequently, he was with Transpectrum Technologies, Los Angeles, where he worked on high-speed amplifiers. He is currently with RF Micro Devices, Newport Beach, CA. His research interests include analog and RF circuits for wireless communications and high-speed circuits for optical transceivers.



Behzad Razavi (S'87–M'90–SM'00–F'03) received the B.Sc. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1985 and the M.Sc. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1988 and 1992, respectively.

He was an Adjunct Professor with Princeton University, Princeton, NJ, from 1992 to 1994, and Stanford University in 1995. He was with AT&T Bell Laboratories and Hewlett-Packard Laboratories until 1996. Since September 1996, he has been an Associate Professor and, currently, Professor of electrical engineering at University of California at Los Angeles. His current research includes wireless transceivers, frequency synthesizers, phase-locking and clock recovery for high-speed data communications, and data converters. He is the author of *Principles of Data Conversion System Design* (New York: IEEE Press, 1995), *RF Microelectronics* (Englewood Cliffs, NJ: Prentice-Hall, 1998) (translated to Japanese by Tadahiro Kuroda), *Design of Analog CMOS Integrated Circuits* (New York: McGraw-Hill, 2001), and *Design of Integrated Circuits for Optical Communications* (New York: McGraw-Hill, 2002), and the editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (Piscataway, NJ: IEEE Press, 1996).

Dr. Razavi received the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the best paper award at the 1994 European Solid-State Circuits Conference, the best panel award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, and the best paper award at the IEEE Custom Integrated Circuits Conference in 1998. He was the corecipient of both the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence at the 2001 IEEE International Solid-State Circuits Conference. He served on the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC) from 1993 to 2002 and is currently a member of the Technical Program Committee of the Symposium on VLSI Circuits. He has also served as Guest Editor and Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, and the *International Journal of High Speed Electronics*. He is an IEEE Distinguished Lecturer.