A 2-V CMOS Cellular Transceiver Front-End

Michel S. J. Steyaert, *Senior Member, IEEE*, Johan Janssens, *Student Member, IEEE*, Bram De Muer, *Student Member, IEEE*, Marc Borremans, *Student Member, IEEE*, and Nobuyuki Itoh, *Associate Member, IEEE*

***Abstract*—This work presents the design and implementation of a 2-V cellular transceiver front-end in a standard 0.25-μm CMOS technology. The prototype integrates a low-IF receiver (low noise amplifier, I/Q mixers, and VGAs) and a direct-upconversion transmitter (I/Q mixers and pre-amplifier) on a single die together with a complete phase-locked loop, including a 64/79 prescaler, a fully integrated loop filter, and a quadrature voltage-controlled oscillator with on-chip inductors. Design trade-offs have been made over the boundaries of the different building blocks to optimize the overall system performance. All building blocks feature circuit topologies that enable comfortable operation at low voltage. As a result, the IC operates from a power supply of only 2 V, while consuming 191 mW in receiver (RX) mode and 160 mW in transmitter (TX) mode. To build a complete transceiver system for 1.8-GHz cellular communication, only an antenna, an antenna filter, a power amplifier, and a digital baseband chip must be added to the analog front-end. This work shows the potential of achieving the analog performance required for the class I/II DCS-1800 cellular system in a standard 0.25-μm CMOS technology, without tuning or trimming.**

I. Transceiver Architecture

THE TOPOLOGY of the implemented CMOS transceiver front-end is shown in Fig. 1. The transceiver IC integrates a low-IF quadrature receiver, a direct upconversion transmitter, and a fully integrated phase-locked loop (PLL) synthesizer—including *LC* tank and loop filter—on the same CMOS die. The receive path consists of a low noise amplifier (LNA), a quadrature mixer, and an LF VGA filter. The transmit path consists of a quadrature upconversion mixer and an RF output driver. The PLL contains a fully integrated polyphase quadrature voltage-controlled oscillator (VCO), a 64/79 modulus prescaler, a phase-frequency detector, and an on-chip loop filter with linearization.

A complete 1.8-GHz cellular system (Fig. 1) can be built by flanking the transceiver IC with an antenna filter/switch, a power amplifier, a cristal reference, and a digital baseband chip, containing the A/D, D/A, and the all-digital delta–sigma fractional-N PLL steering.

A low-IF/direct upconversion architecture has been selected because of its excellent integratability. Since the image rejection and the channel selection do not rely on high-Q filtering, in principle no external filters are required. In the receiver, the image rejection is done by quadrature down-mixing, while in the transmit path, the image is canceled due to the quadrature upconversion. The only remaining external filter is the preselector filter, which is directly positioned behind the antenna. This is, however, no real limitation since today's cellular applications always require a switch multiplexer or duplex filter.

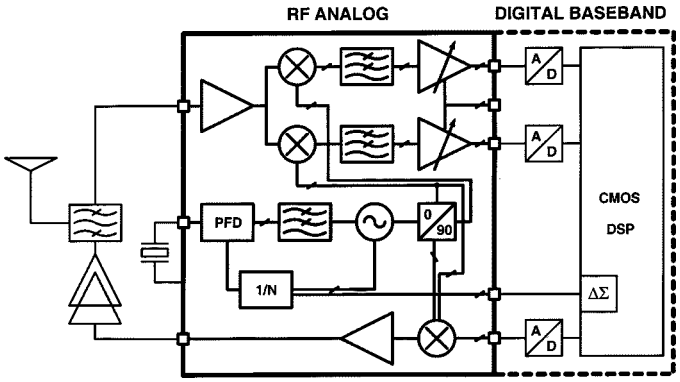


Fig. 1. Transceiver front-end in a complete solution for DCS-1800.

Moreover, due to the absence of the external filters in this architecture, the number of external RF nodes is greatly reduced with respect to a heterodyne topology. Only the receiver (RX) input and the transmitter (TX) output are connected to the outside world. All other high-frequency signals remain on chip. This means that the (external) passives that were previously transforming the local on-chip impedance down to the characteristic impedance of the IF or interstage filters are no longer needed. Also, the robustness of the architecture is improved because the interaction with the package parasitics is minimized. Sensitive nodes are not brought outside, decreasing the sensitivity to interference and crosstalk.

The architecture also fully exploits the power of digital signal processing. Apart from the coarse channel select filter, which also functions as antialiasing filter, and some signal conditioning, the rest of the operations in the receive path, such as image rejection, channel selection and demodulation, are carried out in the digital domain by a digital signal processor (DSP). This is an attractive property, since the digital domain is after all the natural biotope of CMOS. Additionally, in contrast to the analog part, the digital part features a much better scalability (i.e., portability toward next process generations) and a great flexibility (i.e., software reconfigurable chip).

The low-IF architecture features the same high degree of integration as a zero-IF receiver, however, it is less susceptible to $1/f$ noise and dc offset [18]. As long as the A/D converters have enough dynamic range, the dc-offset can be removed in the DSP without loss of information or degradation of the quadrature relation. In addition, a careful choice of the low IF allows

Manuscript received April 19, 2000; revised July 18, 2000.

M. S. J. Steyaert, J. Janssens, B. De Muer, and M. Borremans are with the Katholieke Universiteit Leuven, Department ESAT-MICAS, B-3001 Heverlee, Belgium (e-mail: michiel.steyaert@esat.kuleuven.ac.be).

N. Itoh is with Toshiba Corporation, Kawasaki, 210-8520, Japan.

Publisher Item Identifier S 0018-9200(00)09470-1.

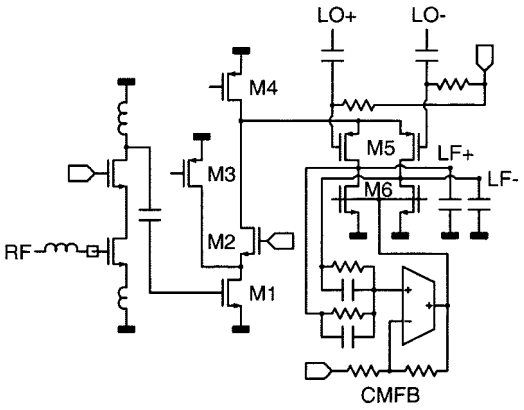


Fig. 2. LNA and mixer topology.

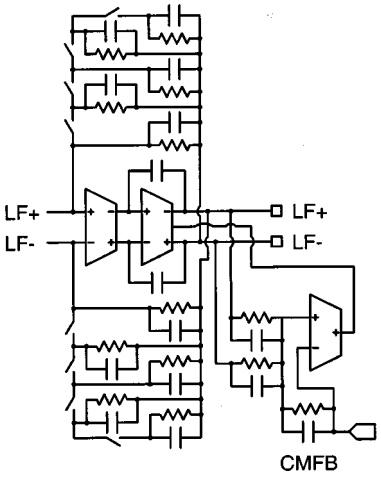


Fig. 3. VGA topology.

for a significant relaxation of the required quadrature accuracy specification. In this transceiver, an IF of 100 kHz is selected because it ensures that the mirror signal is the signal in the adjacent channel. Because the signal in the adjacent channel is maximally only 9 dB higher than the wanted signal [17], the quadrature accuracy specification is set by the second adjacent channel and the required transmitter accuracy.

II. Receive Path

The low-IF receiver consists of an LNA connected to two (I and Q) downconversion mixers (Fig. 2) followed by a variable gain amplifier filter (Fig. 3). The front-end converts the RF signal into a differential I and Q signal, centered at an 100-kHz IF. $\Sigma\Delta$ A/D conversion, channel selection, mirror suppression, and additional AGC is assigned to a digital CMOS baseband chip (Fig. 1).

The LNA employs a classical cascode topology [1] that is input matched using inductive source degeneration through an on-chip spiral inductor. The slightly lower input impedance of 30 Ω improves the LNA gain by about 1 dB compared to an exact 50-Ω match. In the original technique [2], [3], an extra matching section is introduced between the 50-Ω source and the 30-Ω LNA input. However, this LNA does not employ such a section since the S_{11} is already -12 dB, which means that only 6% of the incident power is reflected. The LNA directly drives the downconversion mixer without intermediate image filter, avoiding an LNA output matching circuit and a costly external filter component. The on-chip inductor at the LNA output resonates against the load capacitance of the I and Q mixers, centering the gain at 1.84 GHz. The LNA features a noise figure of only 2.2 dB at a power of 10 mW.

Each downconversion mixer employs a cascoded current-folding switching mixer topology (Fig. 2). The folding mechanism allows low-voltage operation while enabling the insertion of a cascode transistor M2 to reduce local oscillator (LO) leakage and LO self-mixing and to increase mixer linearity. The large $V_{\rm GS}-V_{\rm T}$ of the input transconductor M1 sets the mixer $\rm IP_3$ to $+17$ $\rm dBV_{ref}$ (224 mV rms). To keep the feedback capacitance of the VGA small, the transconductance of M1 must be kept to a minimum. However, noise and offset considerations put a lower bound on the transconductance.

The limited $V_{\rm GS}-V_{\rm T}$ of the top current source M4 is responsible for a lot of noise. The noise contribution of M4 is reduced by supplying a large part of the current of M1 through a pMOS bleeder M3. Because M3 can be biased at a much higher $V_{\rm GS}-V_{\rm T}$ than M4, for the same amount of current its transconductance and hence its noise contribution can be made much lower. In addition, the capacitance on the switching node is reduced, leading to a higher pole frequency and consequently an increased mixer efficiency. The contribution of M3 to the capacitance on the cascode node remains small because of its small size. In principle, the current through M2 can be lowered until the pole on the cascode node is degraded. In practice, the minimum current is set by the maximum input signal of the mixer:

$$I_{2,\min} > \mathrm{gm}_1 v_{\mathrm{in},\max}. \tag{1}$$

The size of the pMOS switches M5 is determined as a compromise between input capacitance, loss due to the pole at the switch node, dc offset, white noise, and residual $1/f$ noise injected due to incomplete switching. The $V_{\rm GS}-V_{\rm T}$ of M6 is made as large as possible to lower the injected noise current. In addition, its area is maximized to suppress the $1/f$ noise. A common-mode feedback (CMFB) circuit sets the common-mode level on the interface between mixer and VGA to 1 V. This feedback is necessary because the common-mode input impedance of the VGA is high. Note that the gate capacitance of M6 determines the nondominant pole of the CMFB circuit.

The VGA, shown in Fig. 3, consists of a two-stage fully differential Miller operational transconductance amplifier (OTA) with a bank of highly matched *RC* transimpedance elements (8R1C, 8R1C, 4R2C, 2R4C, 1R8C). Apart from the VGA function, the *RC* transimpedance performs first-order filtering of the blocking signals and acts as a coarse antialias filter. The gain of the VGA can progressively be decreased by 6 dB by connecting the transimpedance elements in parallel. The VGA switches *must* be placed at the virtual ground of the OTA in order not to cause distortion. The common-mode output voltage of the VGA is controlled by an additional CMFB circuit. The low differential-mode input impedance of the transimpedance amplifier ensures a maximum transfer of current from the mixer to the

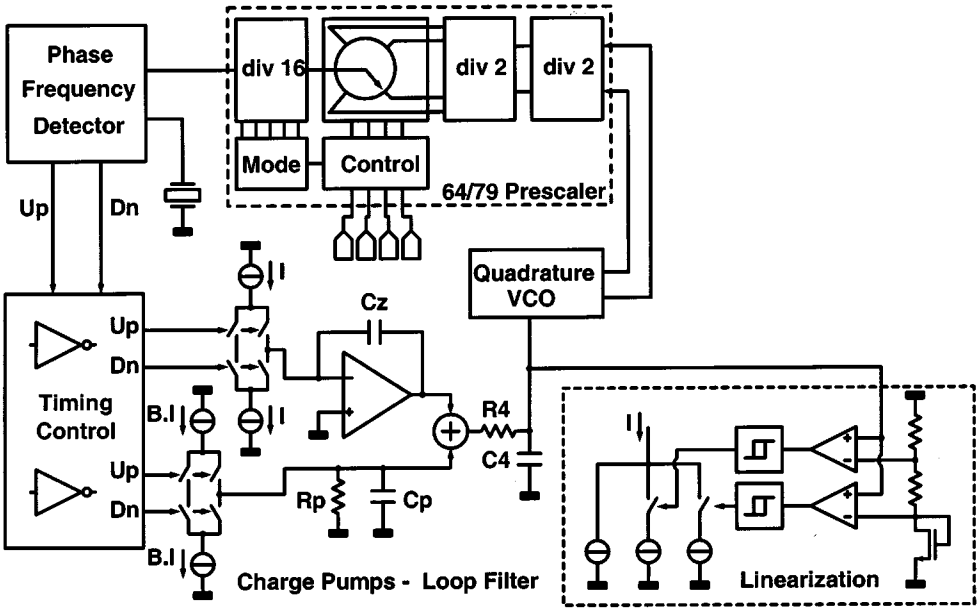


Fig. 4. PLL topology.

VGA. In addition, this structure exploits the linearity of passive elements and high-gain OTAs to provide a rail-to-rail output at minimum distortion. Due to the large loop gain, the output of the VGA stays very linear until the 1-dB compression point of $+15$ dBV$_{\rm ref}$ (224 mV rms) is reached.

III. PLL Frequency Synthesizer

The LO signal for both the RX and TX path is generated by a fully integrated fourth-order type-II PLL frequency synthesizer which is included in the transceiver chip (Fig. 4). A quadrature *LC*-tank VCO as well as a fourth-order 35-kHz low-pass loop filter are integrated on-chip. By integrating the loop filter and the VCO, no external HF nodes are present, reducing transmitted signal pickup and power consumption. Furthermore, a 64/79 high-speed prescaler, a phase-frequency detector with no dead zone, a dual charge pump, and a three-step equalizer are implemented. To synthesize the 200-kHz channel spacing, required by the DCS-1800 standard, delta–sigma fractional-N division [4] must be applied, which is purely digital and therefore in the chip partitioning assigned to the CMOS digital baseband processor (Fig. 1).

The high-speed division of the prescaler is done with two dynamic single transistor clocked logic (DSTC) n-latches [5], forming a differential dynamic D-flip-flop, which is clocked by the differential output signal of the VCO. The flip-flop operates with rail-to-rail internal signals to minimize the residual prescaler phase noise. The 16-modulus division (64/79) is implemented with the phase-switching topology [6]. The different divide factors are generated by switching between the 90° spaced output phases of the second flip-flop, whose output is the input signal divided by four. When the 90° spacing is not ideal, spurs can be generated at 1/4, 2/4, and 3/4 of 26 MHz (the PLL reference frequency). By careful layout and circuit design, the spurs are suppressed to values that could not even be measured with the spectrum analyzer. The maximum operating frequency of the complete prescaler is designed to be 2.2 GHz for a power consumption of only 7 mA at 2 V.

The frequency synthesizer integrated in the transceiver is a charge-pump PLL. The phase difference detection is done with a zero-dead-zone phase-frequency detector (PFD) [7], whose output pulses control a dual charge pump. To minimize reference spur generation by the PFD–charge-pump circuit, the charge-pump current sources are carefully matched and the charge injection due to transients when the pumps are switched is minimized. To accomplish this, first the integration in the first path of the loop filter is done actively to keep the charge-pump output at a fixed level. Second, the charge pump current is designed to be at least a magnitude larger than the fixed parasitic charge injection of the switch transistors. In this case, the charge-pump current is 4 μA. Last but not least, a timing control scheme is developed to control the charge-pump switches. The switching scheme is such that the undesired charge is not injected in the filter impedance, but is deviated through dummy current branches.

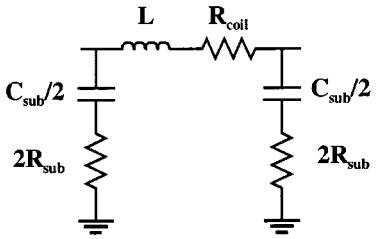
A type-II fourth-order PLL implementation was chosen to ensure sufficient noise and spurious suppression. For sufficient phase margin, a low-frequency stabilizing zero is inserted in the loop filter transfer function. Due to its low-frequency nature, the capacitance to realize the zero is very area expensive. To be able to go to full integration, a dual-path filter topology has been implemented [8] (Fig. 4). Two filter paths, one integration (C_z) and one low-pass filter (R_p, C_p) are added to reveal a virtual zero, without additional capacitance. The frequency of the zero is controlled by the charge-pump scaling factor B. For stability, the zero is placed a factor 4 lower than the crossover frequency of the loop, and the two poles ($\tau_p = R_pC_p$ and $\tau_4 = R_4C_4$) that determine the out-of-band suppression are placed a factor 6 higher than the crossover frequency. The resulting phase margin

TABLE I
PLL PARAMETERS

Design parameters		Passive elements		Performance	
ω_c	35 kΩ	R_p	3.2 kΩ	L_{tot} {600 kHz}	-125.9dBc/Hz
I_{qp}	4 μA	R_4	1.07 kΩ	Settling time	293 μs
B	12	C_p	240 pF		
		C_4	710 pF		
PM	57°	C_z	450 pF		
ζ	0.77	C_{total}	1.4 nF		

TABLE II
VCO INDUCTOR PARAMETERS

#turns	3
Width (μm)	15
Radius (μm)	120
L (nH)	2.857
C_{sub} (pF)	1.83
R_{coil} (Ω)	3.7
R_{sub} (Ω)	75



is 57° and the damping factor ζ is 0.77. The open loop transfer function of the PLL is then given by

$$GH(s) = \frac{I_{qp} \cdot K_{\text{vco}}}{2\pi \cdot N} \cdot \frac{1 + s\tau_z}{s^2 \cdot C_z \cdot (1 + s\tau_p)(1 + s\tau_4)} \qquad (2)$$

with $\tau_z = R_z \cdot (C_p + B \cdot C_z) \approx BR_pC_z$, $\tau_p = R_pC_p$, $\tau_4 = R_4C_4$, I_{qp} the charge pump current, N the division factor, and K_{vco} the VCO gain.

A PLL model that calculates the noise contributions of the different PLL elements has been implemented in Matlab [9]. Using the program, an optimization has been performed to determine the values of the loop passive components and the loop bandwidth. The most important optimization goal is to achieve the phase-noise specification for DCS-1800 with all capacitance on-chip. This trade-off is mainly controlled by the charge-pump factor B, the size of R_4 (and thus C_4), and the loop bandwidth. The resulting loop parameters, the loop filter components, and the simulated PLL performance are summarized in Table I. The total integrated capacitance is only 1.4 nF. The loop bandwidth of 35 kHz is chosen to satisfy the settling performance, which is simulated using Saber [10]. To comply with the 2-V power-supply constraint, the addition of both filter paths is performed in the current domain. This gives a sufficient margin to synthesize the DCS-1800 frequency band, since the VCO's tuning range is more than 28% at 2 V [11].

The out-band PLL phase noise is determined by the phase noise of the VCO. An inductor with a Q of 9 is integrated in the standard CMOS process with only two normal-sized metal layers (M1: 0.6 μm and M2: 1.0 μm) and a moderate substrate resistance of 5 Ωcm. The inductor parameters are listed in Table II. The VCO is designed to drive the polyphase filter without additional buffering. The resulting phase-noise degradation is simulated to be less than 1.8 dB, while no increase in power consumption. The injection of spurs, generated by the high-speed digital switching in the prescaler are minimized by separating the prescaler power supply from other supply lines and on-chip bypassing. Moreover, isolation buffers are inserted between the VCO and the prescaler to prevent kickback noise from entering the VCO *LC* tank.

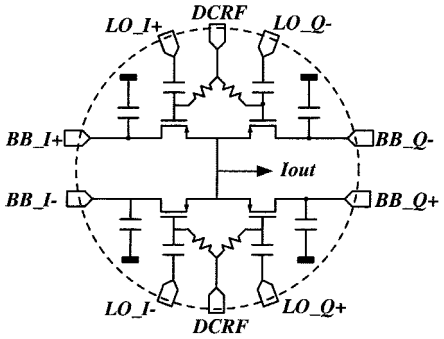


Fig. 5. Upconversion mixer transistor structure.

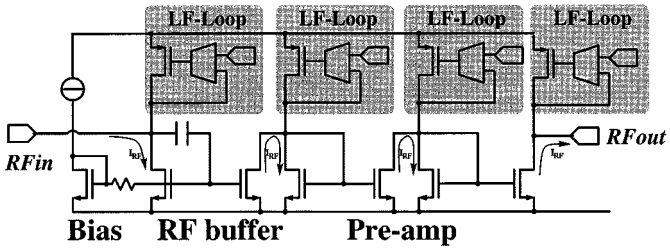


Fig. 6. RF current buffer with high-pass filter function and the pre-amplifier.

As can be seen in (2), the VCO gain determines the open loop gain of the PLL. To make sure that the loop is stable and achieve its noise specifications over the complete tuning range, the VCO gain influence must be stabilized. Therefore, a three-step equalizer is implemented, which keeps the product of the VCO gain and the charge-pump current constant within predetermined ranges. The equalization is done by comparing the VCO control voltage with voltages generated by a reference ladder. Schmitt triggers provide the hysteresis necessary to avoid instabilities.

IV. TRANSMIT PATH

An intrinsically linear transconductance mixer topology has been selected to convert the baseband and local oscillator signals into a linear high-frequency modulated current. Four nMOS nonswitching transistors biased in the linear operating region have been combined to provide balanced quadrature direct upconversion with a single-ended output (Fig. 5). A good understanding and optimization of the impedance degeneration effects on the sensitive mixer nodes is essential to prevent the signal from being reduced and to guarantee the proper linear operation. Based on the analysis of the first- and second-order effects and the short channel effects on the linearity [13], the transconductance mixer has been designed to have low distortion, intermodulation and LO-feedthrough components.

Fig. 5 also shows the large on-chip integrated capacitors at the baseband nodes of the mixer transistors. The modulated RF current flows through the capacitors toward ground and not through

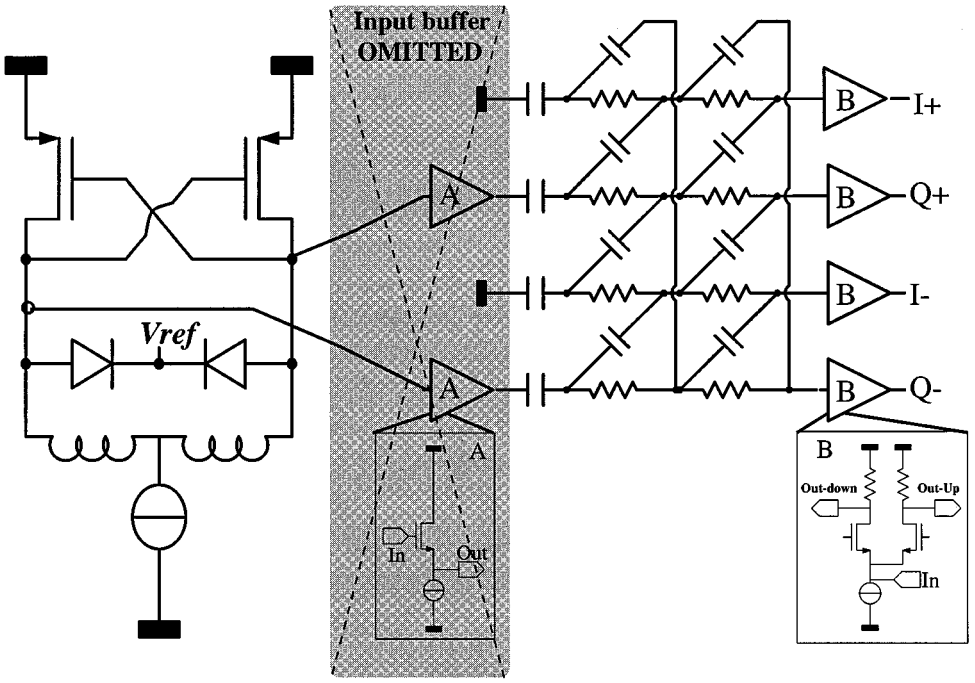


Fig. 7. Quadrature VCO

the bonding wires. The RF signal linearity and amplitude become independent of the bonding wire's matching and length as the RF signal remains on chip.

A low impedance is required at the common mixer node to prevent additional mixing products by the low-frequency square baseband current component and to minimize the degeneration of the high-frequency component. The buffer used in this design provides a low impedance at both high and low frequency and also performs a high-pass filter function on the mixer current. The transistor schematic is shown in Fig. 6. The ac coupling in the buffer offers the advantage that this circuit can be used at a very low supply voltage. Another advantage of this ac-coupled topology is that the dc voltage at the common mixer node can be chosen quasi-independently of the optimization of the output buffer, resulting in an important extra degree of design freedom.

Any low-frequency mixing component is compensated by the pMOS feedback loop, which also sets the dc voltage. The bandwidth and the gain of the LF loop and of the HF ac-coupled loop have been designed to provide both the required low impedance and the high-pass filter function. The current buffer, which guarantees correct mixer operation, and the successive output driver are based on nMOS folding current mirrors. This has the advantage that the power-supply current stays constant. The RF current only flows locally in small loops. In this way, coupling to other parts of the system through the power supply is prevented.

A major advantage of the folded current mirror structure is that a good linearity can be achieved with a relatively low dc current. The distortion components can easily be estimated from the I–V characteristics of MOS transistors. For a current mirror this results in

$$HD2 = \frac{1}{8} \cdot \frac{\Delta V_{\mathrm{T}}}{V_{\mathrm{GS}} - V_{\mathrm{T}}} \cdot \frac{I_{\mathrm{ac}}}{I_{\mathrm{dc}}} \tag{4}$$

and

$$HD3 = \frac{1}{32} \cdot \frac{\Delta V_{\mathrm{T}}}{V_{\mathrm{GS}} - V_{\mathrm{T}}} \cdot \left(\frac{I_{\mathrm{ac}}}{I_{\mathrm{dc}}}\right)^2. \tag{5}$$

The relatively large currents require considerable transistor widths. Because of the direct relation between the matching performance and the transistor area [14], a good transistor matching (low ΔV_{T}) is achieved. Hence, a relatively low dc/ac current ratio can be allowed in the pre-amplifying current mirror stages. The current amplifications are a trade-off between the gain and the poles at the different nodes. The dc voltages have been designed to be at the same value in the pre-amplifier stages, guaranteeing the same drain–source voltage biases. In this way, optimal linear behavior is achieved.

Each pre-amplifier stage also includes a low-frequency feedback loop through the pMOS current source transistor. It determines the dc bias and also suppresses any residual low-frequency signal. The total amplification has been designed to achieve a 0-dBm output signal in a 50-Ω load.

The upconversion mixer is driven by balanced quadrature signals. The balanced quadrature LO signal is generated by a differential *LC*-type oscillator and a differential-to-quadrature converting polyphase filter. The second-order polyphase filter has an I–Q accuracy of more than 35 dB over several hundreds of megaHertz, resulting in a sufficient safety margin to deal with technological inaccuracy. A higher order for the polyphase filter results in a better accuracy and a larger frequency band, but this is at the cost of a higher power consumption in the buffers. To prevent the signal loss, which is intrinsically caused by the passive nature of the *RC* network, the active output buffers provide the LO signal to the mixers. Although the passive *RC* filter does not consume any dc power, the buffers that are typically included between the VCO and the polyphase filter are very power hungry. Therefore, these buffers have been questioned, resulting

in the overall optimization of the VCO, the polyphase filter, the mixers, and the pre-amplifier. In this design, the VCO directly drives the two-stage polyphase filter. The transistor schematics are given in Fig. 7. The merging of those two building blocks can be considered as a quadrature oscillator.

Eliminating the polyphase filter's input buffer has severe consequences on the VCO performance. Two main effects can be distinguished when analyzing the circuit: the capacitive and the resistive loading of the VCO by the *RC* network. The capacitive load determines the oscillation frequency and can easily be taken into account in the design of the VCO as being part of the fixed capacitance. The resistive load negatively affects the loop gain of the VCO and therefore degrades the phase noise. By taking this effect into account, the nonbuffered VCO–polyphase combination achieves a phase noise that is only a few decibels higher than that of the stand-alone VCO. The schematic of the VCO and the directly driven polyphase filter is given by omitting the source follower in Fig. 7. The cascode transistors in the output buffer of the polyphase filter select either the up- or downconverter.

The input impedance of the polyphase filter can be simulated or calculated. For a given frequency, this series circuit can be transformed to an equivalent parallel load. The resulting equivalent parasitic capacitance can be considered as a part of the fixed *LC*-tank capacitance. This can be taken into account in the design. The equivalent load resistor has an important effect on the phase-noise performance. Small resistor values considerably degrade the phase-noise performance. The optimization of the high-frequency polyphase filter as a buffered sub-circuit leads to small resistor values in the *RC* network (in [15] values of 25 to 35 Ω are used for a 2-GHz circuit). Such low resistor values can not be allowed in the directly driven topology.

The VCO's output signal amplitude is no longer restricted to the source follower's input swing. The gain in the polyphase filter can be lowered to get the same signal at the mixers input. This involves that a lower power consumption in the output buffers (1 mA) and larger resistors in the *RC* network can be used.

In the global transceiver design, the maximum load that has to be driven by the polyphase filter is limited as the polyphase filter's resistor values are inversely proportional to the capacitive load that has to be driven. By reducing the load (i.e., the mixer transistors!), the resistor values in the filter can be enlarged, which is beneficial for the VCO's performance. However, making the load by the mixer transistors small reduces the transconductance gain in the mixers and consequently additional amplification is required in the pre-amplifier. A second limitation in the downscaling of the load is the matching performance of the mixers. The mixer transistors have been dimensioned to achieve better than 30-dB matching. Increasing the width improves the matching suppression and signal amplitude, yet requires smaller resistors in the polyphase circuit, degrading the VCO's phase noise. The transistor dimensions have been optimized to achieve an optimal DCS-1800 transmitter performance, including the VCO phase noise, mirror suppression, and the total power consumption.

The implemented VCO has been simulated directly driving a two-stage polyphase filter. In this design, the sum of the resistors in the polyphase filter is 500 Ω. In the case where an input buffer/source follower is used, the value of the magnitude of the input impedance is important. However, in the directly driven version, it is not the magnitude of the impedance that is important. Only the real part of the impedance has an effect on the phase-noise performance. This results in a different performance depending on how the resistor values are divided over the network. If the largest resistor values are at the input of the polyphase filter, the real part of the impedance will be the largest and the imaginary part the smallest (*RC* product constant). This results in a better phase-noise performance. Fig. 8 illustrates this idea. It shows the simulated phase-noise performance for several resistor values. The second resistor is designed to 500 Ω minus the first resistor $R1$.

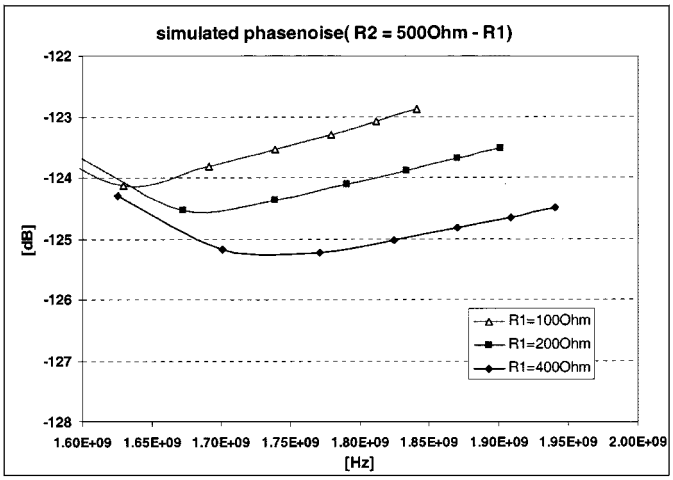


Fig. 8. Simulated phase noise at 600 kHz versus frequency for different values of $R1$. The sum of the resistors in the polyphase filter is constant 500 Ω. Best phase noise is achieved with the largest resistor first.

The figure clearly shows what has been explained in this paragraph. The phase-noise performance is better when the first resistor is the largest. It can be considered as a kind of passive buffer. In the practical design, the value of resistor is limited by two factors: first. the amplification or signal loss in the polyphase filter, and second, the additional noise generated by the resistors.

Fig. 8 also shows a frequency shift between the different simulations. This can be understood from the smaller capacitance when raising the resistor value. This means that when the first resistor value is taken large, the additional (fixed) capacitive load for the oscillator is reduced, which is favorable for both the achievable oscillation frequency and the tuning range.

A 2-pF coupling capacitance has been used between the VCO and the polyphase filter to guarantee independent dc operation. Fig. 9 gives the equivalent parallel resistor and capacitor values for a 400-Ω/220-fF first stage as a function of the coupling capacitor value. The smaller the coupling capacitance the better the values for a good phase-noise performance. However, the value is again limited by the overall gain in the polyphase filter. If the capacitor is too small, the total impedance becomes large, resulting in a considerable signal loss. Therefore, also the magnitude of the impedance value by the capacitor is added to the figure. From this discussion, it has become clear that an optimal

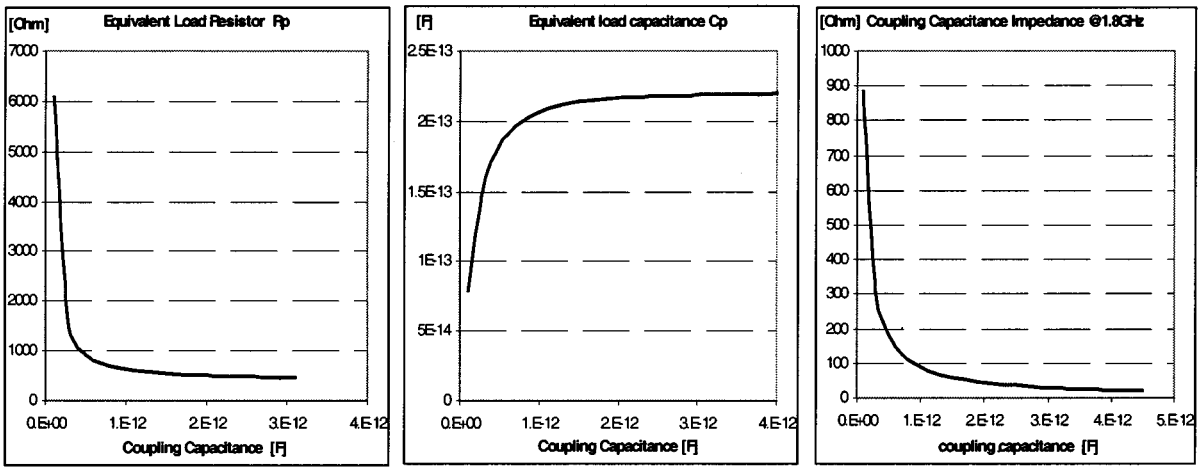


Fig. 9. Effect of the coupling capacitor on the effective parallel resistor and capacitor. The absolute impedance by the capacitor at 1.8 GHz is also shown. ($R1 = 400\ \Omega$; $C1 = 220$ fF).

capacitor value can be taken as a function of the phase-noise performance and the overall gain.

The previous section has made clear that by designing a system as one entity, the power consuming buffers can be avoided. The quadrature oscillator, mixers, and pre-amplifier have been optimized as one building block, trading off output signal and VCO phase noise against global power consumption. The quadrature VCO has been designed to meet the DCS specifications, including a minimized phase-noise degradation due to the polyphase network.

The different design parameters of the traditional building blocks become closely linked. The transistor size of the linear nonswitching mixers is, e.g., a trade-off between modulated RF signal power, matching performance, the quadrature VCO dimensions and phase noise, the amplification in the next stage, the bandwidth and the global power consumption.

V. Experimental Results at 2 V

In this section, the measurement results of the integrated transceiver circuit are discussed.

The conversion gain is measured by supplying the IC with a -50 dBm RF signal which is swept over the DCS-1800 receive band. Each time, the local oscillator frequency is adjusted to track the RF signal with a frequency offset of 10 kHz. The conversion gain of the I-channel at maximum VGA gain is shown in Fig. 10. The gain increases from 54.3 dB at 1.8 GHz to 54.5 dB at 1.83 GHz, and decreases down to 53.3 dB at 1.88 GHz. The steeper roll-off at higher frequencies and the somewhat flatter onset of the gain curve is a direct consequence of the pole on the switch node of the downconversion mixer shaping the second-order roll-off of the LNA *LC*-tank. Note that the gain of the complete low-IF receiver, i.e., the gain from the RF signal toward the low-frequency $I + jQ$ vector signal, is another 3 dB higher and therefore equals 57.5 dB.

The input reflection coefficient of the receive path is shown in Fig. 11. The commonly accepted antenna filter termination requirement of -10 dB is met between 1.65 and 2.1 GHz. The S_{11} is even better than -11.5 dB between 1.72 and 1.97 GHz.

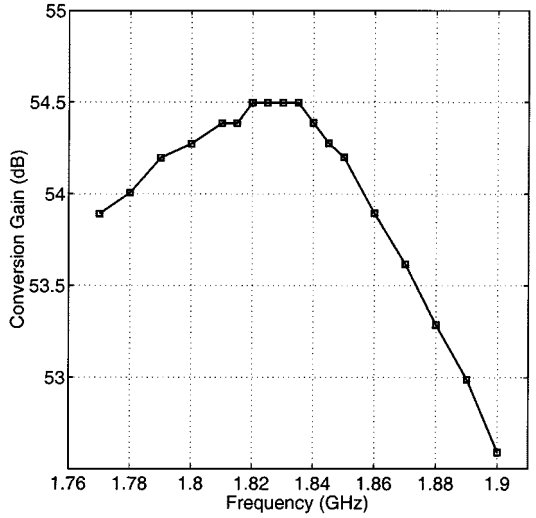


Fig. 10. Conversion gain in the DCS-1800 band.

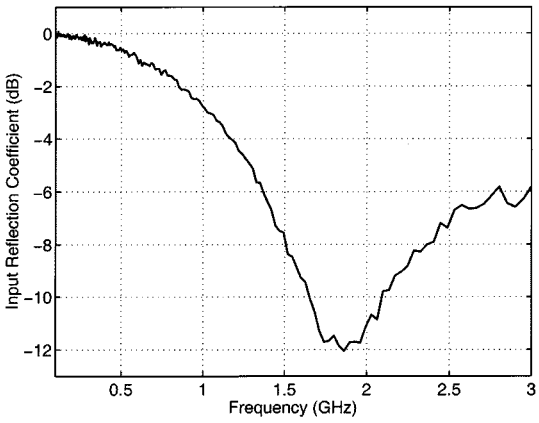


Fig. 11. Input reflection coefficient (S_{11}).

The LO leakage is measured by connecting the RF input terminal to the spectrum analyzer and subtracting 3 dB from the measured power to take into account the loss of the antenna filter. The net LO leakage toward the antenna is less than -63 dBm in the DCS-1800 band. The DCS specification only

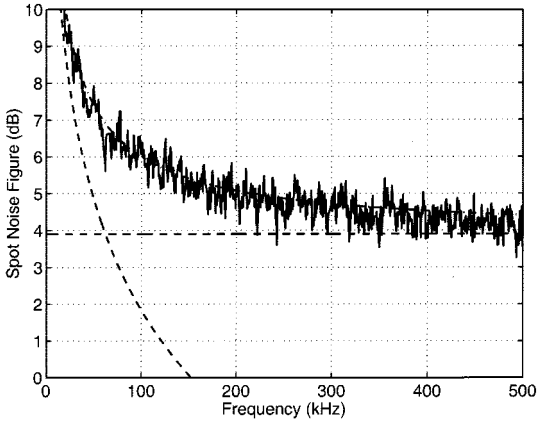


Fig. 12. Measured spot noise figure versus frequency offset from the LO.

requires the LO leakage to be less than −47 dBm (see the Appendix).

To measure the noise performance of the receive path, a 50-Ω noise source is applied to the input. The differential output of a single channel is connected to a differential instrumentation amplifier to convert the output noise into a single-ended signal. In this way, the noise figure of a single path can be measured. The noise figure of the complete low-IF receiver can then be calculated by subtracting 3 dB from the single channel noise figure. After all, the conversion gain of the complete quadrature receiver is two times larger than the conversion gain of a single path. And, on the other hand, it can be shown that the integrated output noise of the quadrature receiver is identical to the measured output noise of a single path. This is true as well for the noise contribution of the mixers and the VGA circuits as for the noise coming from the source and from the LNA. Consequently, the quadrature low-IF output features a 3-dB improvement in the signal-to-noise ratio (SNR) compared to the output of a single low-IF path. And, since the SNR at the input is the same in both cases, the noise figure improves by 3 dB.

Fig. 12 shows the spot noise figure of the receiver at 1.8 GHz versus frequency offset from the carrier. The total noise figure of the complete low-IF receive path ($I+jQ$), i.e., resulting from integration of the output noise in the 200-kHz positive frequency band around the 100-kHz IF, is 6.2 dB. The largest part, 3.9 dB, is caused by white noise. The remaining 2.4 dB is caused by low-frequency $1/f$ noise. The white noise and $1/f$ noise contributions are indicated by the dashed lines in Fig. 12. With a noise figure of 6.2 dB, signals at the DCS-1800 reference sensitivity level of −100 dBm can be detected with an SNR of 11 dB, which is 2 dB better than the 9-dB SNR required by the DCS-1800 specification (see the Appendix). Compared to the noise figure at 1.8 GHz, the noise figure at 1.88 GHz is hardly 1 dB larger. In [16], a higher noise figure value of 8.2 dB is stated because only the influence of the image rejection on the LNA noise had been taken into account.

The image rejection ratio (IMRR) of a receiver is determined by the amplitude and phase accuracy of the quadrature local oscillator and by the circuit mismatch between the I and Q paths. Since circuit mismatch increases with decreasing area, the worst-case IMRR occurs at maximum VGA gain, i.e., when the "activated" area of the *RC* transimpedance bank is minimal.

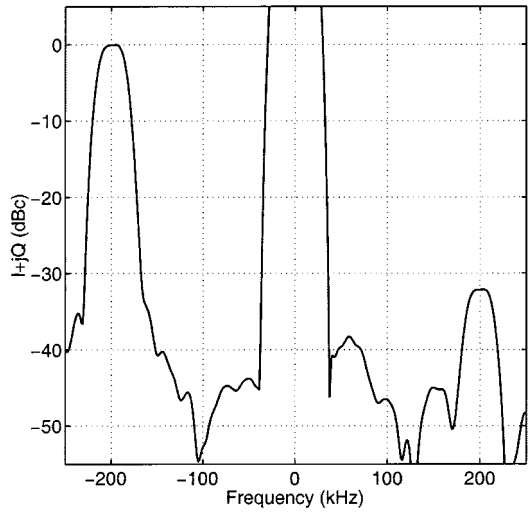


Fig. 13. Image suppression (IMRR) at 200-kHz offset from the LO.

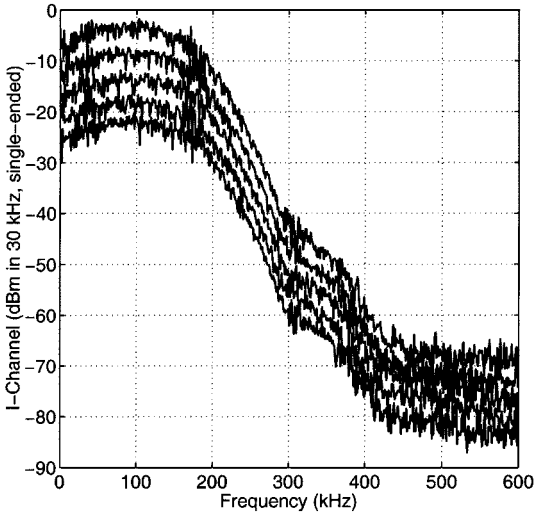


Fig. 14. Spectrum of a −50-dBm GMSK signal after downconversion to the 100-kHz IF. The VGA control bits are swept to select all gain levels.

The IMRR is accurately measured using the HP89410A vector signal analyzer. As shown in Fig. 13, the worst-case IMRR is 32.2 dB at 200-kHz offset from the carrier. The IMRR is measured at 200 kHz because it is precisely at this frequency that the tail of the largest adjacent channel—i.e., the channel at 400-kHz offset from the wanted signal—interferes with the wanted signal. As derived in the Appendix an IMRR of 32 dB sufficiently suppresses this tail. The measured IMRR of 32.2 dB is very close to the measured image suppression in the transmit path (33 dB), which indicates that the limitation stems from the accuracy of the common quadrature VCO. The IMRR value of 32.2 dB corresponds to an amplitude accuracy of 0.3 dB and a phase accuracy of 2.1°.

The measured IP_3 and IP_2 values of the receive path are −6 and +26 dBm, respectively, and are independent of the VGA gain setting. The output capability of a single channel is about +14.8 dBm, i.e., 3.4 $V_{\rm ptp}$ while the in-channel input capability ranges from −38 dBm at maximum gain to −20.4 dBm at minimum gain. Note that the measured intercept point values

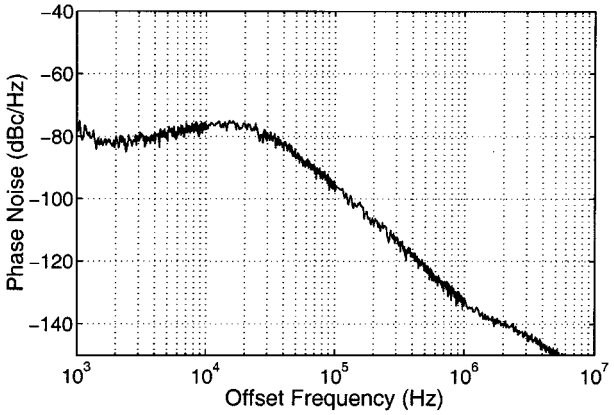


Fig. 15. Measured PLL phase noise.

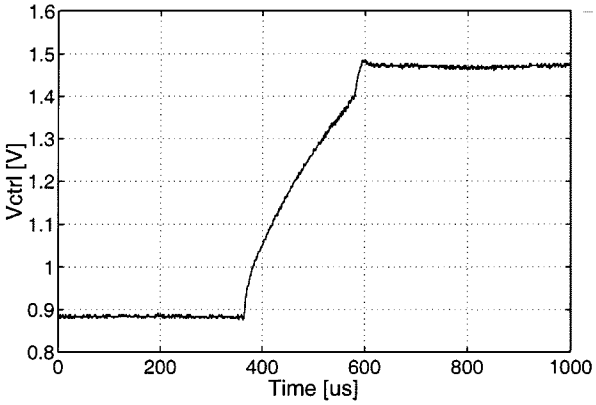


Fig. 16. The measured PLL settling behavior

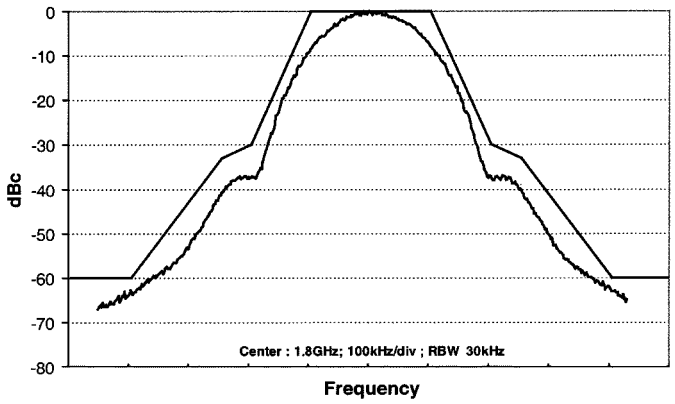


Fig. 17. ETSI DCS-1800 mask compared to GMSK TX output.

apply to the complete receive path. If the LNA would be bypassed, which is typically the case when the power of the wanted signal is high, the intercept points and the input capability immediately improve by about 18 dB.

At the highest VGA gain, the dc offset due to LO self-mixing and static mismatch is measured to be 1.1 V. As long as the A/D converters are not overloaded, the dc offset can be accounted for by putting half a bit extra in the A/D converter.

To demonstrate how the low-IF receiver is used in practice, a 1.84-GHz, −50 dBm PN9 Gaussian minimum shift keying (GMSK) signal is applied to the input of the receiver and downconverted to the 100-kHz IF. The VGA control bits are swept in

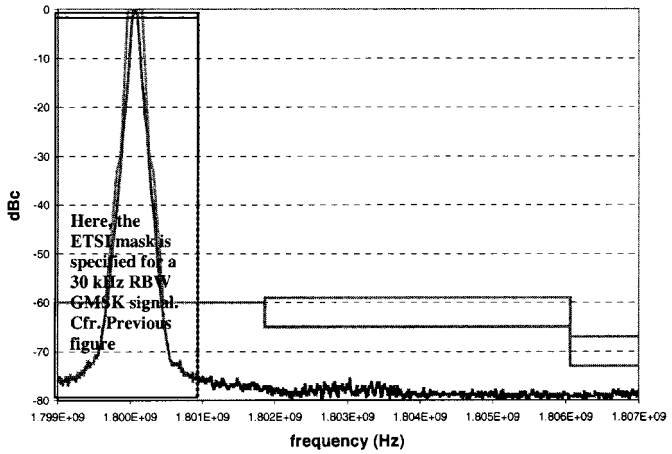


Fig. 18. Measured modulation spectrum compared to ETSI mask, showing that the region from 1.8 MHz from the carrier on complies well to the ETSI specs. (100-kHz resolution bandwidth, 1.8-GHz center frequency).

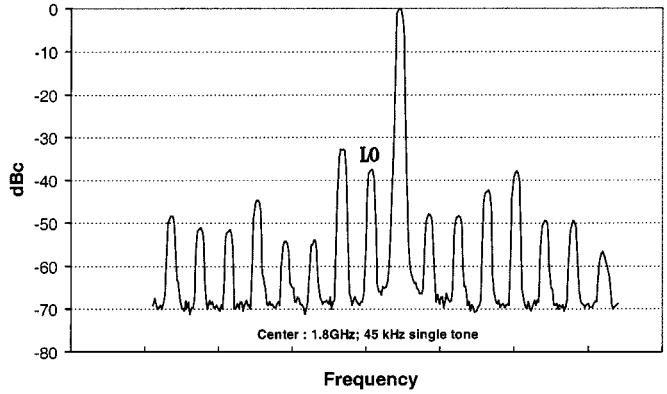


Fig. 19. TX output spectrum with a 45-kHz single-tone LF input.

order to select all the gain levels. The resulting low-frequency GMSK signal is shown in Fig. 14. All measurements are performed with a resolution bandwidth of 30 kHz, the value that is generally used in the DCS-1800 specifications.

To measure the PLL frequency synthesizer, an HP signal generator is used as the 26-MHz reference frequency source. Its low-frequency stability is worse than that of a crystal oscillator, resulting in a slightly higher in-band phase noise for the PLL. The phase-noise spectrum is plotted in Fig. 15. The phase-noise measurement at offsets higher than 5 MHz is not accurate due to the delay line of the dedicated phase-noise measurement system. The measured phase noise is as low as −125.8 dBc/Hz at 600-kHz offset and −143.7 dBc/Hz at 3 MHz offset, exceeding the DCS-1800 specs with almost 10 dB (see the Appendix). The in-band phase noise is measured to be less than −81 dBc/Hz. The settling behavior of the PLL is shown in Fig. 16. When synthesizing a 104-MHz step (four prescaler moduli), the PLL settles to a 100-Hz accuracy in 226 μs. This is faster than half a DCS-1800 time slot, which means that the PLL meets both the generic and high-speed settling specification (see the Appendix). The spurious suppression is measured to be better than −84 dBc. The actual spur level is lower than the noise level of the spectrum analyzer and could therefore not be

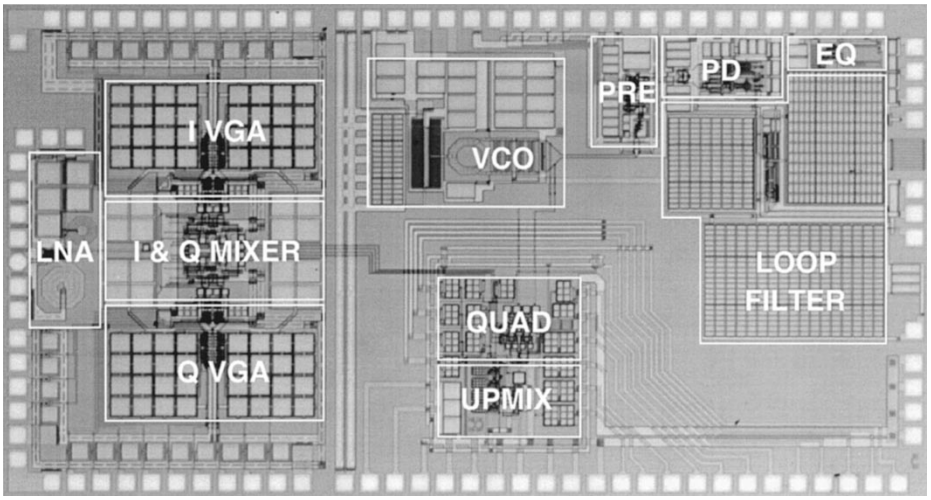


Fig. 20. Chip microphotograph.

measured. The tuning range of the PLL is 10.5%, which corresponds to eight prescaler moduli. The power consumption of the PLL is 70 mW from a 2-V power supply. The fully integrated low-phase-noise VCO is responsible for almost 70% of the total power consumption. The rather high VCO power consumption is due to the excellent phase-noise performance and not due to the extra load of the polyphase filter.

Fig. 17 shows the TX output signal. The GMSK output spectrum at 1.8 GHz, measured at 30-kHz RBW, is compared to the European Telecommunication Standard Institute (ETSI) DCS-1800 requirement mask [17]. Fig. 18 has been added to show that the noise and the spurious at a larger distance (>1.8 MHz) from the carrier (measured with a 100-kHz RBW as required by ETSI) are also achieving the ETSI specifications. The measured noise floor is in fact limited by the noise of the baseband quadrature generator. Fig. 19 shows a 45-kHz single-tone output spectrum at 1.8 GHz. The mirror suppression is better than −33 dBc and the LO feedthrough and all spurious distortion components are below −38 dBc. The measured output power is −13 dBm in a nonideal 50-Ω load, i.e., including board parasitics, connectors, cables, etc. The difference between the simulated 0 dBm and the measured −13 dBm is believed to be caused by a larger on-chip parasitic capacitance value and by not calibrating out the measurement setup.

Even with the smaller output signal, the DCS-1800 noise and distortion specifications are met in this chip.

A chip microphotograph of the 15.4 mm^2 transceiver IC is shown in Fig. 20.The complete circuit at transistor level is shown in Fig. 21. The total power consumption of the 2-V 0.25-μm CMOS transceiver chip is 191 mW (113+70+8) in receive mode and 160 mW (82+70+8) in transmit mode. The experimental results of the transceiver at 2 V are summarized in Table III.

TABLE III
TRANSCEIVER MEASUREMENTS

Low–IF RX			PLL		Direct Upconv. TX	
NF	6.2 dB		Tuning	10.5 %	Output Power	-13 dBm
	White	3.9 dB				
	1/f	2.4 dB				
IMRR	32.2 dB (2 dB - 0.3°)		Settling Time	226 µs for 104 MHz step	Mirror Suppr.	–33 dBc
Gain	54.5 dB		Phase Noise	-125.8 dBc/Hz @600 kHz	LO Feedthr.	–38 dBc
IIP_3	>-6.2 dBm			-143.7 dBc/Hz @3 MHz		
LO Leakage	<-63 dBm		Spurious Suppr.	-84 dBc	GMSK Mask	ETSI
Power	113 mW		Power	70 mW +8 mW buffer	Power	82 mW

VI. CONCLUSION

A 2-V cellular transceiver front-end integrates a receive path and a transmit path with a complete *on-chip* PLL on a single CMOS die, including the loop filter and the *LC* tank. Only a power amplifier, an antenna filter, and a reference crystal are required to build the complete analog part of a DCS-1800 system.

All building blocks feature circuit topologies that have been specially designed to operate comfortably at 2 V, despite the relatively high threshold voltages (nMOS V_T of 0.65 V and pMOS V_T of 0.75 V). This includes the design of a new CMOS folding downconversion mixer topology and a new low-voltage current buffer in the fully-differential-to-single-ended upconverter. To the author's knowledge, this is the lowest voltage CMOS RF front-end published to date. The transceiver IC demonstrates the capability of achieving the analog performance that is required for the class I/II DCS-1800 cellular system in a standard 2-Metal 0.25-μm CMOS process, without the use of extra-thick metal layers (M1: 0.6 μm, M2: 1.0 μm).

APPENDIX
DCS-1800 SPECIFICATIONS

A. Noise Figure Requirement [ETS(I) 300 910, GSM 05.05 v.5.4.1 p. 25, 6.2]

The reference sensitivity level of a class I/II DCS-1800 mobile station lies at −100 dBm, measured at the output of the antenna. In the absence of other signals, this signal must be detectable with an SNR of 9 dB. So the equivalent input noise

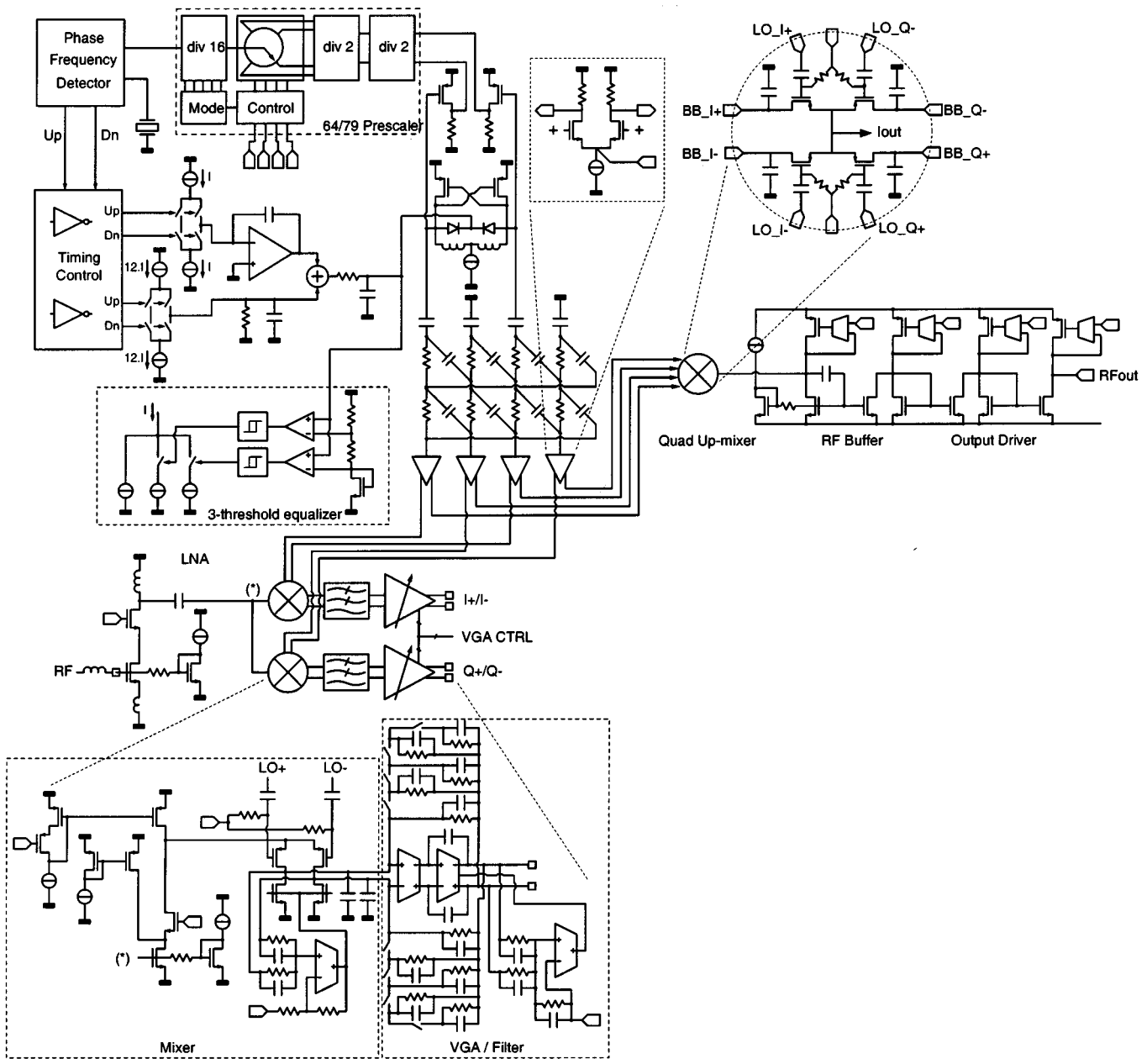


Fig. 21. Topology of the complete transceiver.

power at the antenna input must be lower than -109 dBm. The contribution of 50-Ω noise power can be calculated as -173.87 dBm $+53$ dB (integration over the 200-kHz GMSK bandwidth), and is equal to -120.87 dBm. The noise figure required at the antenna output is

$$-109\ \text{dBm} - (-120.87\ \text{dBm}) = 11.87\ \text{dB}.$$

Since the attenuation of the succeeding antenna filter is 3 dB, the noise figure requirement for the receive path becomes

$$11.87\ \text{dB} - 3\ \text{dB} = 8.87\ \text{dB}.$$

B. Image Rejection Requirement [ETS(I) 300 577, GSM 05.05 v.5.4.1 p. 26, 6.3]

The IMRR specification for the low-IF receiver is set by the adjacent channel interference owing to the channel at 400-kHz offset from the wanted signal. This channel will, after down-conversion, become centered around 300 kHz, 200 kHz above the 100-kHz IF. At 200 kHz, the tail of this adjacent channel directly interferes with the wanted signal and must be suppressed by ensuring a high enough image suppression. The ETSI specification requires that the reference interference performance must be met when the adjacent interferer at 400 kHz is 41 dB larger than the wanted signal. Since the bit error rate (BER) is, by construction, preserved when the *unremovable* tail of the adjacent channel at 200-kHz offset from the wanted signal is interfering with the wanted signal, while its power is 9 dB higher

than the wanted signal, the required image rejection for the adjacent channel at 400-kHz offset from the wanted signal is

$$41\ \text{dB} - 9\ \text{dB} = 32\ \text{dB}.$$

The requirements for the adjacent channel at 200 kHz, which is directly superimposed onto the wanted signal, are less stringent; The reference interference performance must be met when this channel is only 9 dB larger than the wanted signal, and must only be suppressed to the level equal to the co-channel interference specification (-9 dB), requiring only 18-dB mirror signal suppression.

C. Spurious Emission [ETS(I) 300 577, GSM 05.05 v.5.4.11 p. 19, 4.3.3]

The spurious power emissions can not be higher than -47 dBm (20 nW) between 1–12.75 GHz.

D. Intermodulation Requirement [ETS(I) 300 577, GSM 05.05 v.5.4.1 p. 18, 5.3]

A GMSK signal 3 dB above the reference sensitivity ($-100\ \text{dBm} + 3\ \text{dB} = -97$ dBm) must still be detectable with an SNR of 9 dB in the presence of a -49 dBm static sine and a -49 dBm GMSK signal. Since the nominal loss of the RF filter is 3 dB, the two interferers that occur at the input of the receiver are both -52 dBm. The GMSK interferer that is generated due to third-order intermodulation can under these conditions not be larger than an equivalent input signal with the following power:

$$-97\ \text{dBm} - 3\ \text{dB} - 9\ \text{dB} = -109\ \text{dBm}.$$

The required IIP_3 to meet this specification is thus ($\text{IIP}_3 = P_{\text{in}} - \text{IM}_3/2$):

$$-49\ \text{dBm} - 3\ \text{dB} + (-49\ \text{dBm} - 3\ \text{dB} - (-109\ \text{dBm}))/2 = -23.5\ \text{dBm}.$$

E. Out-band Phase-Noise Requirements [ETS(I) 300 910, GSM 05.05 v. 5.4.1 p. 22,5.2 & p. 25,6.2]

The phase-noise requirement of the frequency synthesizer originates from the downconversion of unwanted signals by the carrier's phase noise onto the desired signal, corrupting the SNR. The most critical unwanted signals that can be downconverted onto the desired signal are the adjacent channel at 400 kHz, which can be 41 dB larger than the wanted signal, the -43 dBm blocking signal at 600 kHz, and the -26 dBm blocking signal at 3 MHz. The channel width is 200 kHz. The reference sensitivity level is -100 dBm, but the blocking levels are defined for "a useful signal at frequency f_0, 3 dB above the reference sensitivity level." In order to obtain a SNR of 9 dB after downconversion for further signal processing, the phase noise needs to be lower than

At 400 kHz :

$$\begin{aligned} L\{400\ \text{kHz}\} &= -41\ \text{dB} - 9\ \text{dB} - 10.\log(200\ \text{kHz}) \\ &= -103\ \text{dBc/Hz} \end{aligned}$$

At 600 kHz:

$$\begin{aligned} L\{600\ \text{kHz}\} &= (-100\ \text{dBm}) + 3\ \text{dB} \\ &\quad - (-43\ \text{dBm}) - 9\ \text{dB} - 10.\log(200\ \text{kHz}) \\ &= -116\ \text{dBc/Hz} \end{aligned}$$

At 3 MHz:

$$\begin{aligned} L\{3\ \text{MHz}\} &= (-100\ \text{dBm}) + 3\ \text{dB} \\ &\quad - (-26\ \text{dBm}) - 9\ \text{dB} - 10.\log(200\ \text{kHz}) \\ &= -133\ \text{dBc/Hz} \end{aligned} \tag{3}$$

Assuming that the phase noise of a frequency synthesizer has a -20 dB/dec roll-off for the critical offset frequencies, the phase-noise specification at 3 MHz can be calculated to be the most stringent.

F. In-band Phase-Noise Requirements

The in-band phase-noise requirement originates from unwanted mixing of the phase-noise spectrum by the desired signal itself. The SNR after downconversion must be at least 30 dB. Numerical convolution has been applied to determine the noise specification for this frequency synthesizer, i.e., the in-band phase noise must be less than -80 dBc/Hz integrated over a bandwidth equal to the channel width.

G. Spurious Suppression [ETS(I) 300 910, GSM 05.0.5 version 5.4.1 p. 22 5.1 and p. 25 6.2]

A spur can be seen as a LO signal for a possible blocking signal, which is maximally -26 dBm. Under these conditions, a -97 dBm wanted signal (reference sensitivity of 100 dBm $+3$ dB) must be detectable with an SNR of 9 dB, resulting in a spurious specification of -80 dBc.

$$-97\ \text{dBm} - 9\ \text{dB} - (-26\ \text{dBm}) = -80\ \text{dBc}.$$

H. Settling Requirements

The settling requirement is determined by the high-level system requirements for DCS-1800. The PLL must be able to switch between RX and TX paths in one and a half time slot. A DCS-1800 time slot is 577 μs, setting the settling spec to 865 μs. For the high-speed data communication service of DCS-1800, the specification is more severe: only half a time slot or 288 μs.

I. Spectrum Due to Modulation and Wideband Noise: [ETS(I) 300 910, GSM 05.05 v.5.4.1, p. 33, Figure A.3: DCS 1800 MS Spectrum Due to Modulation]

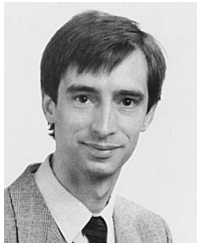
The required GMSK output spectrum of the transmitter is defined in this specification. It has been graphically represented in the measurement section to compare it with the measured output spectrum.

REFERENCES

[1] D. K. Shaeffer and T. H. Lee, "A 1.5-V 1.5-GHz CMOS low-noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, pp. 745–759, May 1997.

[2] J. Janssens and M. Steyaert, "Optimum MOS power matching by exploiting the nonquasi static effect," *IEE Electron. Lett.*, vol. 35, no. 8, pp. 672–673, 1999.

[3] J. Janssens and M. Steyaert, "MOS noise performance under impedance matching constraints," *Electron. Lett.*, vol. 35, no. 15, pp. 1278–1280, 1999.
[4] T. Riley, M. Copeland, and T. Kwasniewski, "Delta–sigma modulation in fractional-N frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 28, May 1993.
[5] J. Yuan and C. Svensson, "New single-clock CMOS latches and flip-flops with improved speed and power savings," *IEEE J. Solid-State Circuits*, vol. 32, pp. 62–69, Jan. 1997.
[6] J. Craninckx and M. Steyaert, "A 1.75-GHz/3-V dual modulus divide-by-128/129 prescaler in 0.7-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 31, pp. 890–897, July 1996.
[7] F. M. Gardner, *Phaselock Techniques*. New York: Wiley, 1979.
[8] D. Mijuskovic and Bayer *et al.*, "Cell-based fully integrated CMOS frequency synthesizers," *IEEE J. Solid-State Circuits*, vol. 29, pp. 271–279, Mar. 1994.
[9] The Mathworks Inc., *Matlab User's Guide, Version 5*, 1997.
[10] Analogy, *Saber User Manual*, 1996.
[11] B. De Muer, N. Itoh, M. Borremans, and M. Steyaert, "A 1.8-GHz highly tunable low-phase-noise CMOS VCO," in Proc. IEEE Custom Integrated Circuits Conference (CICC 00), to be published.
[12] B. De Muer, C. De Ranter, J. Crols, and M. Steyaert, "A simulator-optimizer for the design of low-phase-noise CMOS *LC*-oscillators," presented at the ICECS, Sept. 1999.
[13] M. Borremans and M. Steyaert, "A 2-V low-power single-ended 1-GHz CMOS direct up-conversion mixer," *J. Solid State Circuits*, vol. 33, pp. 359–366, Mar. 1998.
[14] M. Pelgrom *et al.*, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1439, May 1989.
[15] M. Steyaert *et al.*, "A single-chip CMOS transceiver for DCS-1800 wireless communications," in *ISSCC Dig. Tech. Papers*, Feb. 1998, pp. 48–49.
[16] M. Steyaert, J. Janssens, B. De Muer, M. Borremans, and N. Itoh, "A 2-V CMOS cellular transceiver front-end," in *Proc. 2000 IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2000, pp. 142–143.
[17] "Digital cellular telecommunications system (Phase $2+$); Radio transmission and reception," ETS(I), 300 910 (GSM 05.05 version 5.4.1).
[18] J. Crols and M. Steyaert, *CMOS Wireless Transceiver Design*. Boston, MA: Kluwer, 1997.



Michel S. J. Steyaert (SM'92) was born in Aalst, Belgium, in 1959. He received the Masters degree in electrical-mechanical engineering and the Ph.D. degree in electronics from the Katholieke Universiteit Leuven (K.U.Leuven), Heverlee, Belgium, in 1983 and 1987, respectively.

From 1983 to 1986, he received an IWONL fellowship (Belgian National Foundation for Industrial Research) which allowed him to work as a Research Assistant at the Laboratory ESAT at K.U. Leuven. In 1987, he was responsible for several industrial projects in the field of analog micropower circuits at the Laboratory ESAT as an IWONL Project Researcher. In 1988, he was a Visiting Assistant Professor at the University of California, Los Angeles. In 1989, he was appointed by the National Fund of Scientific Research, Belgium, as Research Associate, in 1992 as a Senior Research Associate and in 1996 as a Research Director at the Laboratory ESAT, K.U. Leuven. Between 1989 and 1996, he was also a part-time Associate Professor, and since 1997 he has become an Associate Professor, at the K.U. Leuven. His current research interests are in high-performance and high-frequency analog integrated circuits for telecommunication systems and analog signal processing.

Dr. Steyaert received the 1990 European Solid-State Circuits Conference Best Paper Award, the 1995 and 1997 ISSCC Evening Session Award, the 1999 IEEE Circuit and Systems Society Guillemin–Cauer Award, and the 1991 NFWO Alcatel-Bell-Telephone Award for innovative work in integrated circuits for telecommunications.

Johan Janssens (S'90) was born in Aalst, Belgium, in 1972. He received the M.Sc. degree in electrical engineering in 1995 from the Katholieke Universiteit Leuven, Belgium.

Since 1995, he has been a Research Assistant at the ESAT-MICAS Laboratories of the Katholieke Universiteit Leuven, where he is currently working toward the Ph.D. degree on the design of sub-micron CMOS RF receiver front-ends. His research interests are in high-performance analog integrated circuits for telecommunications.

Bram De Muer (S'00) was born in Sint-Amandsberg, Belgium, in 1973. He received the M.Sc. degree in electrical engineering in 1996 from the Katholieke Universiteit Leuven, Belgium, where he is currently working toward the Ph. D. degree on high-frequency low-noise integrated frequency synthesizers.

He has been a Research Assistant with ESAT-MICAS Laboratories, Katholieke Universiteit Leuven, since 1996. His main research interests are in the area of integrated RF circuits for telecommunications.

Marc Borremans (S'00) was born in Asse, Belgium, on August 15, 1971. He received the M.Sc. degree in electrical engineering in 1995 from the Katholieke Universiteit Leuven, Belgium, where he is working toward the Ph.D. degree in the area of CMOS RF design.

Currently he is a Research Assistant at the ESAT-MICAS Laboratory at the Katholieke Universiteit Leuven. His main research topics are in the area of single-chip full CMOS transmitters for wireless communications, wide-band RF cable transmitters, and high-performance D/A converters.

Nobuyuki Itoh (M'99–A'99) was born in Tokyo, Japan, in 1960. He received the B.S. and M.S. degrees in chemistry from the Science University of Tokyo, Tokyo, Japan, in 1983 and 1985 respectively.

In 1985, he joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he was engaged in the research and development of CMOS device technologies for advanced CMOS gate arrays. From 1986 to 1993, he was involved in the research and development of bipolar device technology and bipolar circuit design for high-speed gate arrays, high-speed logic, and high-frequency analog circuits in the ULSI Research Center. Since 1994, he has been involved in the research and development of high-frequency CMOS analog circuits. He was Visiting Scientist at the Katholieke Universiteit Leuven, ESAT-MICAS, Leuven, Belgium, from 1996 to 1998. He has worked on design of on-chip spiral inductor VCOs and PLLs at the Katholieke Universiteit Leuven. Since 1998, he has been engaged in the research and development of high-frequency analog circuits at the Semiconductor Division, Toshiba Corporation. His current research interests are in high-frequency CMOS integrated circuits for telecommunications.

Mr. Itoh is a member of the Institute of Electronics and Communication Engineers of Japan.