A 5-GHz CMOS Transceiver for IEEE 802.11a Wireless LAN Systems

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***Abstract*—A 5-GHz transceiver comprising the RF and analog circuits of an IEEE 802.11a-compliant WLAN has been integrated in a 0.25-μm CMOS technology. The IC has 22-dBm maximum transmitted power, 8-dB overall receive-chain noise figure, and −112-dBc/Hz synthesizer phase noise at 1-MHz frequency offset.**

***Index Terms*—IEEE 802.11a, low-noise amplifier, OFDM, power amplifier, RF transceiver, synthesizer, wireless LAN.**

I. Introduction

THE GROWING wireless LAN market has generated increasing interest in technologies that will enable higher data rates and capacity than initially deployed systems. The IEEE 802.11a standard, which is based on orthogonal frequency division multiplexing (OFDM) modulation, provides nearly five times the data rate and as much as ten times the overall system capacity as currently available 802.11b wireless LAN systems [1]–[3]. As illustrated in Fig. 1, the 802.11a standard operates in the 5-GHz unlicensed national information infrastructure (UNII) band, which provides a total available signal bandwidth of 300 MHz, as compared to the 85 MHz available for 802.11b. As indicated in Fig. 1, the 802.11a standard supports channel bandwidths of 20 MHz, with each channel being an OFDM modulated signal consisting of 52 subcarriers. Each of the subcarriers can be either a BPSK, QPSK, 16-QAM, or 64-QAM signal. The composite radio frequency (RF) signal has a data rate of up to 54 Mb/s in a 20-MHz channel.

The spectral efficiency of the 802.11a standard comes at the expense of a more complicated transceiver with strict requirements on the radio performance. For example, the use of 64-QAM modulation requires a signal-to-noise ratio (SNR) of 30 dB, which is substantially greater than that required by the FSK modulation in Bluetooth and the QPSK modulation in 802.11b. This high SNR translates to stringent phase noise requirements for the frequency synthesizer and tight I/Q matching constraints for both the transmitter and receiver. OFDM, which is highly desirable because of its resilience to multipath interference, can substantially complicate the transceiver design. Imagine that each of the 52 subcarriers

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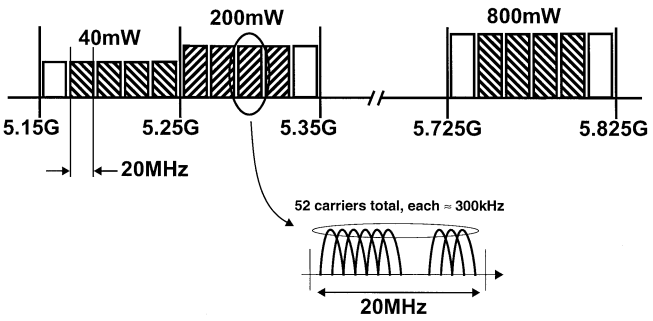

Fig. 1. Channel allocation of the IEEE 802.11a standard within the UNII band.

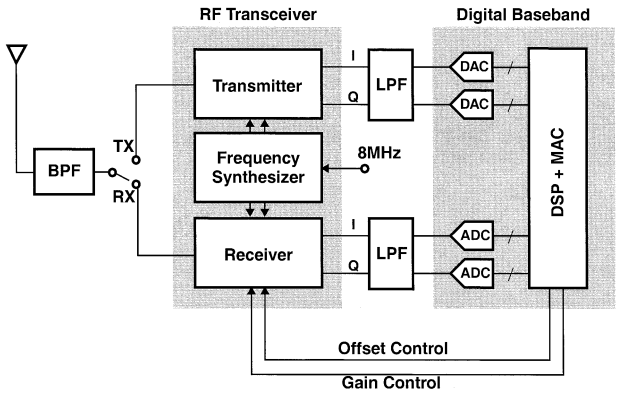

Fig. 2. IEEE 802.11a wireless LAN system architecture.

of the OFDM signal is a single-tone sinewave such that the composite waveform in the time domain will have large peaks and valleys. If the peaks of all 52 sinewaves should line up in time, the peak voltage will be 52 times larger than that of a single sinewave. In this case, the peak-to-average ratio will be $10\log(52) \approx 17$ dB. Therefore, the transceiver must be able to accommodate signals whose peak amplitudes are 17 dB larger than the average signal. This translates into the need for a large power backoff in the transmitter and wide dynamic range in the receiver. In practice, some signal clipping can be tolerated without significantly degrading the radio performance.

The RF frontend and digital baseband functions for an IEEE802.11a wireless LAN standard have been integrated in a standard 0.25-μm CMOS technology as the two-chip transceiver shown in Fig. 2 [4], [5]. This paper describes the RF transceiver chip in detail.

The next section of the paper reviews the architecture and frequency plan of the transceiver. Section III describes the detailed

circuit implementation of individual block, and experimental results are reported in Section IV.

II. Architecture

Shown in Fig. 2 is the overall block diagram of the wireless LAN system consisting of an RF transceiver together with a baseband and media access controller (MAC) processor. The RF transceiver consists of a transmitter, receiver, and frequency synthesizer. The analog baseband inphase (I) and quadrature (Q) input current signals for the transmitter are generated by two 160-MHz, 9-b current-steering digital-to-analog converters (DACs) on the companion baseband chip [5]. On the receiver side, the quadrature signals I and Q at the transceiver output are digitized by two 80-MHz, 9-b analog-to-digital converters (ADCs) on the baseband chip before being processed by the baseband and MAC processor. Off-chip LC low-pass filters are used between the two chips for noise bandwidth limiting and anti-aliasing reasons. No off-chip intermediate frequency (IF) filter is required in the system.

The architecture and frequency plan of the RF transceiver play an important role in the complexity and performance of the overall system. Two of the most common choices in transceiver architecture are direct conversion and the traditional superheterodyne. Direct conversion is usually preferred in a fully integrated design because it avoids the need for an off-chip IF filter and requires only a single frequency synthesizer. However, it suffers from drawbacks such as local oscillator (LO) leakage and frequency pulling due to the fact that the synthesizer operates at the same frequency as the RF signal [6]. The superheterodyne architecture overcomes many of the disadvantages of direct conversion at the expense of an off-chip IF filter and an extra frequency synthesizer [7].

The RF transceiver described in this paper uses a dual conversion architecture with a sliding IF of 1 GHz. Shown in Fig. 3 is the detailed block diagram of the transceiver. On the transmit side, the baseband I and Q signals are first mixed to 1 GHz by a pair of image-reject mixers. The quadrature 1-GHz IF signal is then converted to 5 GHz by the RF mixer. Double image reject mixers are used in the transmitter in order to avoid the need for an IF filter. The upconverted 5-GHz signal is finally transferred to the antenna through an on-chip power amplifier (PA). Since the transmitter output signal is at least 1 GHz away from any of the LO frequencies, no LO pulling is caused by the PA. Furthermore, any LO leakage to the antenna will appear as an out-of-band tone and will not interfere with the operation of other receivers operating in the 200-MHz UNII band.

The receiver frequency plan is very similar to that of the transmitter. An incoming 5-GHz RF signal is first mixed down to IF at 1 GHz and then converted to the baseband quadrature signals. As depicted in Fig. 4, for an RF signal centered at 5 GHz, the image channel is located 2 GHz away at 3 GHz. This undesired signal will be attenuated at least 23 dB by the bandpass gain stages between the receiver input and the RF mixer. By mixing the incoming RF signal with the 4-GHz LO, the RF mixer generates the desired 1-GHz IF and a spurious signal at 9 GHz. The spurious signal is attenuated by the inherent bandwidth limitation of the circuits. As a result, an image-reject mixer is not required in the receiver.

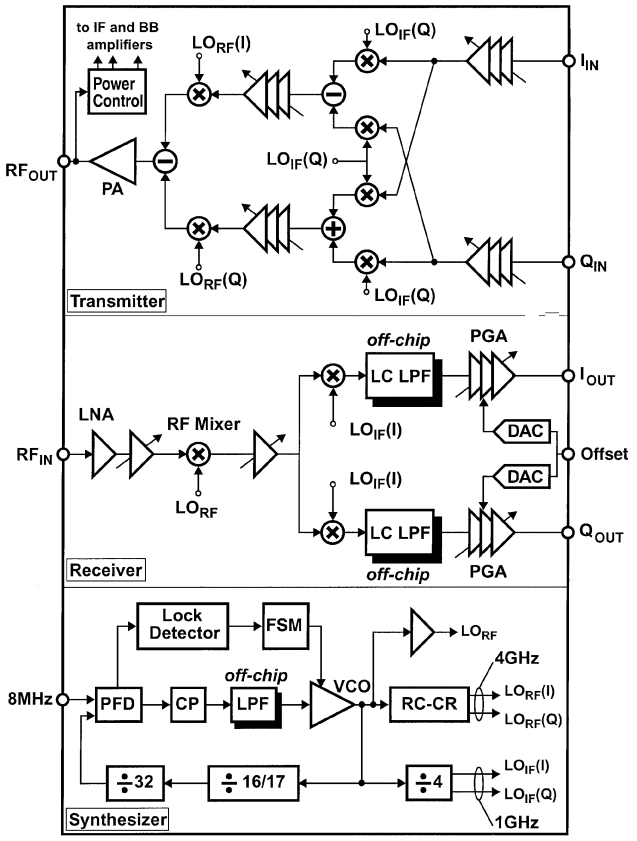

Fig. 3. RF transceiver chip block diagram.

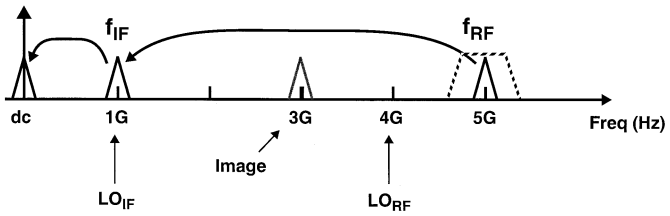

Fig. 4. Receiver frequency plan.

The use of a sliding IF architecture, whereby the $\mathrm{LO_{IF}}$ is generated from the $\mathrm{LO_{RF}}$ using a divide-by-four counter, eliminates the need for two synthesizers. Designed in a twisted-ring architecture [8], the divide-by-four counter can inherently provide very precise quadrature LO signals at 1 GHz, thereby improving the transmitter's image rejection.

III. Circuit Implementation

Advantages and challenges accompany the implementation of the RF transceiver in a CMOS technology. CMOS ultimately provides a significant cost advantage over alternatives. Moreover, scaled CMOS processes generally offer multiple layers of interconnects that allow for the use of integrated inductors with quality factors as high as 10 at a frequency of 5 GHz [9]. These inductors are used extensively throughout the transceiver described in this work in order to enhance the gain of narrow-band

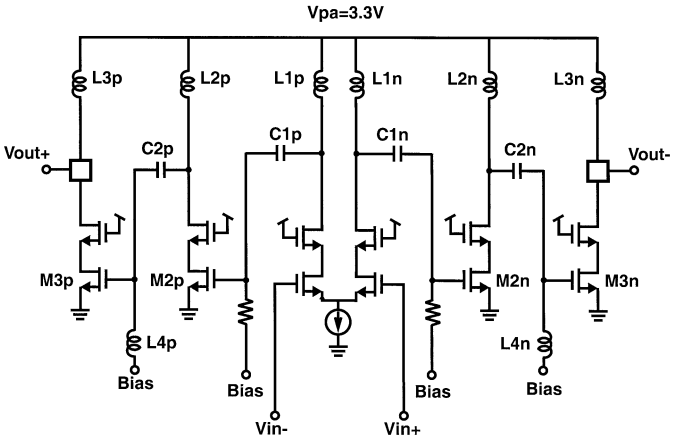

Fig. 5. Simplified PA schematic.

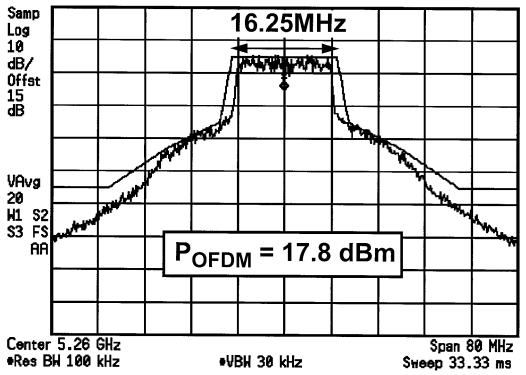

Fig. 6. Measured OFDM output power spectrum.

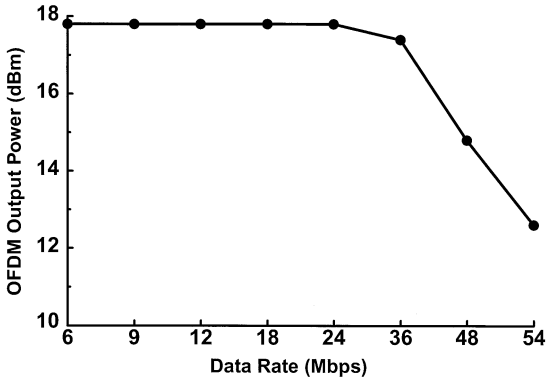

Fig. 7. Transmitter constellation for a 64-QAM signal.

amplifiers. Device characteristics in CMOS can vary significantly over changes in process and temperature, resulting in substantial variations in performance. This drawback can be overcome by using adjustable gain stages and implementing an automatic gain control (AGC) algorithm in the system.

A. Transmitter

As shown in Fig. 3, in the transmit chain, fully differential quadrature baseband input currents are mirrored into the 1-GHz up-conversion mixer and then upconverted to RF by a pair of 4-GHz quadrature mixers. The resulting 5-GHz signal then drives the PA.

The design of the PA is one of the most challenging tasks in the transmitter implementation. As mentioned earlier, the peak-to-average ratio of an 802.11a OFDM signal can exceed 17 dB. This large peak-to-average ratio requires the PA to provide a substantially higher peak output power than its average. For instance, with 6-dB peak-to-average ratio, obtaining 40 mW of average output power requires a PA that is capable of delivering four times as much power or 160 mW. In practical applications, since the signal peaks are infrequent the peak-to-average ratio requirement can be significantly less that 17 dB without major degradation in the overall SNR. In the case of 16-QAM modulation, simulations indicate that a 6-dB peak-to-average ratio degrades the system SNR by only 0.25 dB [10]. However, in practice, peak-to-average ratios as low as 4 dB may meet the error vector magnitude (EVM) and packet error rate (PER) requirements of the IEEE 802.11a specifications.

Fig. 5 shows the three-stage class-A PA employed in the transmitter, wherein each stage consists of a cascoded differential pair. The gate terminals of the cascode transistors are biased at the supply voltage. The cascode topology allows the PA to use a 3.3-V supply for increased headroom and improved linearity. On-chip inductors L4p and L4n form parallel resonances with the gate capacitances of output transistors M3p and M3n so that the level-shifting capacitors C2p and C2n can be kept smaller than 2 pF. The fully differential PA output reduces the effects of parasitic supply and ground inductances. The inductive loads L3p and L3n are implemented with bondwires having estimated inductance of 1.6 nH. Closed-loop power control provides a constant transmitted output power independent of process, temperature, and supply voltage variations. The power control loop, consisting of a peak detector, a comparator, and 24 dB of adjustable transmitter gain in 0.5-dB steps, adjusts the transmitter gain until the PA output matches a pre-programmed level. The key features of this three-stage design can be summarized as: cascoding, inductive loading, and capacitive level-shifting. The transistors are sized to deliver a measured saturated output power ($P_{\rm sat}$) of 22 dBm.

Measurements indicate that the transmitter can provide a peak output power of 22 dBm and an average OFDM output power of 17.8 dBm. Fig. 6 shows a transmitted OFDM spectrum. The measured spectral images and RF carrier leak are -51 and -29 dBc, respectively.

The measured transmit output power is plotted in Fig. 7 as a function of the transmit signal data rate. At low data rates, the measured output power is about 18 dBm and is limited by the spectral mask requirements. At higher data rates, a power backoff of up to 5 dB is needed for the transceiver to meet the dynamic range requirements of the OFDM signal. Fig. 8 illustrates the measured transmit constellation for a single-carrier 64-QAM signal indicating an EVM of 2.3%.

B. Receiver

The receiver mixes the 5-GHz RF input first to the 1-GHz IF and then to the quadrature baseband outputs for digitization by the ADCs on the baseband chip. The entire receive chain is designed to provide sufficient dynamic range and linearity for a

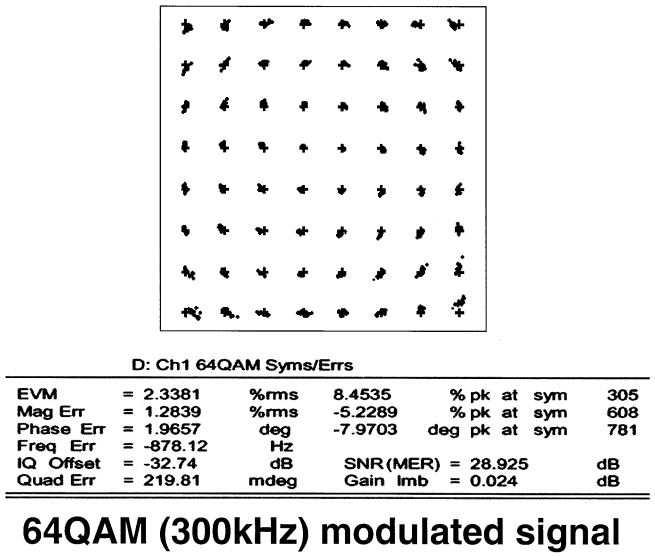

Fig. 8. Measured OFDM output power as a function of data rate.

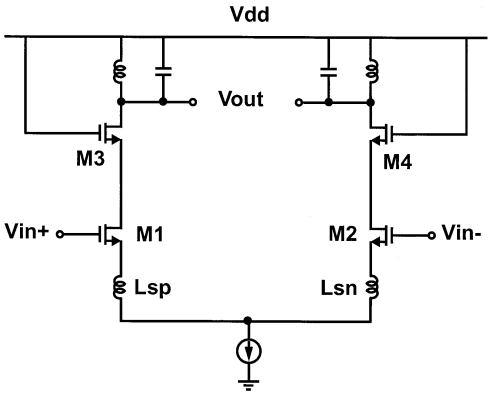

Fig. 9. Simplified LNA schematic.

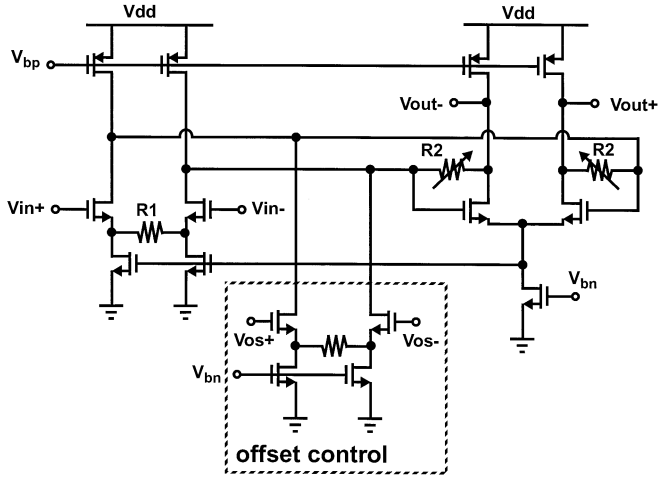

Fig. 10. Simplified PGA gain stage.

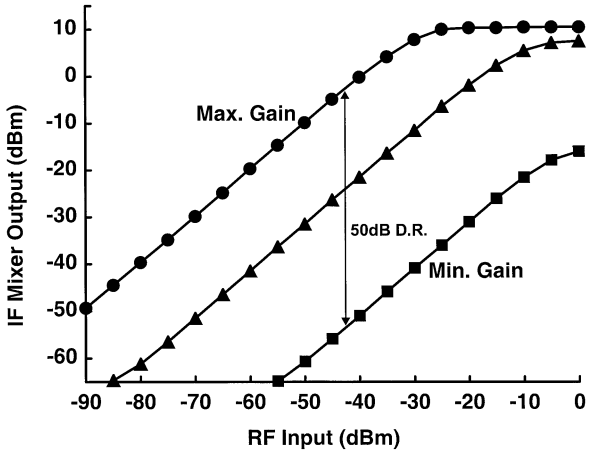

Fig. 11. Receiver gain from the LNA input to the IF mixer outputs.

64-QAM OFDM signal. The RF and IF gain stages have a maximum combined gain of 36 dB that significantly reduces the noise contribution of subsequent baseband stages. The down-converted I and Q signals are passed through the off-chip passive LC channel-select filters and amplified by a programmable gain amplifier (PGA). The PGA comprises a cascade of three stages with a composite gain that can be adjusted from 0 to 41 dB in 1-dB steps. The dc offset of the receive chain is cancelled using two pairs of 6-b DACs. The dc offset cancellation, AGC, and receive signal strength indicator are implemented with algorithms in the baseband chip.

A simplified schematic of the LNA is shown in Fig. 9. The LNA consists of a cascoded differential pair with inductive loads that tune the amplifier output to 5 GHz. The inductive degeneration formed by Lsp and Lsn results in a complex input impedance that can be matched to a 50-Ω source impedance with an off-chip matching network.

Fig. 10 shows the schematic of the amplifier block used in baseband PGAs. The amplifier is a two-stage design in which the first differential pair converts the input voltage to a current inversely proportional to R1. This current is then converted back into voltage by the second differential pair through the shunt feedback resistor R2. The overall gain of the amplifier is established by the ratio of resistors R1 and R2 and is accurate to within 1 dB. Common-mode feedback is conveniently provided from the common source of the second stage to the tail current source of the first. Offset control is provided by a separate differential pair with large resistive degeneration that lowers the gain of the offset control loop.

Fig. 11 shows the measured receiver gain from the LNA input to the IF mixer outputs. The receiver achieves over 50 dB of adjustable RF and IF gain. At minimum gain, the input P1 dB is -8.5 dBm. Shown in Fig. 12 are the I and Q baseband waveforms measured at the receiver output. The receiver achieves an I/Q phase mismatch of 1.5° and amplitude mismatch of 1.5 dB. The measured noise figure of the entire receive chain from LNA to the baseband PGA is 8 dB.

C. Synthesizer

The frequency synthesizer generates the quadrature 1-GHz and 4-GHz LO frequencies needed for the mixers in the receive and transmit chains. As shown in Fig. 3, the synthesizer phase locks an on-chip VCO to an 8-MHz reference. The VCO frequency is fine tuned using P+/N-well varactors D1 and D2. Coarse frequency adjustment is accomplished by switching

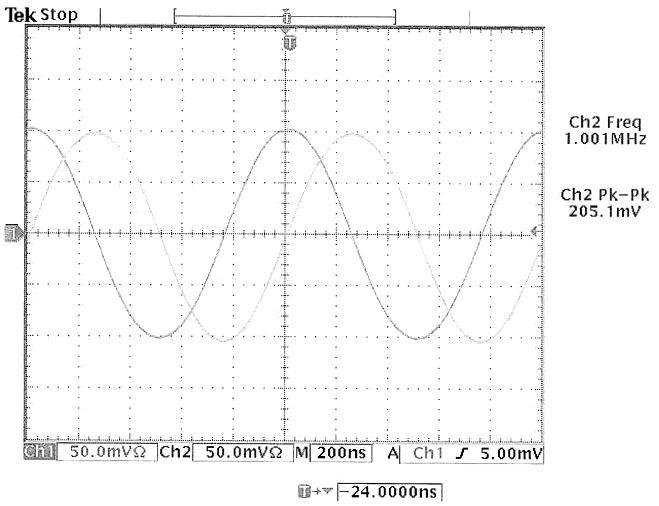

Fig. 12. I and Q waveforms at the receiver output.

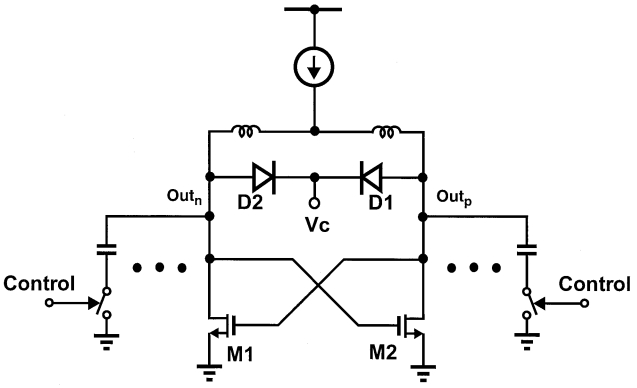

Fig. 13. VCO schematic.

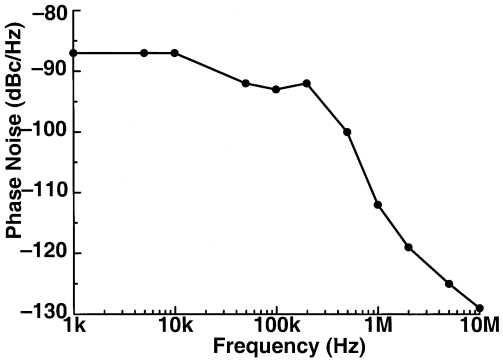

Fig. 14. Synthesizer phase noise profile measured at the PA output.

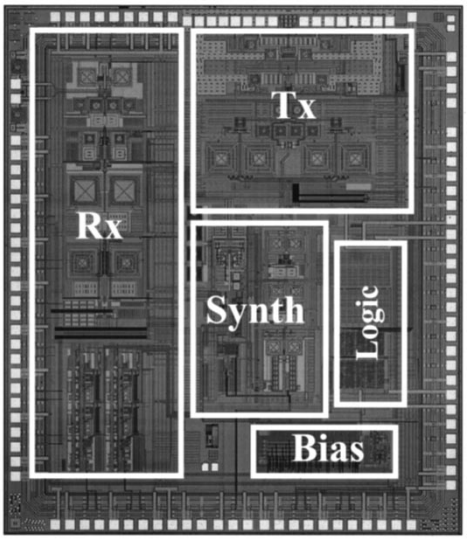

Fig. 15. Die micrograph.

fixed capacitors to the output nodes Out_p and Out_n as depicted in Fig. 13. The switching sequence is determined by a state machine in conjunction with a lock detector circuit. For a particular RF channel if the varactors fail to force the loop to lock, the state machine switches in enough fixed capacitors until the varactors can pull the loop to lock.

The variable divider in the feedback loop consists of a divide by 16/17 dual-modulus prescaler followed by a divide-by-32 and a channel select decoder. The synthesized frequency can be varied from 4.128 GHz to 4.272 GHz, which corresponds to an RF carrier frequency ranging from 5.16 GHz to 5.34 GHz. The quadrature 1-GHz LO signals are generated by a divide-by-four counter. Designed in a twisted-ring architecture, this divider can generate very precise 1-GHz quadrature signals and maintain this precision over process and temperature. The quadrature 4-GHz LOs are generated by passing the VCO waveform through a single-stage RC–CR polyphase filter [11].

The composite phase noise of the synthesizer as measured at the output of the power amplifier is shown in Fig. 14. The close-in phase noise is -87 dBc/Hz at 1-kHz frequency offset. Outside the loop bandwidth of 250 kHz, the phase noise decreases to -112 dBc/Hz at 1-MHz offset.

TABLE I
PERFORMANCE SUMMARY

TX Output Power Level	22 dBm
RX Chain Noise Figure	8 dB
Phase Noise (Δf=1MHz)	–112 dBc/Hz
Supply Voltages	2.5 V & 3.3 V I/O
TX Chain Power Dissipation	790 mW
RX Chain Power Dissipation	250 mW
Synthesizer Power Dissipation	180 mW
Technology	0.25 μm 1P5M CMOS
Package	64-pin LPCC
Die Size	22 mm^2

IV. EXPERIMENTAL RESULTS

The RF transceiver has been integrated in a 0.25-μm, single-poly, five-metal CMOS technology. It occupies a total area of 22 mm^2 and is packaged in a 64-pin leadless plastic chip carrier

with an exposed backside contact for good thermal and electrical performance. A die photograph of is shown in Fig. 15. The transceiver operates from a 2.5-V supply with 3.3-V I/O. The transmit chain dissipates 790 mW of power including a 22-dBm power amplifier. The receiver and synthesizer consume 250 and 180 mW, respectively.

The transceiver has been incorporated into a radio system to form a high-speed, IEEE 802.11a-compliant, wireless LAN. Its typical measured performance is summarized in Table I.

V. Conclusion

An IEEE 802.11a radio transceiver has been designed in a standard 0.25-μm digital CMOS technology for 5-GHz wireless LAN applications. The design avoids the need for any external IF filtering by means of two architectural choices: the use of double image-reject mixers in the transmitter and a very high IF of 1 GHz in the receiver. The use of dual conversion with a sliding IF requires only a single frequency synthesizer, thereby reducing power and area. The integrated transceiver consists of a transmitter with 22 dBm of output power, a receiver with 8-dB receive chain noise figure, and a synthesizer with phase noise of -112 dBc/Hz at 1-MHz offset.

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References

[1] *IEEE Standard 802.11a-1999: Wireless LAN MAC and PHY Specifications—High-Speed Physical Layer in the 5GHz Band*, New York, IEEE, 2000.

[2] W. Eberle, *et al.*, "Digital 72Mbps 64-QAM OFDM transceiver for 5GHz wireless LAN in 0.18μm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2001, pp. 336–337.

[3] P. Ryan, *et al.*, "A single chip PHY COFDM modem for IEEE 802.11a with integrated ADC's and DACs," in *ISSCC Dig. Tech. Papers*, Feb. 2001, pp. 338–339.

[4] D. Su, *et al.*, "A 5GHz CMOS transceiver for IEEE 802.11a wireless LAN," in *ISSCC Dig. Tech. Papers*, Feb. 2002, pp. 92–93.

[5] J. Thomson, *et al.*, "An integrated 802.11a baseband and MAC processor," in *ISSCC Dig. Tech. Papers*, Feb. 2002, Paper 7.2.

[6] A. A. Abidi, "Direct-conversion radio transceivers for digital communication," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1399–1410, Dec. 1995.

[7] S. Sanievelici, *et al.*, "A 900-MHz transceiver chipset for two-way paging applications," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2160–2168, Dec. 1998.

[8] E. J. McCluskey, *Logic Design Principles*. Englewood Cliffs, NJ: Prentice-Hall, 1986.

[9] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, pp. 743–752, May 1998.

[10] R. Van Nee and R. Prasad, *OFDM for Wireless Multimedia Communications*. Norwell, MA: Artech House, 2000.

[11] F. Behbahani, *et al.*, "CMOS mixers and polyphase filters for large image rejection," *IEEE J. Solid-State Circuits*, vol. 36, pp. 873–887, June 2001.

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He worked at Brooktree Corporation, San Diego, CA, during the summer of 1992 on circuit techniques for improving the accuracy of speed testing at the wafer level and was a Research Assistant at the Center for Integrated Systems, Stanford University, from 1992 to 1996. He has been a design consultant with a number of companies including Sony Semiconductors of America, San Jose, CA, and Averant Inc., Alameda, CA. From 1996 to 1999, he was a Member of the Technical Staff at Wireless Access, Inc., Santa Clara, CA, where he designed integrated circuits for two-way paging systems. During 1999 and 2000, he was a part-time Consulting Assistant Professor at Stanford University where he taught graduate courses on RF and mixed-signal IC design. Since December 1998, he has been with Atheros Communications, Sunnyvale, CA, as Analog Design Manager engaging in the design of RF/baseband mixed-signal integrated circuits for wireless LAN applications. His current interests include design of RF and mixed-signal circuits for integrated broad-band wireless networks.

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From 1985 to 1989, he worked as an IC design engineer at Hewlett-Packard Company, Corvallis, OR, and Singapore where he designed full-custom and semi-custom application-specific integrated circuits. From 1989 to 1994, he was a Research Assistant with the Center for Integrated Systems, Stanford University. From 1994 to 1999, he was a Member of Technical Staff with the High Speed Electronics Department of Hewlett Packard Laboratories, Palo Alto, CA, where he designed CMOS analog, RF, and mixed-signal ICs for wireless communications. Since February 1999, he has been with Atheros Communications, Sunnyvale, CA, where he is the Director of Analog Design, engaging in the design and development of integrated CMOS transceivers for wireless LANs. His research interests include the design of RF, analog, mixed-signal, and data conversion circuits. He has also been a Consulting Assistant Professor at Stanford University since 1997.

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He has held summer positions at Texas Instruments, Dallas, TX, and Hewlett Packard Laboratories, Palo Alto, CA, in 1993 and 1994, respectively. From August to November 1998, he was a Research Associate at the Center for Integrated Systems, Stanford, CA, where he conducted research in high-frequency modeling of on-chip passive components and interconnects. In December 1998, he joined Atheros Communications, Sunnyvale, CA, where he has been focusing on CMOS RF IC design and device modeling for wireless LAN applications. Since the spring of 2001, he has been an Consulting Assistant Professor at Stanford University. He has authored or coauthored more than 15 technical articles in the area of RF designs and contributed to *The VLSI Handbook* (CRC Press and IEEE Press, 1999).

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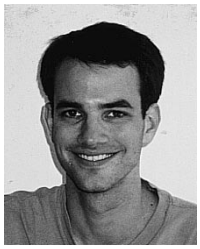
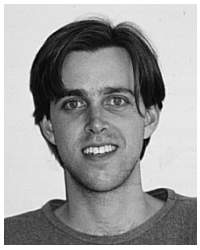
From 1989 to 1992, he was a Manufacturing Development Engineer at Hewlett-Packard, Santa Rosa, CA, where he was responsible for SAW and optical devices. During the spring of 1994, he worked on a low-power A/D converter for hearing aids at Siemens, Munich, Germany. From January 1997 to March 1999, he was a Staff Design Engineer at Level One Communications, San Francisco, CA, where he designed circuits for CMOS wireless transceivers and a voiceband codec. From April 1999 to August 2001, he was at Atheros Communications, Sunnyvale, CA, as Analog Design Manager engaged in the design of CMOS transceivers and data conversion circuits for wireless LAN applications. In August 2001, he cofounded Aeluros Communications, Mountain View, CA, a provider of integrated circuits for high-speed communications.



David Weber was born in Massachusetts in 1973. He received the B.S. degree in electrical engineering from the University of New Hampshire in 1995 and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, in 1996.

From 1996 to 1999, he worked in the components group of Agilent Technologies designing RF power modules for digital cellular phones. In 2000, he joined Atheros Communications, Sunnyvale, CA, as an RFIC designer, where he has worked on power amplifiers, frequency synthesizers, and other mixed-signal circuits for wireless LAN products.

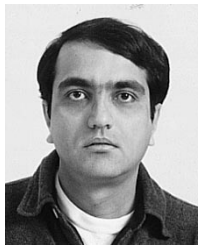


Brian J. Kaczynski (M'00) was born in Beverly, MA, in 1976. He received the B.A.S. degree in physics and English and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, in 1997 and 2001, respectively.

From 1998 to 1999, he worked as an Applications Engineer at Maxim Integrated Products, Sunnyvale, CA. Since December, 1999, he has been with Atheros Communications, Sunnyvale, CA, where he designs analog, RF, and mixed-signal circuits to be integrated into CMOS transceivers for wireless LAN. In addition to analog, RF, and mixed-signal circuit design, his interests include composition and performance of electronic music.

Srenik S. Mehta (S'93–M'96) was born in Passaic, NJ, on August 10, 1971. He received the B.S. and M.S. degrees in electrical engineering from the University of California, Berkeley, in 1992 and 1997, respectively.

From 1995 to 2000, he worked as a Senior Analog Design Engineer at Level One Communications, San Francisco, CA, where he designed CMOS RF and mixed-signal ICs for cordless telephones. His interests included the design of integrated frequency synthesizers, codecs, and wireless transceivers. Since February 2000, he has been with Atheros Communications, Sunnyvale, CA, where he is an Analog Design Manager. He is currently engaged in the design of analog, mixed-signal, and RF IC design for integrated wireless LANs.

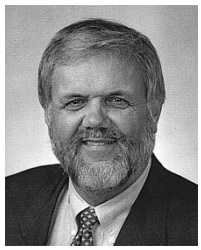


Kalwant Singh received the B.Eng. (First Class Honors) degree in electrical engineering from the National University of Singapore in 1985 and the M.S.E.E. and Ph.D. degrees from Rensselaer Polytechnic Institute, Troy, NY, in 1990 and 1993, respectively. His M.S.E.E. research involved the study of the effects of bandgap narrowing on the performance of Indium Phosphide solar cells, and his doctoral research in nonlinear optics involved the study of the propagation of optical solitons through Erbium-doped fiber lasers and optical amplifiers.

From 1985 to 1988, he was an IC designer with Hewlett-Packard, Singapore. He rejoined Hewlett Packard in 1994 and worked on the design and test of PRML ICs, CCD signal processors, and CMOS Image sensors. He joined Atheros Communications, Sunnyvale, CA, in 2000 and is currently working on the design, characterization, and testing of Wireless LAN CMOS RF ICs.

Sunetra Mendis was born in Sri Lanka. She received the B.S. degree in electrical engineering from Lafayette College in 1988 and the M.S. and Ph.D. degrees in electrical engineering from Columbia University, New York, in 1990 and 1995, respectively.

She was a Member of Technical Staff at Bell Laboratories and Hewlett Packard Laboratories and a Senior Design Engineer at Vanguard - America before joining Atheros Communications, Sunnyvale, CA, in 1999.



Bruce A. Wooley (S'64–M'70–SM'76–F'82) was born in Milwaukee, WI, on October 14, 1943. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1966, 1968, and 1970, respectively.

From 1970 to 1984, he was a Member of the Research Staff at Bell Laboratories, Holmdel, NJ. In 1980, he was a Visiting Lecturer at the University of California, Berkeley. In 1984, he joined the faculty at Stanford University, Stanford, CA, where he is the Robert L. and Audrey S. Hancock Professor of Engineering and the Chairman of the Department of Electrical Engineering. At Stanford, he has also served as the Senior Associate Dean of Engineering and the Director of the Integrated Circuits Laboratory. His research is in the field of integrated circuit design, where his interests include oversampling A/D and D/A conversion, low-power mixed-signal circuit design, circuit design techniques for video and image data acquisition, high-speed embedded memory, high-performance packaging and testing, noise in mixed-signal integrated circuits, and circuits for high-speed communications. He has published more than 130 technical articles and is a coauthor of *The Design of Low-Voltage, Low-Power Sigma–Delta Modulators* (Norwell, MA: Kluwer, 1999). He is a coeditor of *Analog MOS Integrated Circuits, II* (New York: Wiley, 1989).

Prof. Wooley is the current Past President of the IEEE Solid-State Circuits Society. He has served as the Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and as the Chairman of both the International Solid-State Circuits Conference (ISSCC) and the Symposium on VLSI Circuits. He is also a past Chairman of the IEEE Solid-State Circuits and Technology Committee, and he has been a member of the IEEE Solid-State Circuits Council, the IEEE Circuits and Systems Society Adcom, the Executive Committee of the ISSCC, and the Executive Committee of the Symposium on VLSI Circuits. In 1986, he was a member of the NSF-sponsored JTECH Panel on Telecommunications Technology in Japan. He was awarded the University Medal by the University of California, Berkeley and he was an IEEE Fortescue Fellow. He was also a recipient of the IEEE Third Millennium Medal. He received an Outstanding Panelist Award for the 1985 ISSCC and the Winner Editorial Award for papers presented at the 1991 and 1997 ISSCC.