A 2.4-GHz CMOS Transceiver for Bluetooth

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Abstract—A fully integrated CMOS transceiver tuned to 2.4 GHz consumes 46 mA in receive mode and 47 mA in transmit mode from a 2.7-V supply. It includes all the receive and transmit building blocks, such as frequency synthesizer, voltage-controlled oscillator (VCO), power amplifier, and demodulator. The receiver uses a low-IF architecture for higher level of integration and lower power consumption. It achieves a sensitivity of −82 dBm at 0.1% BER, and a third-order input intercept point (IIP3) of −7 dBm. The direct-conversion transmitter delivers a GFSK modulated spectrum at a nominal output power of 4 dBm. The on-chip voltage controlled oscillator has a close-in phase-noise of −120 dBc/Hz at 3-MHz offset.

Index Terms—CMOS integrated circuits, demodulation, frequency modulation, frequency synthesizers, integrated circuits, mixers, radio transceivers, spread-spectrum communication.

Fig. 1. Bluetooth transceiver architecture.

I. INTRODUCTION

THE BLUETOOTH standard defines short-range wireless connection between mobile phones, mobile PCs and other portable devices [1]. It specifies a 2.4-GHz frequency-hopped spread-spectrum system that enables the users to easily connect to a wide range of computing and telecommunication devices without the need for wires or cabling of any kind. Space and cost considerations are among the primary motivators for the drive toward a single-chip radio solution.

Bluetooth uses the unlicensed 2.4-GHz ISM band, and supports a moderate data rate of 1 Mb/s. The modulation scheme is Gaussian binary FSK (GFSK), with frequency deviations of ±160 kHz around the carrier. The transceiver uses a time-division duplexing system. A Bluetooth device must satisfy some certain requirements. It should be low cost and low power to integrate with other portable devices efficiently, and yet it must have a robust performance to function properly along with interferers. Such interferers exist in a noisy RF environment in which several powerful radio signals are present in the proximity of the Bluetooth radio, such as GSM or CDMA signals. This clearly spells great design challenges to realize such a high-performance radio. The following paper presents a low-power and highly integrated transceiver implemented in a digital 0.35-μm CMOS process. The all CMOS design allows the single-chip integration of the radio and baseband chips.

In Section II, the system considerations are discussed, and the proposed transceiver architecture is presented. Section III describes the circuit details of the transceiver building blocks, and in Section IV, the measurement results are presented.

II. TRANSCEIVER ARCHITECTURE

The radio transceiver is fully integrated, including RF and analog sections. The size of the radio transceiver is minimized as a result of full integration of the system. The transceiver architecture is based on a time-division duplexing (TDD) scheme, isolating crosscoupling between transmitter and receiver. Since the system is TDD, the synthesizer can provide different RF local oscillators for the transmitter and receiver. Specifically, the radio transceiver consists of the receiver, the transmitter, and clock generator blocks, as shown in Fig. 1. In this section, details of the receiver, transmitter, and clock generator are discussed.

A. Receiver Architecture

While a direct-conversion architecture is best suitable for FSK receivers [2], it is not used in this design based on the following reasons.

1) Unlike wide-band FSK modulation, GFSK spectrum has considerable energy at zero-IF. Therefore, dc offset and flicker noise [3] may significantly degrade the receiver performance. Particularly, the flicker noise caused by the switches in a current-commutating mixer may be of a magnitude that limits the overall noise figure of the receiver [4], [5].

2) A limiter at baseband cannot be used, since the low-frequency components of the GFSK spectrum produce harmonics which lie inside the desired signal downconverted to a zero IF. This degrades the signal-to-noise ratio (SNR) significantly. This problem may be evaded if an automatic gain control (AGC) is used. However, AGCs are complex and dissipate more power.

On the other hand, a superheterodyne receiver maintains the signal at a higher IF, typically 50 to 200 MHz, and therefore,

it does not compete with flicker noise or dc offset. However, superheterodyne receivers require off-chip filters for channel selection and image rejection. This opposes the goal of single-chip integration, and disqualifies this architecture. In addition to that, driving off-chip low-impedance filters increases the overall receiver current consumption.

The proposed Bluetooth receiver uses a low-IF architecture with 2-MHz intermediate frequency (Fig. 1). The 2-MHz IF positions the desired signal well beyond the flicker noise corner. Moreover, the harmonics of the limited signal, located at 6 MHz and above, are easily removed by a post-limiter bandpass filter (BPF). A higher IF (3 MHz or above) raises the power dissipation of the IF blocks. While an IF of 1 MHz is also a possible choice, removing the dc offset and image signal is more difficult, since they are closer to the desired channel. This disqualifies the choice of 1-MHz IF. Clearly, the IF must be a multiple of 1 MHz to allow the selection of the desired Bluetooth channel.

A low-noise amplifier (LNA) tuned to 2.4 GHz boosts the incoming signal, and I/Q mixers driven by quadrature clock signals downconvert it to a 2-MHz IF. A complex-domain bandpass filter centered at 2 MHz selects the desired channel, and rejects the image signal which falls inside the ISM band, that is, four channels away from the desired signal. Therefore, the image-reject requirement is relaxed and achieved by on-chip complex BPF. Appropriate amount of gain is dispersed between the front-end blocks to keep the noise and linearity as required by the Bluetooth standard.

Following the filter, I/Q limiters amplify the desired channel to a well-defined level, regardless of the input signal power, and the received signal strength (RSSI) is indicated. An analog demodulator at 2-MHz IF detects the GFSK spectrum, and extracts the digital bits at the receiver output.

Since the frequency characteristics of all the IF stages is determined by the RC time constant, an RC calibration circuit is employed to tune RC to the reference crystal frequency (Fig. 1). All capacitors are implemented as digitally controlled switchable array of capacitances. The RC calibration block produces the proper control word by measuring the unit RC time constant.

B. Transmitter Architecture

The transmitter uses a direct-conversion architecture (Fig. 1) to achieve low power consumption, and high level of integration [6]. An on-chip modulator produces FSK signal with ±160-kHz frequency deviation at baseband, followed by I and Q Gaussian low-pass filters to shape the spectrum. Single side-band mixers upconvert the GFSK spectrum at baseband to 2.4 GHz. A class-AB power amplifier (PA) delivers a typical output power of 4 dBm to 50 Ω. The PA linearity is not an issue, since the upconverted spectrum carries the input signal information in its phase, not amplitude. The RC calibration circuit tunes the frequency response of the transmitter filters as well.

Since the transmitter directly upconverts the baseband spectrum to the ISM band, image rejection and LO suppression requirements are relaxed, and achieved on chip. Other in-band spurs are mainly produced due to the upconversion mixer nonlinearity. Thus, the mixers must be designed to meet certain IP3
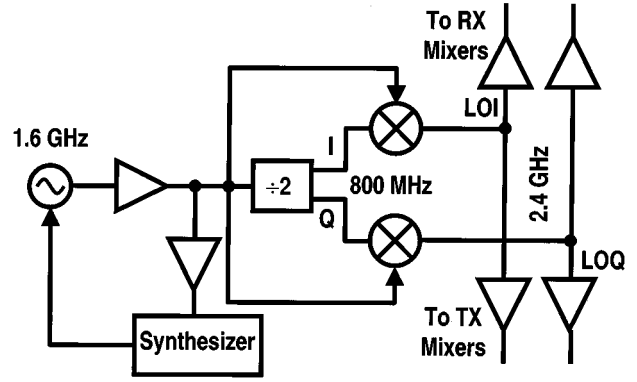

Fig. 2.   Clock generator architecture.

set by the standard. The third-order input intercept point (IIP3) of the transmitter mixers is about 15 dBm in this design.

For a clean LO signal driving the transmitter mixers, out-band spurs are mainly limited to the harmonics of the upconverted signal. These spurs are quite far from the carrier, and removed by on-chip tuned circuits at the transmitter output. In a more practical scenario, the unwanted signals present at the mixer LO port also lead to out-of-band spurs at the transmitter output. This issue is discussed in Section II-C.

The sole LO in a direct-conversion transmitter coincides in frequency with the large modulated signal at the PA output (on the order of 500 mV in Bluetooth). Therefore, in general, this architecture suffers from a major drawback, the disturbance of the local oscillator by the PA, namely, LO pulling by the PA. This problem is more severe in a system which integrates the voltage-controlled oscillator (VCO) and the PA on the same chip. As discussed in the next section, a careful frequency plan avoids the pulling problem in the direct-conversion transmitter.

C. Clock Generator Architecture

As shown in Fig. 2, the clock generator consists of a divide-by-two which produces 800-MHz I and Q signals from the 1.6-GHz VCO, followed by two mixers which generate quadrature clock signals at 2.4 GHz. Buffers between the stages provide isolation, signal amplification, and filtering. The VCO frequency is 800 MHz away from the PA output frequency, and thus, the transceiver is insensitive to direct or harmonic pulling issues. Measurements show that the VCO frequency remains undisturbed at an output power of up to +20 dBm, using an external power amplifier.

Because of the hard-switching action in a Gilbert-type mixer, such as the one used in the clock generator, spurious signals accompany the desired 2.4-GHz clock. For a VCO frequency of f_{VCO}, the clock generator output can be expressed as

$$f_{OUT} = m \times f_{VCO} \pm n \times \frac{f_{VCO}}{2} \qquad (1)$$

where f_{OUT} is the clock generator output frequency. Equation (1) indicates that the mth harmonic of the VCO output mixes with the nth harmonic of the divider output. The closest spurs are the lower sideband at 800 MHz, and the VCO third harmonic mixed with the divider output, producing a spur at 4 GHz. However, these spurs are attenuated by the on-chip LC filters at the
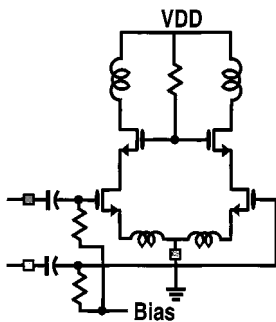
Fig. 3.   Circuit of the low-noise amplifier.

Fig. 4.   Front-end standalone performance.

output of the clock generator mixer and its buffer. The on-chip inductors have a quality factor of 5.5 at 2.4 GHz. Therefore each *LC* circuit attenuates the spur at 1.6 GHz away by about 20 dB. These spurs will be rejected furthermore by the on-chip *LC* filters in the receive and transmit paths. Measurements indicate that all the out-of-band spurs are within the requirements set by the Bluetooth standard, without needing an off-chip preselect filter.

Compared to a conventional dual-conversion transceiver, the advantage of the proposed architecture is that one step of frequency translation is performed inside the clock generator, where noise or linearity are not an issue. Since mixers are inherently noisy and nonlinear, this leads to a better performance at a lower power consumption.

III. CIRCUIT IMPLEMENTATIONS

A. Receiver Front-End

The receiver front-end consists of a low-noise amplifier tuned to 2.4-GHz ISM band, I/Q Gilbert-type mixers, and a complex-domain active-RC BPF centered at 2 MHz [7]. The active-RC topology is chosen because of its superior dynamic range to the other types of active filter implementation [8], [9]. Fig. 3 shows the LNA circuit. It consists of an inductively degenerated common-source differential pair tuned to 2.4 GHz [10]. The fully differential scheme is chosen to be insensitive to the noise at the supply and ground lines. Moreover, the differential LNA drives double-balanced mixers which are insensitive to clock feedthrough and noise at the LO port. The LNA input is matched by the 50-Ω microstrip line and an off-chip floating capacitor. This saves two inductors compared to conventional matching networks which use an LC circuit. The measured input return loss is 16 dB at the center of the band, and remains better than 10 dB across the entire ISM band.

The front-end performance is directly measured through the standalone test chips, and indirectly verified by the actual receiver measurements, which will be discussed in Section IV. Fig. 4 shows the front-end frequency response, dominated by the BPF shape. It is centered at 2 MHz, and the 3-dB bandwidth is 1 MHz. The BPF rejection at 2 MHz away is about 52 dB. The overall voltage gain at 2 MHz IF is about 47 dB. The receiver front end achieves a noise figure of 12 dB, and IIP3 of −7 dBm. The receiver image rejection is mostly dominated by the mismatch between the I/Q signal and clock paths, and is about 42 dB.
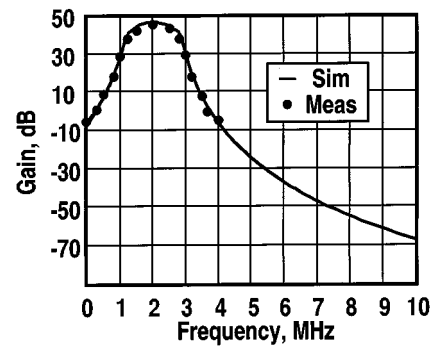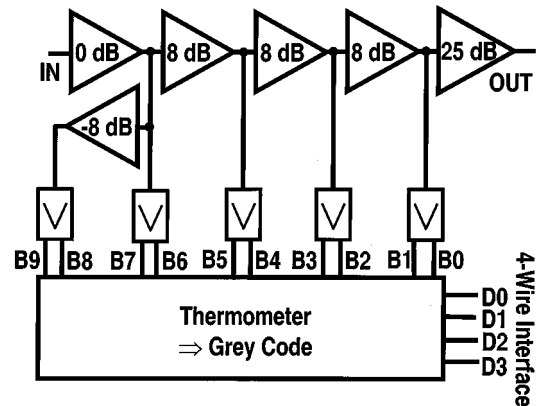

Fig. 5.   Limiter and RSSI block diagram.

B. Receiver IF Blocks

The selected channel at the BPF output is amplified by I and Q limiters to a well-defined level, insensitive to process and temperature variations. Each limiter consists of three stages of 8-dB gain amplifiers, followed by a 25-dB gain stage to limit the received signal (Fig. 5). These stages are ac coupled to remove the dc offset without hurting the desired signal positioned at 2-MHz IF. The received signal strength is indicated by tapping the outputs of these 8-dB gain amplifiers, as well as the output of an 8-dB loss stage outside the signal path. These five outputs connect to 2-bit digital rectifiers. The useful dynamic range of each amplifier is limited on the upper end when the input causes the amplifier to clip, and on the lower end when all the stages are in the linear region. The received signal strength indicator (RSSI) achieves a dynamic range of 40 dB in 4-dB steps. The RSSI measured performance is shown in Fig. 6. It can handle the signals at the receiver input as low as −75 dBm, and as high as −35 dBm. The RSSI measured accuracy is ±1 dB, which is limited by the matching of the gain stages. A logic unit converts the 10 bits at the rectifiers output to a 4-bit Grey code, which is passed to the digital baseband chip through a four-wire interface for the transmitter power control.

Following the limiter is an analog demodulator at 2-MHz IF, as shown in Fig. 7 [11]. A BPF at the input rejects the harmonics of the limited desired signal, which are located at 6 MHz and above. Analog differentiators obtain the frequency information of the received signal, followed by I and Q multipliers, which
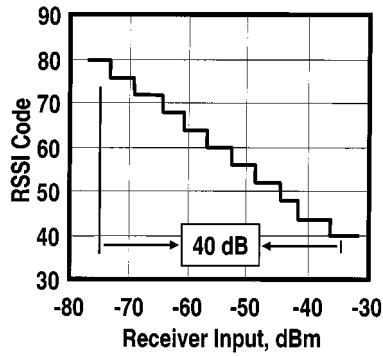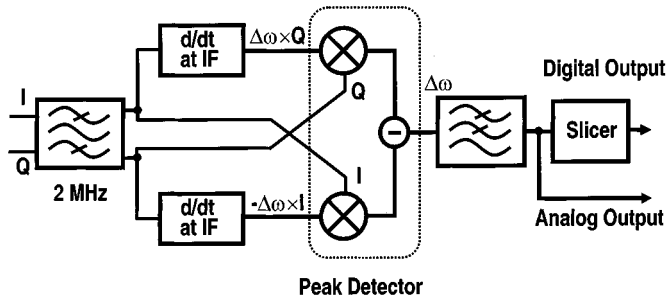
Fig. 6.   RSSI measured performance.

Fig. 7.   IF demodulator block diagram.

detect the envelope of the differentiators output. If the signal at the differentiators input $v_i(t)$ is

$$v_i(t) = A \sin \left(\omega_{\mathrm{IF}} t + \int f(\tau) \, d\tau \right) \qquad (2)$$

where ω_{IF} is the IF frequency (2 MHz), and $f(t)$ is the data, the signal at the multipliers output $v_o(t)$ will be equal to

$$v_o(t) = A \times RC \times f(t) \qquad (3)$$

where RC is the differentiator gain. The RC calibration circuit adjusts the differentiator gain and its center frequency against process or temperature variations. Since the input signal amplitude A is well defined by the limiter, the demodulator gain will be independent of the process or temperature (3). The advantage of this demodulator to conventional analog demodulators is that the differentiators perform at an IF of 2 MHz, rather than zero IF. Otherwise, another step of downconversion from 2-MHz IF to baseband is required. This raises the receiver power consumption and silicon area.

The low-pass filter at the multipliers output removes the unwanted signals accompanying the detected GFSK spectrum. A slicer converts the analog output to digital bits by adjusting the dc level of the analog eye, using peak and valley detectors [11].

C. Voltage-Controlled Oscillator (VCO)

The transceiver uses a single VCO, consisting of a cross-coupled differential pair loaded by on-chip inductors [Fig. 8(a)]. The VCO frequency is tuned by accumulation-mode MOSCAPs [12], [13] which are ac coupled to the VCO output to adjust their dc level at half the supply voltage. This ensures that as the VCO control voltage varies from 0 to V_{DD}, the MOSCAP
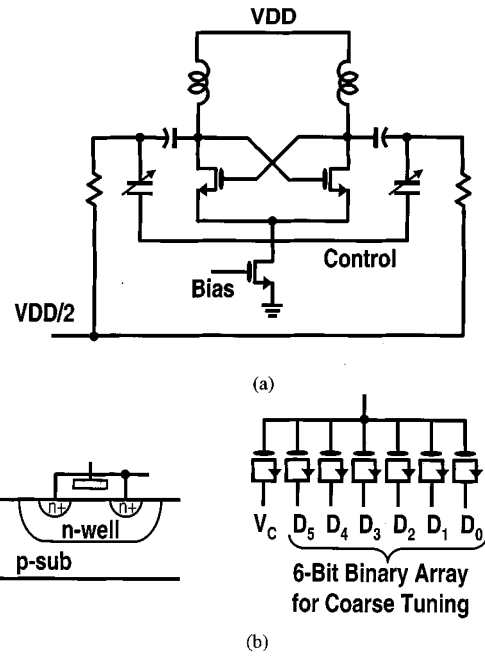

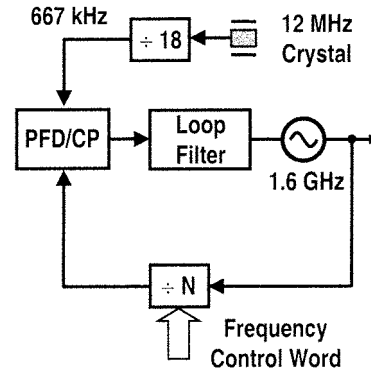Fig. 8.   VCO circuit. (a) VCO core. (b) Details of the varactor.

Fig. 9.   Integer-N frequency synthesizer block diagram.

voltage changes from $-V_{\mathrm{DD}}/2$ to $+V_{\mathrm{DD}}/2$, sweeping the entire MOSFET C–V curve. This leads to the maximum tuning range.

To lower the VCO gain, and as a consequence, to improve its close-in phase noise, the VCO tuning is performed in coarse and fine steps. The coarse calibration uses a 6-bit binary weighted array of MOSCAPs whose control voltages are either connected to V_{DD}, for the maximum capacitance of C_{OX}, or ground, for the minimum capacitance of about $C_{\mathrm{OX}}/3$ [12] [Fig. 8(b)].

Using switches to turn these MOSFETs ON and OFF [14] degrades the LC tank quality factor. Instead, the coarse tuning is performed by turning the MOSCAP itself ON or OFF, that is, by applying a control voltage of either zero or V_{DD} to the MOSFETs. During the coarse tuning, the VCO continuous control voltage is fixed at $V_{\mathrm{DD}}/2$, and the six bits are adjusted to tune the VCO frequency at 1.63 GHz, or equivalently 2.44 GHz, which is the center of the ISM band. Once the coarse calibration is accomplished, the continuous control voltage is connected to the charge pump output, and the desired Bluetooth channel is selected by programming the synthesizer. Thus, the coarse tuning adjusts the VCO frequency against the process variations, whereas the fine tuning covers the desired ISM band.
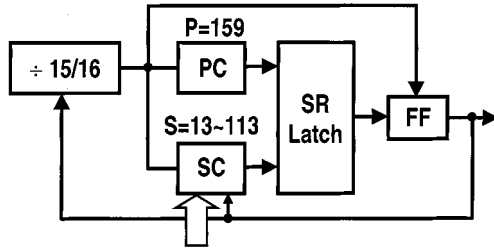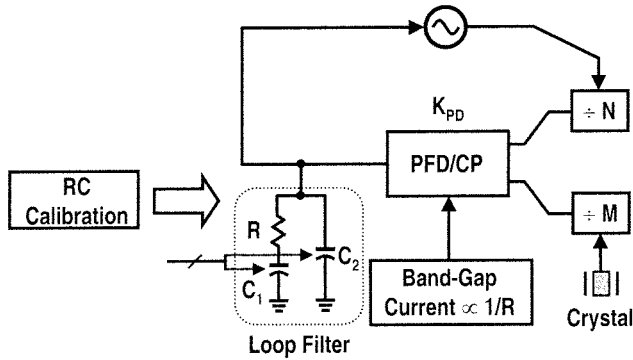
Fig. 10.　Prescaler block diagram.

Fig. 11.　PLL on-chip loop filter.

D. Frequency Synthesizer

The integer-N frequency uses a reference frequency of 667 kHz, produced by dividing the 12-MHz crystal frequency by 18 (Fig. 9). Since the actual transceiver clock frequency is 1.5 times the VCO frequency, this reference leads to 1-MHz channel spacing, as required in Bluetooth. The divide-by-N consists of a prescaler which divides by 15 or 16, a program counter which counts from 0 to 159, and a programmable swallow counter which counts from 0 to 13, and up to 113 (Fig. 10). Therefore, the divide ratio is equal to

$$N = 15 \times 159 + S + 2 = 2400 \sim 2500 \qquad (4)$$

where S changes from 13 to 113. Thus, the entire ISM band (2402–2480 MHz) is covered with some margin.

To lower the number of pins, and to improve the VCO close-in phase noise, the synthesizer loop filter is implemented on chip (Fig. 11). A bandgap adjusts the charge-pump output current inversely proportional to the loop resistor. Therefore, all the loop frequency characteristics are only a function of RC, which is precisely controlled by the RC calibration circuit against the temperature or process variations. The loop capacitors are implemented as digitally controlled switchable array of capacitances.

E. Power Amplifier

The power amplifier is a fully differential circuit, consisting of a preamplifier which provides the required swing, and a driver which uses on-chip matching circuit to 50 Ω (Fig. 12). The preamplifier is a cascode differential pair loaded by an on-chip LC circuit. The cascode scheme assures the stability of the PA, and isolates the PA output from the mixers. The output of the preamplifier is ac coupled to a class-AB differential pair which
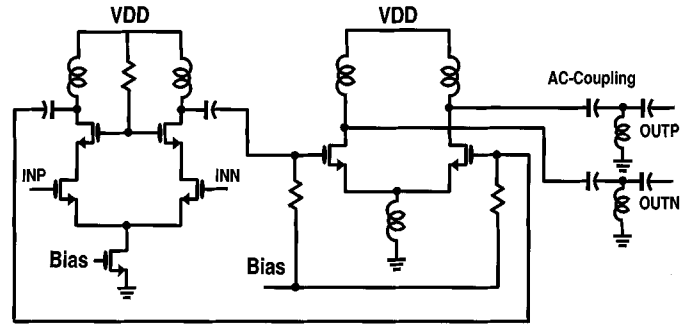

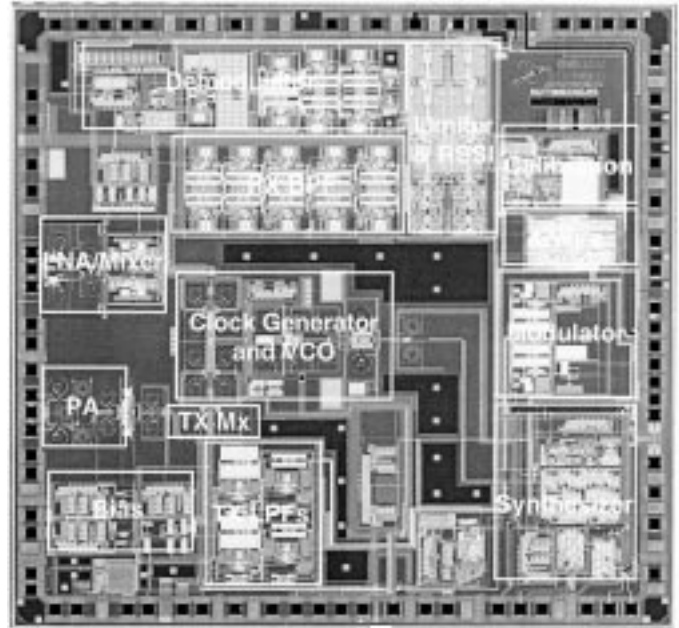Fig. 12.　Circuit of the power amplifier.

Fig. 13.　Transceiver die photo.

uses inductive degeneration. The output resistance of the driver stage is reduced by a shunt inductance, and a series capacitance tunes out the inductive component to match to 50 Ω. The measured return loss at the transmitter output is better than 12 dB across the entire ISM band.

The PA output power is controlled in four steps of 7 dB by changing the bias current of the two stages simultaneously through a bias control circuitry.

IV. Transceiver Measurement Results

This transceiver was fabricated in TSMC 0.35-μm CMOS process. Fig. 13 shows the die photo. All the pads, including the RF pads, use full electrostatic discharge (ESD) protection. Human Body Model (HBM) ESD measurements indicate that all the pads tolerate an electrostatic discharge of up to 2 kV. All the circuits are internally biased by on-chip bandgap circuits.

Fig. 14 shows the receiver bit-error rate (BER) versus the receiver input power. The input is a GFSK modulated signal at 2.44 GHz. At 0.1% BER, as specified, the minimum detectable signal is −82 dBm. This is 12 dB better than the sensitivity required by the Bluetooth standard. Fig. 15 shows the analog demodulator performance, measured by applying a desired GFSK
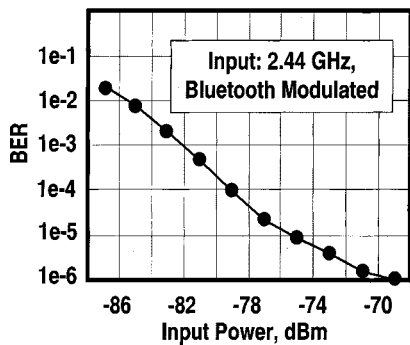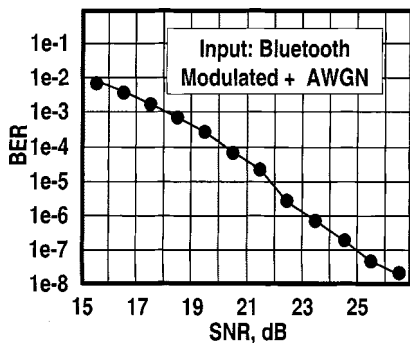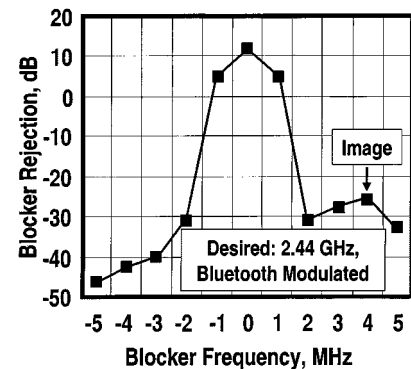
Fig. 14.   Receiver measured sensitivity.

Fig. 15.   Analog demodulator performance.

Fig. 16.   Receiver. (a) In-band blocking performance. (b) Intermodulation performance.

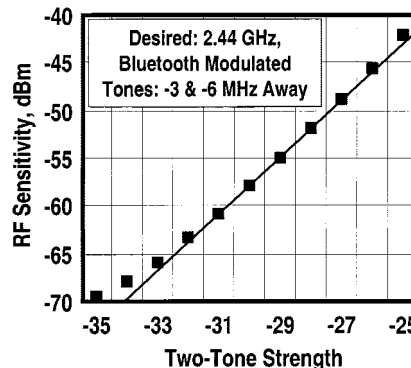Fig. 17.   VCO. (a) Close-in phase noise. (b) Tuning range.

modulated signal on top of known white noise. The applied noise is large enough to bypass the receiver internal noise. Thus, the signal-to-noise ratio (SNR) measured at the receiver input is the same as the one applied at the demodulator input. For 0.1% BER, the required SNR is 18 dB (Fig. 15). The receiver-deduced noise figure is about 12 dB at the LNA input, which matches the front-end standalone measurements discussed in Section III.

The receiver in-band blocking tolerance is illustrated in Fig. 16. Fig. 16(a) shows the receiver blocking rejection in the presence of a GFSK modulated adjacent interferer. The co-channel rejection, set by the demodulator capture range, is 11 dB. The interferers at ± 1 MHz and ± 2 MHz away are rejected by 4 dB and -32 dB, respectively. The blocker at -3 MHz away is attenuated by 40 dB, corresponding to a close-in phase noise of -120 dBc/Hz at 3-MHz offset for the receiver clock. The image blocker, located at 4 MHz away, is rejected by 25 dB. The receiver image rejection is about 42 dB. The receiver intermodulation performance is shown in Fig. 16(b). The interferers are -3 MHz and -6 MHz away from the desired GFSK modulated input. For an interferer power of -32 dBm, the receiver sensitivity is -64 dBm at 0.1% BER. This leads to an IIP3 of about -7 dBm.

Fig. 17(a) shows the standalone VCO phase noise. The close-in phase noise at 3-MHz offset is -127 dBc/Hz at 1.6-GHz center frequency. This translates to a phase noise of -123 dBc/Hz at 2.4 GHz, which is the actual transceiver clock frequency. This is 3 dB worse than the phase noise measured in the clock, and the reason for this 3-dB degradation is the charge-pump noise and other interferers coupling to the VCO control voltage. The VCO tuning characteristic is shown in Fig. 17(b). The VCO calibration circuit adjusts its center
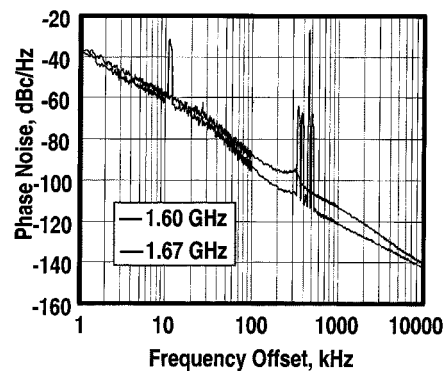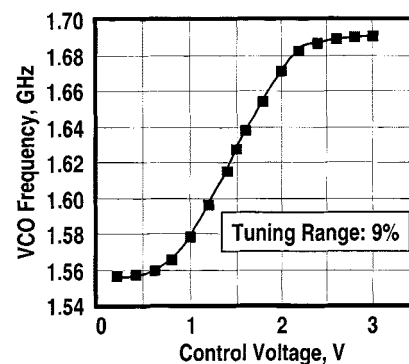
TABLE I
SUMMARY OF TRANSCEIVER PERFORMANCE

Specification	Measurement Results	Bluetooth Requirement
Frequency Band	2.4-2.48 GHz	2.4-2.48 GHz
Sensitivity	-82 dBm	< -70 dBm
IIP3	-7 dBm	> -16.5 dBm
Image Rejection	42 dB	> 29 dB
VCO Phase-noise	-120 dBc/Hz at 3 MHz	< -120 dBc/Hz at 3 MHz
Output Power	4 dBm	-6 to 4 dBm
RX Current Drain	46 mA	Not Specified
TX Current Drain	47 mA	Not Specified
Supply Voltage	2.7-3.3 V	Not Specified
Temperature Range	-25 to 100° C	Not Specified
Technology	0.35 μm CMOS	Not Specified

Output at 2.44 GHz, GFSK Modulated

(a)

1/13 of Symbol Period

(b)

Fig. 18.   (a) Transmitter output spectrum. (b) Corresponding eye diagram.

V. CONCLUSION

A highly integrated low-power transceiver in 0.35-μm CMOS intended for use in Bluetooth applications is reported. A clock generator is shown to resolve the PA pulling issues in a direct-conversion transmitter by offsetting the VCO frequency far from that of PA. The integrated receiver achieves adequate on-chip image rejection and channel selection, using a low-IF architecture and a complex-domain BPF. A global *RC* calibration block is essential to integrate all the receiver and transmitter filters with no external tuning required. Table I summarizes the transceiver performance and compares it to the Bluetooth requirements. This CMOS transceiver meets all the Bluetooth specifications, offering a high-performance low-cost solution for the Bluetooth and future WLAN systems.

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frequency at 1.63 GHz for a control voltage of $V_{\rm DD}/2$. The VCO tuning range is 120 MHz at 1.6-GHz center frequency, which covers the entire ISM band.

The transmitter output spectrum with pseudorandom data applied to its input is shown in Fig. 18(a). The output power at typical condition is 4 dBm, and drops by 2 dB at 85 °C. The transmitter performance is evaluated by processing the eye diagram obtained by demodulating the transmitter output GFSK spectrum [Fig. 18(b)]. The zero-crossing error is $1/13$ of a symbol period, well below the requirement of $1/8$. The modulation index for 10 101 010 pattern is greater than 115 kHz, and for 11 110 000 sequence remains between 145 and 170 kHz.

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