Miniature 3-D Inductors in Standard CMOS Process

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***Abstract*—The structure of the miniature three–dimensional (3-D) inductor is presented in this paper. The proposed miniature 3-D inductors have been fabricated in a standard digital 0.35-μm one-poly-four-metal (1P4M) CMOS process. According to the measurement results, the self-resonance frequency $f_{\rm SR}$ of the proposed miniature 3-D inductor is 34% higher than the conventional stacked inductor. Moreover, the proposed miniature 3-D inductor occupies only 16% of the area of the conventional planar spiral inductor with the same inductance and maximum quality factor $Q_{\rm max}$. A 2.4-GHz CMOS low-noise amplifier (LNA), which utilized the proposed miniature 3-D inductors, has also been fabricated. By virtue of the small area of the miniature 3-D inductor, the size and cost of the radio frequency (RF) chip can be significantly reduced.**

***Index Terms*—CMOS RF circuits, inductors, Q factor, self-resonance frequency.**

I. Introduction

With the continuing reduction of the gate length, the unity-current-gain frequency f_t of the active devices in CMOS technology has exceeded 10 GHz. In addition, CMOS possesses the capability to integrate with the baseband circuits. Thus, CMOS technology seems to be an attractive candidate for low-gigahertz (<5 GHz) radio frequency (RF) applications [1]–[3]. However, the poor characteristics of the passive devices, especially the on-chip inductors and transformers, become the greatest obstacles to realize the fully integrated transceiver in CMOS technology.

Monolithic inductors are widely used in CMOS RF circuits, such as the low-noise amplifier (LNA) [4], voltage-controlled oscillator (VCO) [5], and power amplifier [6]. One of the most important characteristics of the inductor is the quality factor Q. The Q of the inductor significantly affects the performances of the RF circuits and systems, such as the gain/power ratio of the LNA [7], and the phase noise of the VCO [5]. Unfortunately, the spiral inductors implemented in the standard CMOS process suffer from poor quality factors due to the lossy property of the CMOS substrate and the thin metal layers. Therefore, to realize high-Q on-chip spiral inductors in the standard CMOS process is one of the major challenges for CMOS RF researches.

Besides the Q, the self-resonance frequency is also an important consideration for the on-chip inductors. The impedance of the inductor becomes capacitive if the operation frequency exceeds the self-resonance frequency $f_{\rm SR}$. In some cases, such as the LNA and VCO, the highest useful frequency of the inductor is much smaller than $f_{\rm SR}$ because the Q begins to fall off after $f_{\rm max}$, which is the frequency when maximum Q occurs, and equals to zero at $f_{\rm SR}$. Hence, increasing $f_{\rm SR}$ is necessary while the frequency bands of the applications are getting higher and higher. In addition, the planar inductor occupies a large die area [8] and results in long interconnect lines among the passive and active devices. Unfortunately, the long interconnect lines cause excess signal loss due to parasitic resistances and capacitances. Also, the larger die area raises the cost of the RF IC.

In this paper, a structure of miniature 3-D inductors is presented and fabricated in a 0.35-μm standard n-well one-poly-four-metal (1P4M) CMOS process. The proposed miniature 3-D inductor occupies only 16% of the area of the conventional planar spiral inductor with the same inductance and $Q_{\rm max}$. Moreover, the $f_{\rm SR}$ of the proposed miniature 3-D inductor is also 34% higher than the stacked inductor. The basic concepts of the spiral inductor will first be reviewed in Section II. Section III describes the structure of the proposed miniature 3-D inductor. The analytical equations are derived to compare the $f_{\rm SR}$ of the stacked and the miniature 3-D inductors. The simulation result is given and capacitance distribution models are proposed to elucidate the physical meanings of the derived expressions. Experimental results of the proposed inductors are presented in Section IV. A 2.4-GHz monolithic CMOS LNA, which utilizes the proposed miniature 3-D inductors, is also demonstrated in this section. Finally, conclusions are given in Section V.

II. Basic Concepts of the On-Chip Spiral Inductors

Fig. 1(a) shows the typical layout of the on-chip spiral inductor. The on-chip spiral inductor can be defined by the design parameters, which are the outer diameter d, the metal width w, the spacing between the wiring metal s, and the number of turns n. A common simplified lumped-element model [9], [10] is shown in Fig. 1(b). L_s and R_s represent the inductance and series resistance, respectively. C_f models the parasitic capacitance consisting of the overlap capacitance between the spiral inductor and the underpass metal, and the fringing capacitances between metal wires. The oxide capacitance between the metal wire and the substrate is modeled by $C_{\rm ox}$. $R_{\rm sub}$ and $C_{\rm sub}$ are used to model the loss of the silicon substrate.

In CMOS technology, the on-chip inductor suffers from three main loss mechanisms, namely the ohmic, capacitive, and inductive losses [9], [11]. Ohmic loss results from the current flowing through the resistance of the metal tracks. Using a wider metal line can reduce the ohmic loss, however, it also increases the capacitive loss and can cause a decrease in Q and $f_{\rm SR}$ resulting from the larger metal-to-substrate capacitance. The displacement currents conducted by the metal-to-substrate capacitances and the eddy currents generated by the magnetic flux

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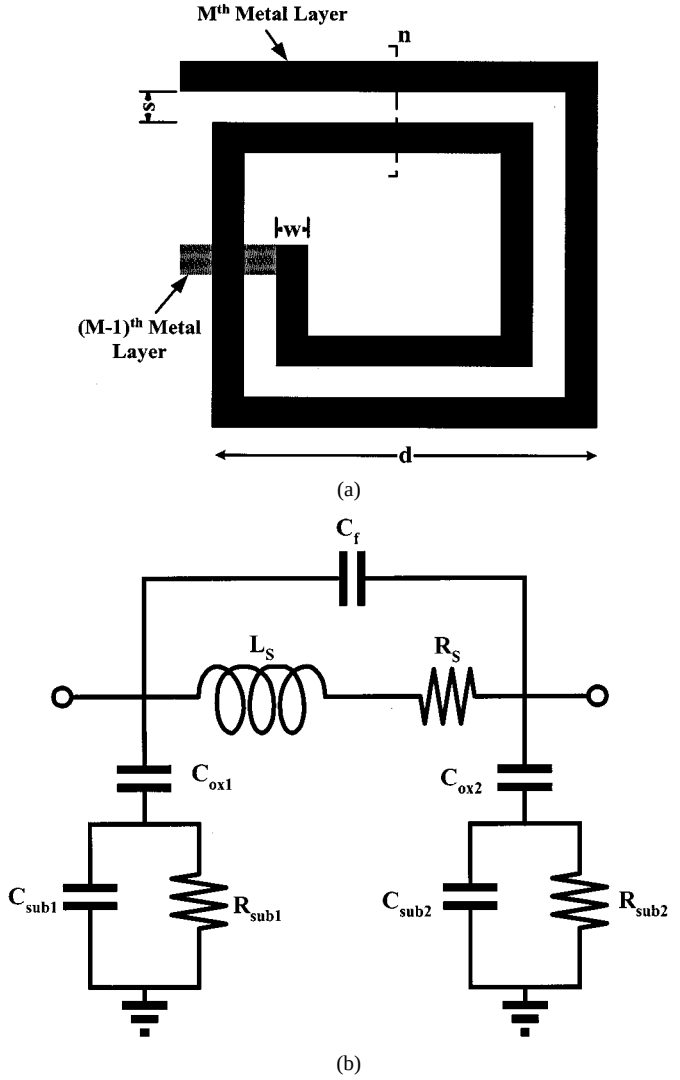


Fig. 1. (a) Layout and design parameters of the on-chip spiral inductor. (b) Simplified lumped-element inductor model.

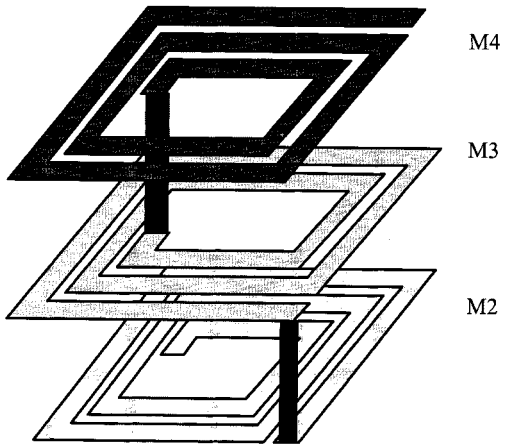


Fig. 2. Structure of the conventional stacked inductor.

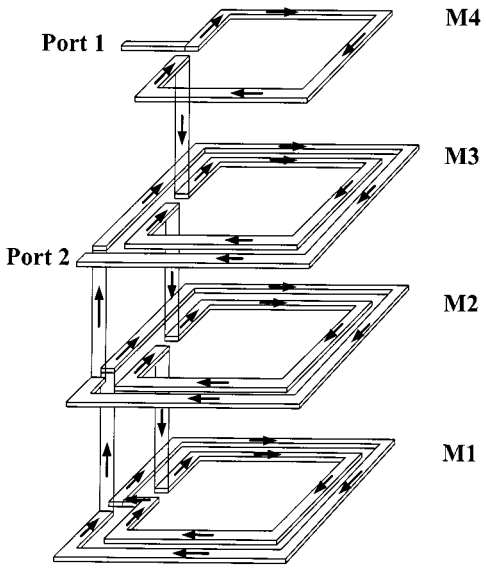


Fig. 3. Structure of the miniature 3-D inductor.

penetrating into the substrate result in capacitive and inductance losses, respectively. Design an on-chip inductor involves trade-offs among various design parameters. For example, increasing the wiring metal width can improve $Q_{\max}$ of the inductor by reducing the resistance of the metal tracks, but this method also increases the area of the inductor. Moreover, this improvement method will be limited by eddy current effect and skin effect in the high frequency, even if the metal width is further increased. Detail design guidelines of the on-chip inductor can be found in [5], [9], and [12]. With the aid of CAD tools, such as ASITIC [13], a nearly optimized inductor can be quickly attained.

The patterned ground shield (PGS) inductor [14], and multilevel parallel shunting inductor [15] have been proposed to improve the quality factor at the price of $f_{\rm SR}$ degradation. The planar spiral inductor often occupies a large die area in the RF IC, and this causes some limitations on placement and routing. Using stacked inductors [16] can save the die area, however, this also sacrifices $f_{\rm SR}$. Hence, an on-chip inductor with small area, high $f_{\rm SR}$, and high quality factor will greatly benefit CMOS RF integrated circuit design.

III. Proposed Miniature 3-D Inductor

A. Conventional Stacked Inductor Structure

The conventional stacked inductor, as shown in Fig. 2, consists of series-connected spiral inductors in different metal layers. Every spiral inductor in the different metal layers may have the same or different turns. The wires wind downward from the top metal layer to the bottom one. A distributed model of the stacked inductor can be found in [17].

B. Proposed Miniature 3-D Inductor Structure

Our proposed miniature 3-D inductor structure is illustrated in Fig. 3, and its distributed model is shown in Fig. 4. Every segment in the distributed model represents a single stacked inductor and $M_{(l,l+1)}$ models the mutual coupling between the adjacent stacked inductors where l is the lth turn. The miniature 3-D inductor consists of at least two or more stacked inductors by series connections, and every stacked inductor has only one turn in every metal layer. For example, if there are two stacked inductors with different diameters, and one of them is a one-turn

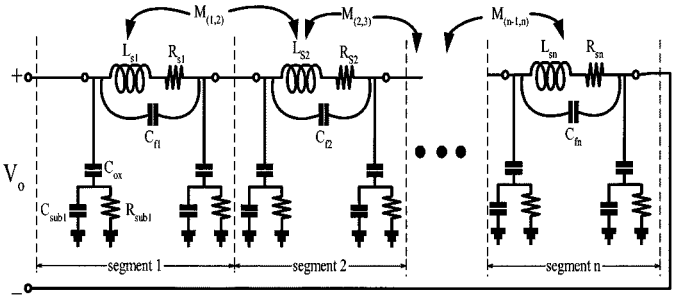


Fig. 4. Distributed model of the proposed miniature 3-D inductor.

stacked inductor from the metal layer 4 to the metal layer 1 and the other is a one-turn stacked inductor from the metal layer 1 to the metal layer 3, then the miniature 3-D inductor is formed by connecting two stacked inductors at the metal layer 1.

C. Derivation of Self-Resonance Frequency

Stacked and miniature 3-D inductors use the multiple metal layers to achieve the required inductances in the small area. Unfortunately, using the lower metal layer also decreases the f_{SR} of the inductor. In order to investigate the f_{SR} of these two types of inductors, analytical equations have been derived. For simplicity, the following assumptions are made.

1) In this experiment, the width of the metal tracks ($\geq$5 μm) is much larger than the metal thickness ($\leq$0.95 μm). Therefore, even for a small spacing between the adjacent metal tracks, the capacitances between them are usually smaller than the interlayer capacitances. Hence, the first assumption ignores the capacitances between the adjacent tracks [17].
2) The spacing when calculating the lengths of the metal tracks is ignored.
3) In the same turn, the voltage potential is equal and is determined by averaging the voltages of the previous turn and the next one.
4) Voltage distribution is proportional to the lengths of the metal tracks [17].

Supposing a 2-layer stacked inductor with inner radius r, metal width w, and n turns in each layer, the voltage profile across the inductor is shown in Fig. 5 and the self-resonance frequency can be derived as follows.

The ratio of the metal length for every turn can be expressed as

$$l_1 : l_2 : \ldots : l_n = [r+(n-1)w] : [r+(n-2)w] : \ldots : [r] \quad (1)$$

where l_k is the metal length of the kth turn. The beginning voltage of the mth turn in the top metal layer is

$$V_{m\mathrm{th,beginning}} = V_0 - \frac{V_0}{2} \times \frac{[1+(n-1)\frac{w}{r}]+\cdots+[1+(n-m+1)\frac{w}{r}]}{[1+(n-1)\frac{w}{r}]+[1+(n-2)\frac{w}{r}]+\cdots+[1+(n-n)\frac{w}{r}]} \quad (2)$$

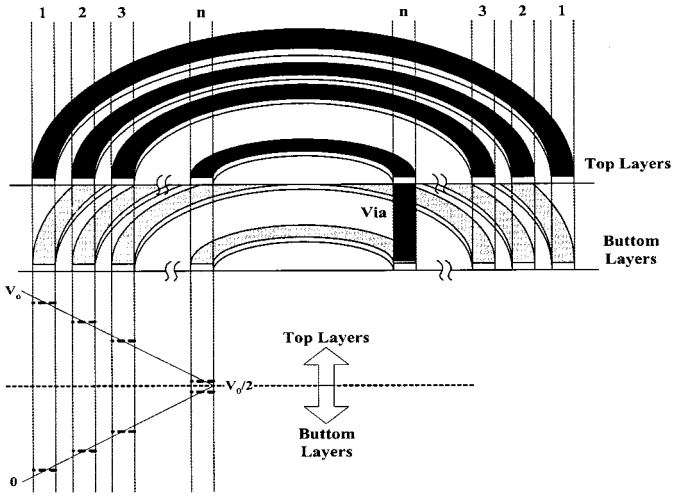


Fig. 5. Voltage profile of n-turn 2-layer stacked inductor.

The ending voltage of the mth turn in the top metal layer is

$$V_{m\mathrm{th,ending}} = V_0 - \frac{V_0}{2} \times \frac{[1+(n-1)\frac{w}{r}]+\cdots+[1+(n-m)\frac{w}{r}]}{[1+(n-1)\frac{w}{r}]+[1+(n-2)\frac{w}{r}]+\cdots+[1+(n-n)\frac{w}{r}]} \quad (3)$$

Hence the voltage of the mth turn in the top metal layer is

$$\begin{aligned} V_{m\mathrm{th,top}} &= \frac{1}{2} \times [V_{m\text{-th,beginning}} + V_{m\mathrm{th,ending}}] \\ &= V_0 - \frac{V_0}{2} \times \frac{[1+(n-1)\frac{w}{r}]+\cdots+[1+(n-m+1)\frac{w}{r}]+\frac{1}{2}[1+(n-m)\frac{w}{r}]}{[1+(n-1)\frac{w}{r}]+[1+(n-2)\frac{w}{r}]+\cdots+[1+(n-n)\frac{w}{r}]} \\ &= V_0 - \frac{V_0}{2} \times \frac{(m-1)\times[2+(2n-m)\frac{w}{r}]+[1+(n-m)\frac{w}{r}]}{n\times[2+(n-1)\frac{w}{r}]} \end{aligned} \quad (4)$$

Using the same method, the voltage of the mth turn in the bottom metal layer can be calculated as

$$V_{m\mathrm{th,bottom}} = \frac{V_0}{2} \times \frac{(m-1)\times[2+(2n-m)\frac{w}{r}]+[1+(n-m)\frac{w}{r}]}{n\times[2+(n-1)\frac{w}{r}]} \quad (5)$$

So, the voltage drop between the top and the bottom metal layer of the mth turn is

$$\begin{aligned} V_{m\mathrm{th,drop}} &= V_{m\mathrm{th,top}} - V_{m\mathrm{th,bottom}} \\ &= V_0 \times \left(\frac{n-m}{n}\right) \times \frac{2+(n-m-1)\frac{w}{r}}{2+(n-1)\frac{w}{r}} \\ &\quad + V_0 \times \frac{1+(n-m)\frac{w}{r}}{n\times[2+(n-1)\frac{w}{r}]}. \end{aligned} \quad (6)$$

Assume C_{m2m} represents the metal-to-metal capacitance per unit area, then the electric energy stored between the top and the bottom metal layers of the mth turn is

$$\begin{aligned} E_{mm} &= \frac{1}{2}CV^2 \\ &= \frac{1}{2}\times C_{\mathrm{m2m}}\times \pi w\times [2r+(2n-2m-1)w] \\ &\quad\times\left[V_0\times\left(\frac{n-m}{n}\right)\times\frac{2+(n-m-1)\frac{w}{r}}{2+(n-1)\frac{w}{r}}\right. \\ &\quad\left.+\,V_0\times\frac{1+(n-m)\frac{w}{r}}{n\times\left[2+(n-1)\frac{w}{r}\right]}\right]^2. \end{aligned} \tag{7}$$

Therefore, the equivalent capacitance between the top and the bottom metal layers of the mth turn is

$$\begin{aligned} C_{m\mathrm{th,m2m}} &= C_{\mathrm{m2m}}\times\pi w\times[2r+(2n-2m-1)w] \\ &\quad\times\left[\left(\frac{n-m}{n}\right)\times\frac{2+(n-m-1)\frac{w}{r}}{2+(n-1)\frac{w}{r}}\right. \\ &\quad\left.+\,\frac{1+(n-m)\frac{w}{r}}{n\times\left[2+(n-1)\frac{w}{r}\right]}\right]^2. \end{aligned} \tag{8}$$

In addition to the metal-to-metal capacitance, the capacitance between the bottom metal layer and the substrate is also considered. Assuming that C_{m2s} represents the metal-to-substrate capacitance per unit area, the equivalent metal-to-substrate capacitance of the mth turn is

$$\begin{aligned} &C_{m\mathrm{th,m2s}} \\ &= C_{\mathrm{m2s}}\times\pi w\times[2r+(2n-2m-1)w]\times\frac{1}{4} \\ &\quad\times\left[\frac{(m-1)\times\left[2+(2n-m)\frac{w}{r}\right]+\left[1+(n-m)\frac{w}{r}\right]}{n\times\left[2+(n-1)\frac{w}{r}\right]}\right]^2 \end{aligned} \tag{9}$$

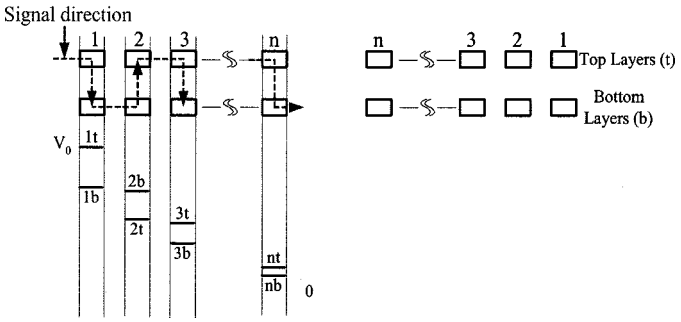


Fig. 6. Voltage profile of n-turn 2-layer miniature 3-D inductor.

Thus, the total equivalent capacitance of the n-turn 2-layer stacked inductor is shown in (10) at the bottom of the page. Now, calculate the total equivalent capacitance of the miniature 3-D inductor, which has all the same design parameters as the n-turn 2-layer stacked inductor. The voltage profile across the miniature 3-D inductor is shown in Fig. 6. After the tedious derivations, the total equivalent capacitance of the miniature 3-D inductor can be calculated as shown in (11) at the bottom of the page.

D. Simulation Results and Discussions

Table I tabulates the total equivalent capacitances, calculated by (10) and (11), of the 4-turn 2-layer stacked inductor and miniature 3-D inductor with different inner radii r, and wiring metal widths w. It shows that the equivalent capacitances of the stacked inductors are larger than those of the miniature 3-D inductors. Because the self-resonance frequency of the inductor can be defined as $f_{\mathrm{SR}}=(2\pi\sqrt{L_{\mathrm{eq}}C_{\mathrm{eq}}})^{-1}$, where L_{eq} and C_{eq} are the equivalent inductance and capacitance, respectively, the analytical analysis indicates that the miniature 3-D inductor has a higher f_{SR} than the stacked inductor.

According to (8)–(11), Fig. 7(a) and (b) shows the accumulated metal-to-metal, metal-to-substrate, and the accumulated

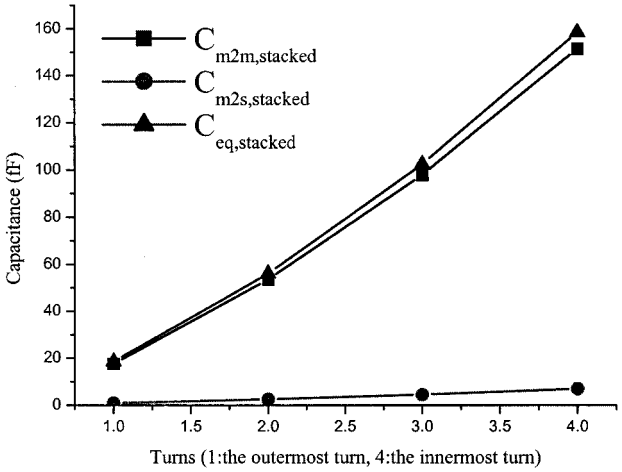
$$\begin{aligned} C_{\mathrm{eq,stacked}} &= \sum_{m=1}^{n}\{C_{m\mathrm{th,m2m}}+C_{m\mathrm{th,m2s}}\} \\ &= \sum_{m=1}^{n}\left\{\begin{array}{l} C_{\mathrm{m2m}}\times\pi w\times[2r+(2n-2m-1)w]\times\left[\left(\frac{n-m}{n}\right)\times\frac{2+(n-m-1)\frac{w}{r}}{2+(n-1)\frac{w}{r}}+\frac{1+(n-m)\frac{w}{r}}{n\times\left[2+(n-1)\frac{w}{r}\right]}\right]^2 \\ +C_{\mathrm{m2s}}\times\pi w\times[2r+(2n-2m-1)w]\times\frac{1}{4}\times\left[\left(\frac{m-1}{n}\right)\times\frac{2+(2n-m)\frac{w}{r}}{2+(n-1)\frac{w}{r}}+\frac{1+(n-m)\frac{w}{r}}{n\times\left[2+(n-1)\frac{w}{r}\right]}\right]^2 \end{array}\right\} \end{aligned} \tag{10}$$

$$\begin{aligned} &C_{\mathrm{eq,miniature-3-D}} \\ &= \sum_{m=1}^{n}\left\{\begin{array}{l} C_{\mathrm{m2m}}\times\pi w\times[2r+(2n-2m-1)w]\times\left[\frac{1+(n-m)\frac{w}{r}}{n\times\left[2+(n-1)\frac{w}{r}\right]}\right]^2 \\ +C_{\mathrm{m2s}}\times\pi w\times[2r+(2n-2m-1)w]\times\left[\frac{\frac{n-m}{2}\left[2+(n-m-1)\frac{w}{r}\right]+\frac{3}{4}\left[1+(n-m)\frac{w}{r}\right]+(-1)^m\frac{1}{2}\left[1+(n-m)\frac{w}{r}\right]}{\frac{n}{2}\left[2+(n-1)\frac{w}{r}\right]}\right]^2 \end{array}\right\}. \end{aligned} \tag{11}$$

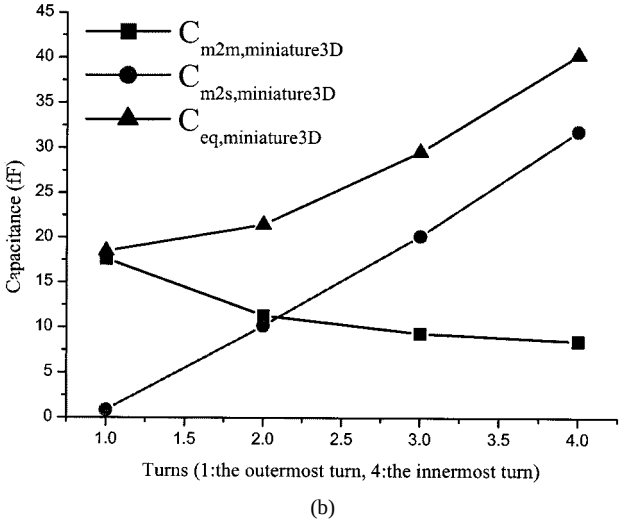
TABLE I
TOTAL EQUIVALENT CAPACITANCES OF THE STACKED INDUCTOR AND THE MINIATURE 3-D INDUCTOR WITH DIFFERENT INNER RADII AND METAL WIDTHS

$C_{eq,stacked}$ (fF) / $C_{eq,\ miniature3D}$ (fF)	r = 10-μm	r = 20-μm	r = 30-μm	r = 40-μm
W = 5-μm	30	49.1	68.4	87.7
	7.7	12.5	17.4	22.3
W = 10-μm	82.3	120.1	158.2	196.5
	21.8	30.8	40.2	49.9
W = 15-μm	157.4	213.4	270.1	327.2
	42.7	55.7	69.4	83.4

<Note>Spacing = 1-μm, C_{m2m} = 4.49e-17 F/μm^2, C_{m2s} = 8.7e-18 F/μm^2 [18]



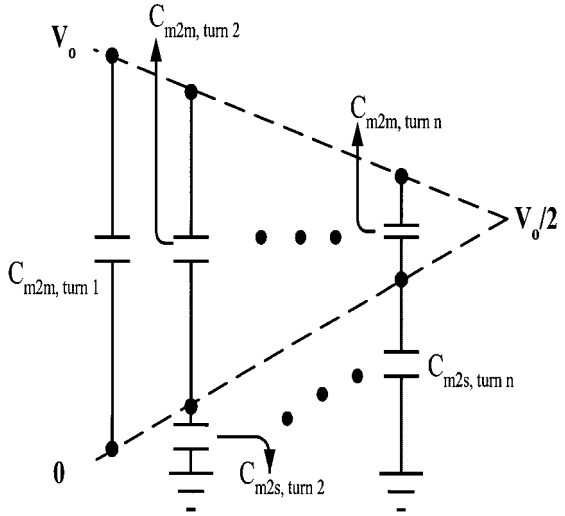
(a)



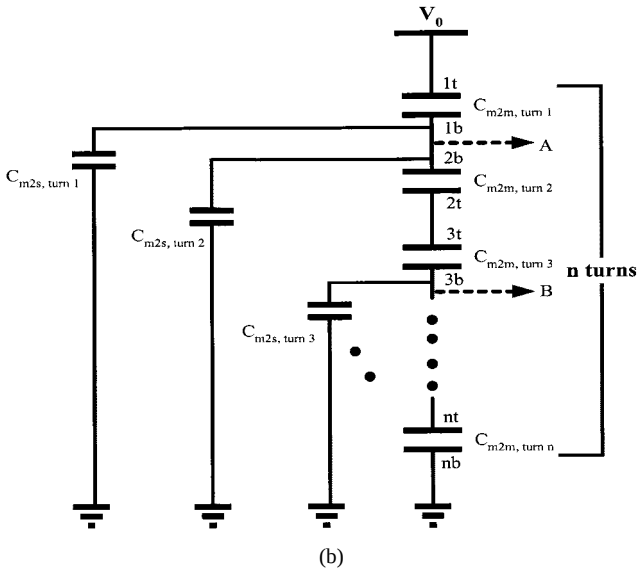
(b)

Fig. 7. Accumulated metal-to-metal, metal-to-substrate, and total equivalent capacitances of 4-turn 2-layer (a) stacked and (b) miniature 3-D inductors.

equivalent capacitances of 4-turn 2-layer stacked and miniature 3-D inductors with 30-μm inner radius and 10-μm wiring metal width, respectively. In Fig. 7(a), the accumulated metal-to-metal $(C_{\mathrm{m2m,stacked}})$, metal-to-substrate $(C_{\mathrm{m2s,stacked}})$, and the accumulated equivalent capacitances $(C_{\mathrm{eq,stacked}})$ increase with an increased number of turns. This result can be explained by



(a)



(b)

Fig. 8. Capacitances distribution models of (a) stacked and (b) miniature 3-D inductors.

the capacitances distribution model, as shown in Fig. 8(a), of the stacked inductor. While increasing the turns of the stacked inductor, more and more metal-to-metal and metal-to-substrate capacitances are generated and parallel connected. Thus, the accumulated equivalent capacitances become larger and larger. Hence, the self-resonance frequency of the stacked inductor decreases while the number of turns increases. As shown in Fig. 8(b), the capacitance distribution model of the miniature 3-D inductor is used to elucidate the results shown in Fig. 7(b). First, while the number of turns increases, more and more metal-to-metal $(C_{\mathrm{m2m,miniature3-D}})$ capacitances are generated and series connected. It results in smaller and smaller accumulated metal-to-metal capacitance. Second, the metal-to-substrate $(C_{\mathrm{m2s,miniature3-D}})$ capacitance is larger than that of the stacked inductor because the voltage drops between the bottom metal layer and substrate may be larger than $V_0/2$ of the miniature 3-D inductor but always smaller than $V_0/2$ in all turns of the stacked inductor. In Fig. 7(b), the accumulated equivalent capacitance $(C_{\mathrm{eq,miniature3-D}})$ is much

TABLE II
TECHNOLOGY PARAMETERS OF TSMC 0.35-μm 1P4M CMOS PROCESS

Layer	Thickness	Resistance
Substrate	> 650-μm	8 Ω-cm
M1	0.67-μm	0.085 Ω/sq.
M2	0.64-μm	0.085 Ω/sq.
M3	0.64-μm	0.085 Ω/sq.
M4	0.925-μm	0.05 Ω/sq.

TABLE III
INDUCTORS USED TO INVESTIGATE THE EFFECTS OF THE DIFFERENT INNER RADII, SPACINGS, AND WIDTHS UPON THE INDUCTANCES AND QUALITY FACTORS

	Inner radius (μm)	Spacing (μm)	Width (μm)	Measured L	Measured Q
Group I	20	1	10	Fig. 9(a)	Fig. 9(b)
	30				
Group II	30	1	15	Fig. 10(a)	Fig. 10(b)
		2			
		5			
Group III	30	1	10	Fig. 11(a)	Fig. 11(b)
			15		

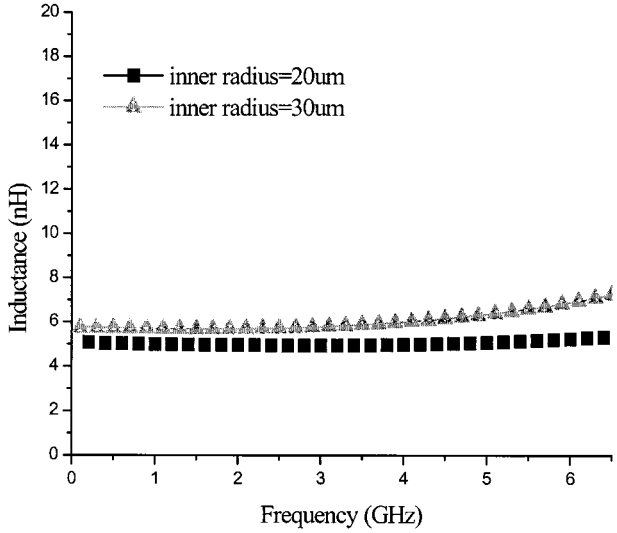
smaller than that of the stacked inductor, and this means the miniature 3-D inductor has higher self-resonance frequency.

To further verify the f_{SR} improvement of our proposed miniature 3-D inductor before fabrication, one miniature 3-D inductor and one stacked inductor, with 2-turn 4-layer 35-μm inner radius, 10-μm metal width, and 5-μm spacing, were simulated by the EM simulator Microwave Office 2000.[1] Results of the EM simulator show that the inductances of these two inductors are the same: 7.8 nH. However, the f_{SR} of the miniature 3-D inductor is 8.6 GHz and of the stacked inductor is 6.2 GHz. EM simulation results prove that the proposed miniature 3-D inductor indeed improves the f_{SR} of the conventional stacked inductor.

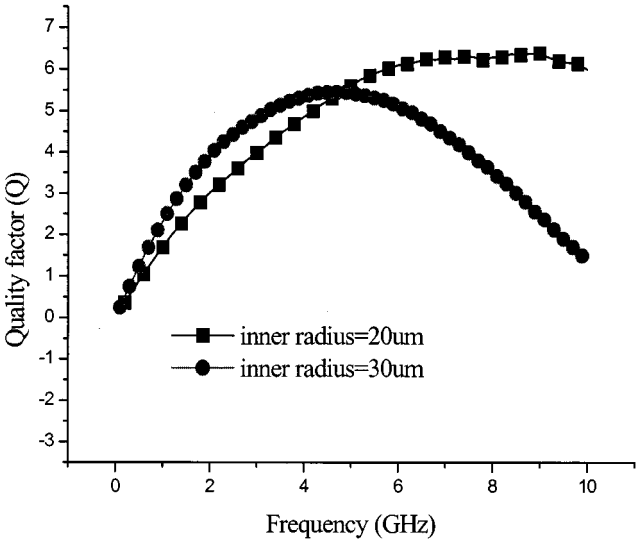
IV. EXPERIMENTAL RESULTS AND APPLICATION

The proposed miniature 3-D inductors have been fabricated in a 0.35-μm standard n-well 1P4M CMOS process. The process parameters are tabulated in Table II. A 2.4-GHz CMOS LNA has also been fabricated in the same process to verify the functions of the miniature 3-D inductors.

[1]Applied Wave Research, Inc. [Online.] Available: http:// www.mwoffice.com



(a)



(b)

Fig. 9. (a) Inductances and (b) quality factors of the miniature 3-D inductor with different inner radii.

A. Measurement Results of Miniature 3-D Inductors

Table III lists the fabricated 2-turn 4-layer miniature 3-D inductors to assess their characteristics. Fig. 9(a) shows that the inductance with the larger inner radius has the larger inductance due to larger magnetic flux, but it also suffers from low quality factor and self-resonance frequency, as shown in Fig. 9(b). In this experiment, the different spacings did not have much influence on inductance, as shown in Fig. 10(a). Fig. 10(b) shows that the inductor with the larger spacing has the higher quality factor in the high-frequency range, and this result coincides with [13]. Fig. 11(a) and (b) should be carefully examined to avoid incorrect conclusions. The wider metal width did not improve the quality factor in this experiment due to the higher resistance of the larger outer diameter. In this case, the miniature 3-D inductor with 20-μm metal width has a higher quality factor below 2.5-GHz than the one with 15-μm metal width. In the high-frequency range, the wider metal width does not help reduce the resistance due to the skin effect; moreover, the wide metal width

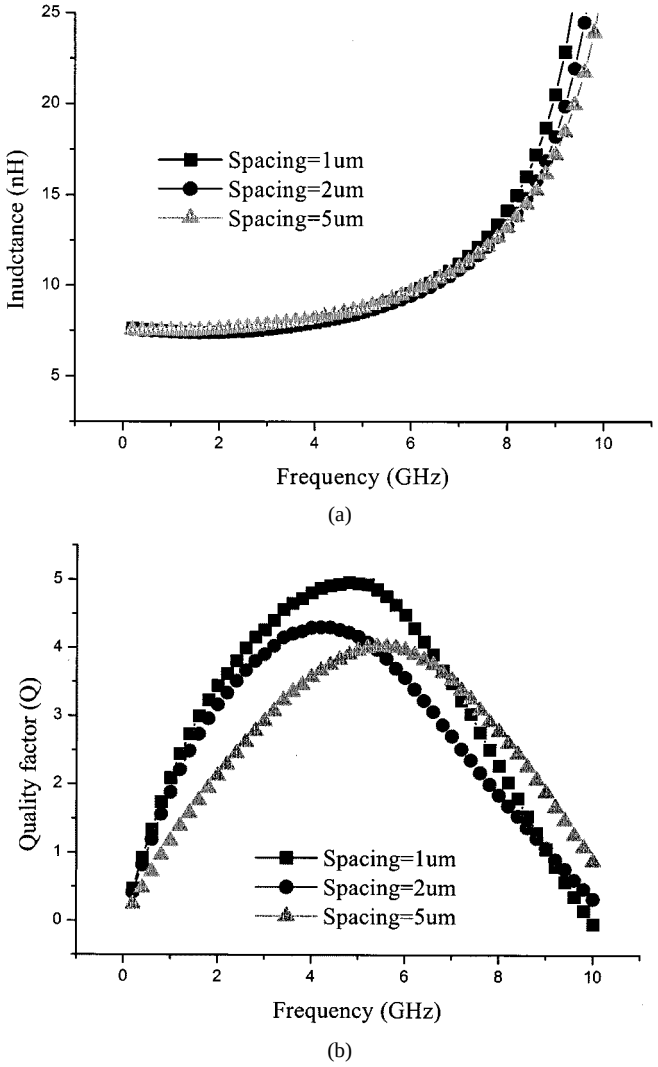


Fig. 10. (a) Inductances and (b) quality factors of the miniature 3-D inductor with different spacings.

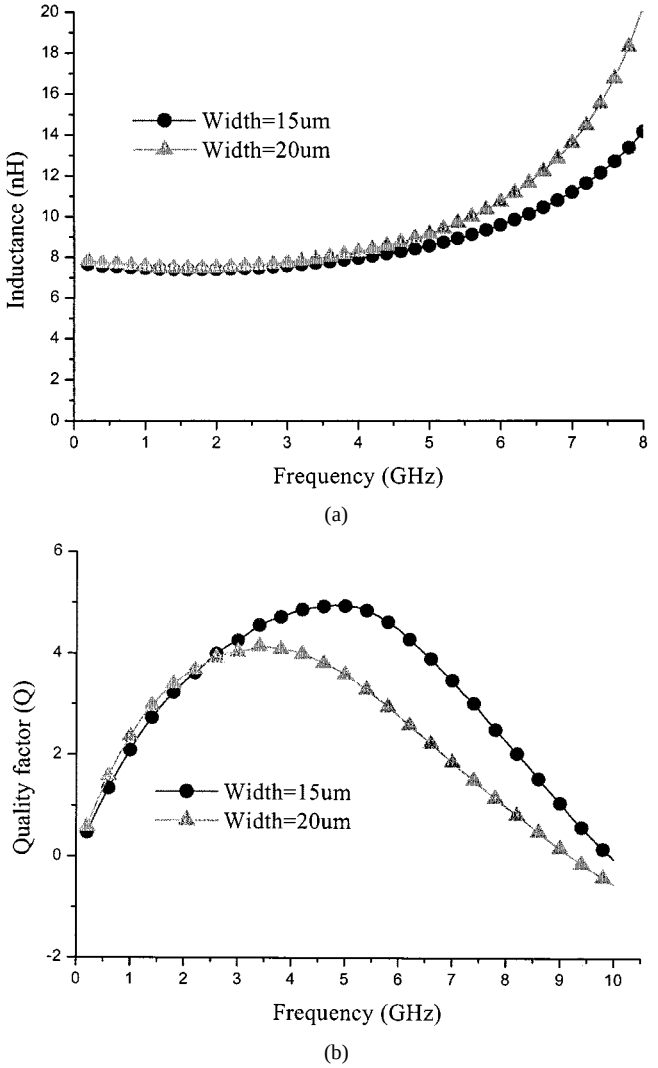


Fig. 11. (a) Inductances and (b) quality factors of the miniature 3-D inductor with different metal widths.

contributes more energy loss through the larger metal-to-substrate capacitance. Thus, the quality factor of the miniature 3-D inductor with 10-μm metal width is higher than the one with 15-μm metal width in the high-frequency range.

A miniature 3-D inductor consists of two or more series-connected single-turn stacked inductors, and thus the coupling should be generated between the adjacent stacked inductors. For a 2-turn 4-layer miniature 3-D inductor, the inner and outer stacked inductors were fabricated and measured to extract the coupling factor. L_{inner} represents the inductance of the inner stacked inductor with 40-μm inner diameter and 15-μm metal width, and L_{outer} represents the inductance of the outer stacked inductor with 56-μm inner diameter and 15-μm metal width. According to the following equations

$$L_{\text{total}} = L_{\text{inner}} + L_{\text{outer}} + 2M \tag{12}$$

$$M = K\sqrt{L_{\text{inner}} L_{\text{outer}}} \tag{13}$$

where L_{total} is the measured inductance of the 2-turn 4-layer miniature 3-D inductor, M is the mutual inductance, and the extracted coupling factor K is 0.3.

B. Comparisons of the Planar, Stacked, and Miniature 3-D Inductors

Fig. 12(a) shows one planar inductor and one miniature 3-D inductor. The sizes of the planar inductor and miniature 3-D inductor are $220\ \mu\text{m} \times 220\ \mu\text{m}$ and $80\ \mu\text{m} \times 80\ \mu\text{m}$, respectively. In this example, the miniature 3-D inductor uses only 16% of the area to achieve the same inductance as the planar inductor, and the higher $Q_{\max}$ compares to the planar inductor, as shown in Fig. 12(b). The planar inductor can use the narrower metal line to achieve the same inductance with the smaller die area, and its $Q_{\max}$ will occur at a higher frequency. However, using the narrower metal line may decrease the Q and even $Q_{\max}$ due to the larger resistive loss. In most applications, Q significantly determines the performances of the circuits, and therefore it is not acceptable to minimize the occupied area with Q degradation.

In order to compare the self-resonance frequency of the stacked and the miniature 3-D inductors, a 2-turn 4-layer stacked inductor has also been fabricated in the same process with 40-μm inner diameter, 10-μm metal width, and 1-μm

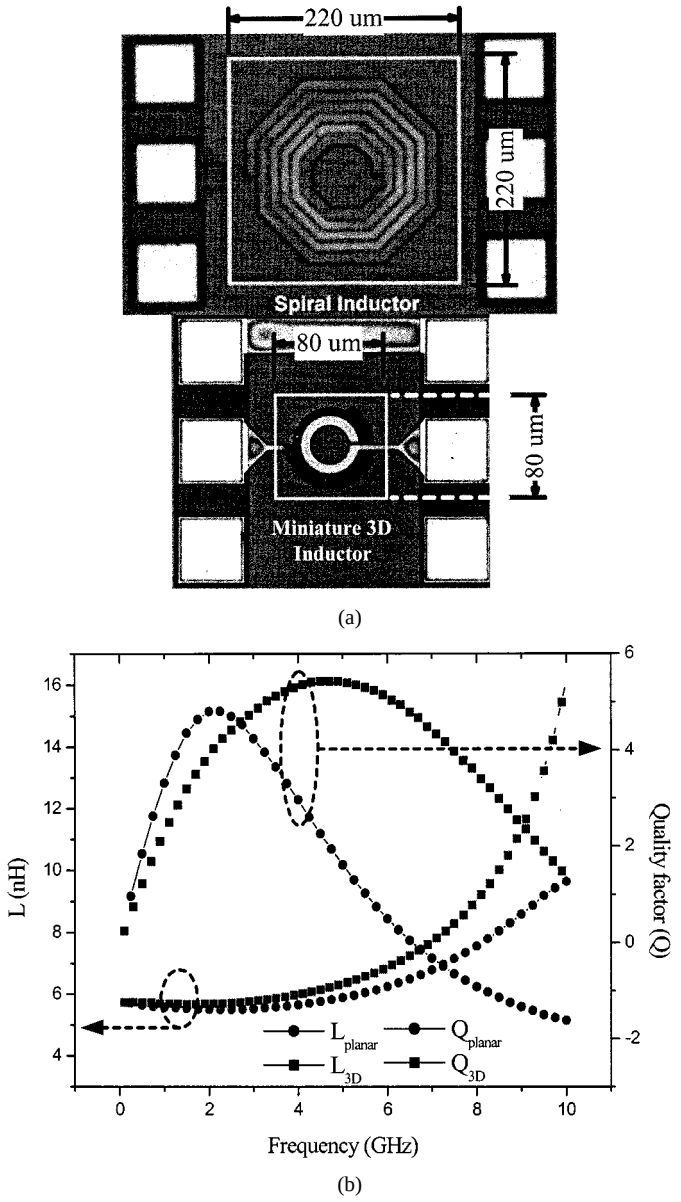


Fig. 12. (a) Die photo of the planar inductor and a miniature 3-D inductor. (b) Measured inductances and quality factors of the planar and the miniature 3-D inductors.

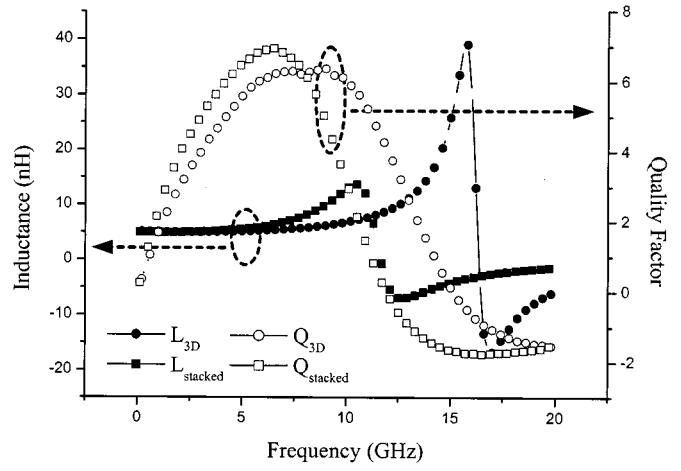


Fig. 13. Measured inductances and quality factors of the stacked and the miniature 3-D inductors.

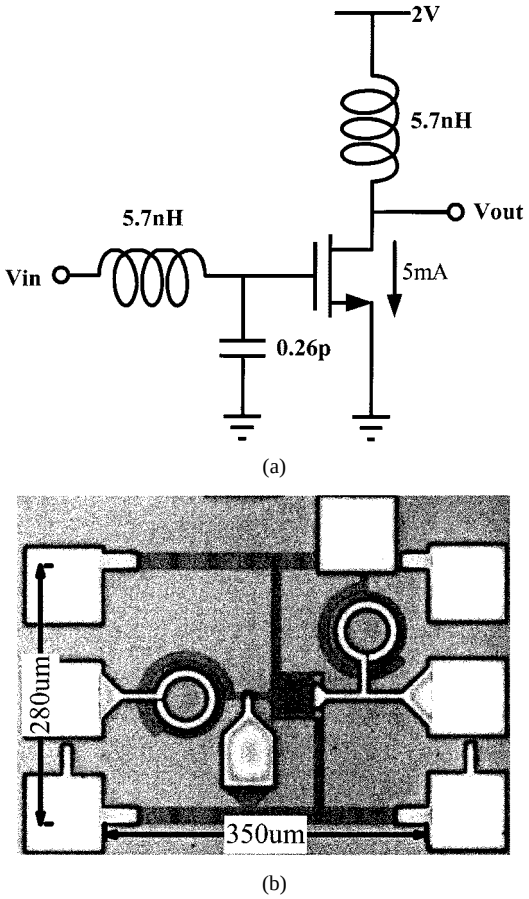


Fig. 14. (a) Schematic and (b) die photo of a 2.4-GHz CMOS LNA.

spacing. Fig. 13 displays the inductance and quality factor of the stacked and miniature 3-D inductors with the same area. The miniature 3-D inductor increases self-resonance frequency by 34%, from 11.8 to 15.8 GHz, with only 8% degradation of the quality factor. The measured equivalent capacitances of the miniature 3-D inductor and the stacked inductor are 24.4 and 36.5 fF, respectively. If we extend (10)–(11) to n-turn 4-layer, then the predicted equivalent capacitances, which are 25.2 and 36.8 fF, respectively, are very close to the measured ones. That means our derived equations can be used to quickly and accurately estimate the f_{SR} of the multilayer multiturn inductor.

Compared to the planar inductor, the miniature 3-D inductor has the advantages of not only small area but also better quality factor. The stacked inductor also can use a smaller area to achieve the required inductance, but it suffers from low self-resonance frequency. Although a modified version of the stacked inductor has been proposed in [17], it needs more metal layers to move the spirals away from each other in order to increase f_{SR}. The miniature 3-D inductor is a new proposed structure to improve the self-resonance frequency without enlarging the area and requiring additional metal layers.

C. Application

On-chip inductors are often used in RF circuits, such as the LNA. The schematic of a single-stage fully monolithic CMOS 2.4-GHz LNA and its die photo are shown in Fig. 14(a) and (b),

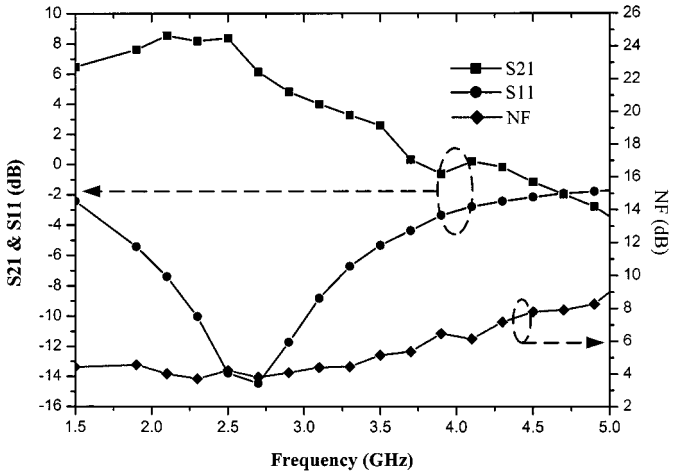


Fig. 15. Measured performances of 2.4-GHz CMOS LNA.

respectively. This LNA utilizes two miniature 3-D inductors, one used in the input matching network and the other being the loading. The measured $S11$ is -14 dB, $S21$ is 8 dB, and NF is 3.7 dB at 2.4 GHz with 10 mW power consumption, as shown in Fig. 15. The area of the CMOS LNA is only 350 μm $\times$ 280 μm and is almost equal to the area of one planar spiral inductor. This experimental result verified the functions and also emphasized the small area of the miniature 3-D inductor.

V. Conclusion

In this paper, a miniature 3-D inductor structure is proposed and several test keys have been fabricated in a 0.35-μm standard 1P4M CMOS technology. The miniature 3-D inductor saves about 80% area, which is required by the conventional planar spiral inductor with the same inductance. We derive analytical equations to estimate the $f_{\rm SR}$ of the miniature 3-D inductor and the stacked inductor and also propose capacitance distribution models to prove that the miniature 3-D inductor has a higher self-resonance frequency than the stacked inductor.

Owing to the advantages of the small area and high self-resonance frequency, the proposed miniature 3-D inductor is very suitable for RF applications. Moreover, the miniature 3-D inductor is fabricated in the standard CMOS process; thus it will not require any process modifications resulting in additional cost. Finally, the proposed structure is not only for CMOS technology but also can be applied to SiGe or Bipolar process.

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