A 1.57-GHz RF Front-End for Triple Conversion GPS Receiver

Francesco Piazza and Qiuting Huang, *Senior Member, IEEE*

***Abstract*— A low-power, 1.57-GHz RF front-end for a global positioning system (GPS) receiver has been designed in a 1.0-μm BiCMOS technology. It consists of a low noise amplifier with 15 dB of gain, a single balanced mixer with 6.3 mS of conversion g_m, a Colpitts *LC* local oscillator, and an emitter coupled logic (ECL) divide-by-eight prescaler. This front-end has a singal sideband (SSB) noise figure of 8.1 dB and is part of a triple conversion superheterodyne receiver whose IF frequencies are 179, 4.7, and 1.05 MHz. Low power consumption has been achieved, with 10.5 mA at 3-V supply voltage for the front-end, while the complete receiver is expected to draw about 12 mA.**

***Index Terms*— CDMA, frequency synthesis, GPS, low noise amplifier, low power, mixer, MMIC, receiver, RF front end.**

I. Introduction

THE fast growing wireless communications market has created urgent demands for low-power, low-cost solutions to implement both the digital processing and the RF analog parts of communications receivers. Until a few years ago, RF design was dominated by discrete circuits or low integration level monolithic microwave integrated circuits (MMIC's) in the low GHz range, where most communication services, including the global positioning system (GPS), are allocated. The general trend toward miniaturization and low cost makes integrated solutions with low external part count highly desirable, and today complete GPS receivers on a single silicon chip have become commonplace [1]. These single-chip receivers, although performing very well, are usually targeted toward relatively big handheld or fixed (e.g., on a car or ship) applications, where the power consumption or the number and size of external components is less a problem. If GPS receivers can be made much less power hungry and much smaller than those on the market today, however, many applications outside navigation and surveying, such as those of the consumer market, can be envisaged. The latter include receivers that are small enough to be carried in the pocket or worn on the wrist, for better convenience. In this paper we present a GPS chip targeted toward these applications. The paper is organized as follows. Section II provides a general description of the GPS system, which contains background technical information that has impact on our receiver planning. The planned receiver architecture is presented next (Section III), before front-end specifications and design are described (Section IV). Sections V–VII discuss achieved power consumption, issues in layout, and measurements respectively.

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The authors are with the Integrated Systems Laboratory, Swiss Federal Institute of Technology (ETH), CH-8092 Zurich, Switzerland.

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II. The GPS System

The GPS is based on 24 satellites located in six orbital planes at a height of 20 200 km and circle the Earth every 12 h. Each plane is inclined at 55° to the Earth's equator and contains four satellites. The GPS positioning is based on one-way time-of-arrival ranging. Each satellite sends the universial time (UTC) and navigation data using a spread spectrum code division multiple access (CDMA) technique. A receiver can calculate its own position and speed by correlating the signal delays from any four satellites and combining the result with orbit-correction data sent by the satellites. Two services are provided by GPS: a precise positioning service (P-code) whose use is restricted to military and a standard positioning service (coarse acquisition, C/A-code), less precise than the P-code but available to everyone.

All 24 satellites send on the same two frequencies: L1 is the primary frequency and carries the C/A-code, and L2 is the secondary frequency and carries the P-code. The two frequencies are derived from a 10.23-MHz atomic frequency standard. The frequency of L1 is 1575.42 MHz (154 times the atomic clock) and that of L2 is 1227.6 MHz (120 times the atomic clock). Interference between signals of different satellites is avoided using pseudorandom signals with low cross-correlation for the CDMA modulation. The C/A-code uses 1023 chips Gold codes [2], [3].

The integrated circuit reported in this work is a low-power RF front-end for a GPS receiver for the 1575.42 MHz civilian L1 band. The immediate application of such an integrated receiver is to provide GPS time reference—GPS positioning will be used to set the correct time zone—for small, portable (wearable) consumer products. Low power consumption is therefore a primary requirement, and the specified power source is a small lithium battery (2.4–3.5 V). The number and size of external components are also important requirements, not only due to cost, but also the space available. Both requirements must already be addressed during system planning.

III. Receiver Architecture

To reduce power consumption, the most obvious thing to do is to reduce the number of components working at the highest frequency, while the high gain IF amplifiers must work at the lowest practical frequency. On the other hand, filter size and selectivity requirements prevent the intermediate frequency

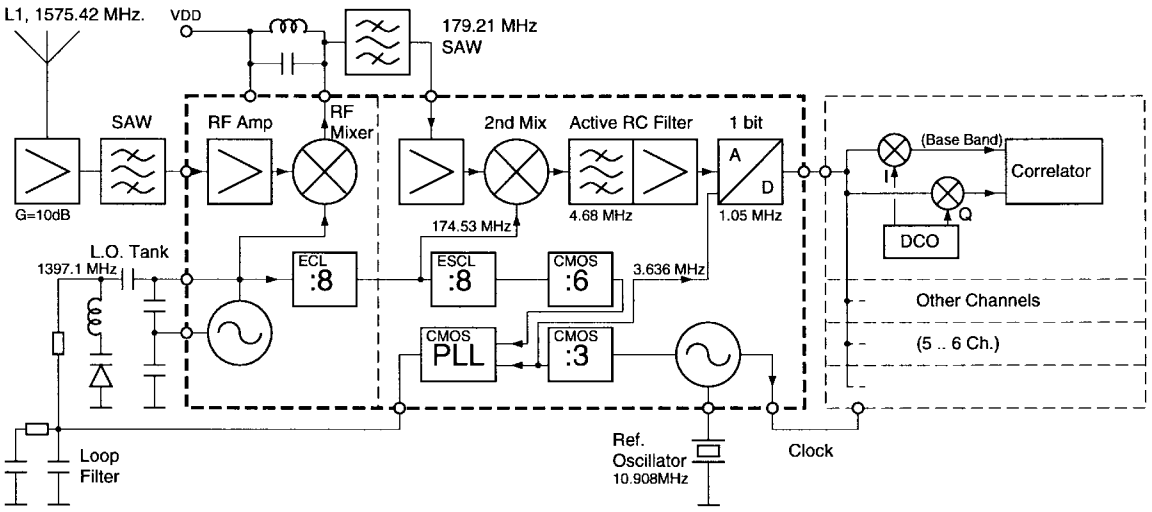

Fig. 1. Block diagram of the complete GPS receiver.

from being too low. Surface acoustic wave (SAW) filters for frequencies lower than roughly 100–150 MHz are typically too big and incompatible with our application. As a tradeoff between these requirements, a triple conversion architecture has therefore been chosen. A block diagram of this receiver, including the most important external components, is shown in Fig. 1.

The 1.57-GHz GPS L1 signal is received by an active patch antenna and filtered with a SAW filter to remove signals at the image frequency and other strong out-of-band signals which may overload the front-end. This signal is then amplified by about 15 dB and mixed down to first IF with a single balanced mixer. The first IF signal is then routed to an off-chip 179-MHz SAW filter where channel filtering takes place. The performance of this filter is critical to system performance, due to the rather low second IF chosen. A relatively high-frequency channel filter has been chosen because of its small size. The wide 1.8-MHz passband makes this possible, without having to use highly selective filters. The filtered signal is then amplified by 12 dB and down-converted to the 4.7 MHz second IF with a double balanced mixer. Since channel filtering occurs at first IF, the second IF filter need only remove the higher frequency mixing products and the local oscillator feedthrough of the first mixer, both being well above 4.7 MHz. The required performance is therefore quite moderate, allowing the filter to be fully integrated on chip. The main benefit of integrating the second IF filter is the reduction of the receiver complexity to a level comparable to that of a single superheterodyne receiver. A fifth-order Butterworth active RC filter has been chosen. After 68 dB of gain, the second IF signal is amplitude limited and converted to digital with a 1-b AD converter. Using a 1-b converter results in slightly degraded performance compared to that of a multibit converter, but it allows the design of a simpler, lower power receiver without automatic gain control. Sampling at 3.6 MHz, the AD converter also down-converts the second IF signal to the third IF of 1.05 MHz. Signal detection is then performed digitally on a second chip that contains all the digital processing and controlling parts of the receiver. Since GPS uses CDMA, the receiver needs only to receive one channel. This means only a single frequency has to be generated by the local oscillator. The frequency synthesizer is therefore a very simple design, and fixed dividers with simple division ratios can be used, resulting in a further reduction in power consumption.

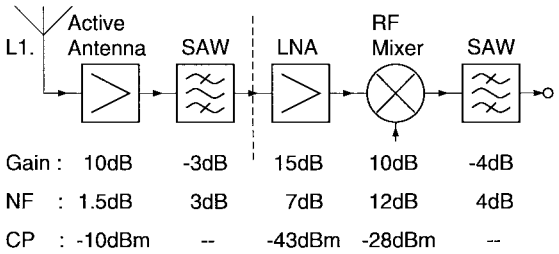

Fig. 2. GPS receiver specifications.

Although a single-chip implementation is envisaged, due to time constraints, the receiver has been split into two blocks. The first is the 1.57-GHz RF front-end to the left of the dashed line in Fig. 1. It consists of a low noise amplifier (LNA), a single balanced mixer, an *LC*-oscillator and an emitter coupled logic (ECL) divide-by-eight prescaler, and has been integrated in a 1-μm BiCMOS technology, whose NPN bipolar transistors have an $f_t = 13$ GHz. The IF and baseband components form the second chip, which has been designed in the same BiCMOS technology [4]. The two chips will be merged later into a single-chip receiver and will be reported separately.

IV. The Front End

The choice of gain for the various blocks of a receiver is always a tradeoff, especially at the front end. The main parameters that have to be taken into consideration are intermodulation (IP3), noise figure (NF), and power consumption. Setting high gain to the active antenna and LNA will help reduce the noise figure by minimizing noise contribution of the mixer, but at the expense of higher power consumption in these blocks and risk of early mixer overloading. Lower LNA gain may improve linearity and power consumption, but a very low noise mixer would be required to maintain an acceptable noise figure. Such a mixer will very likely consume much power and require a large local oscillator amplitude. In other

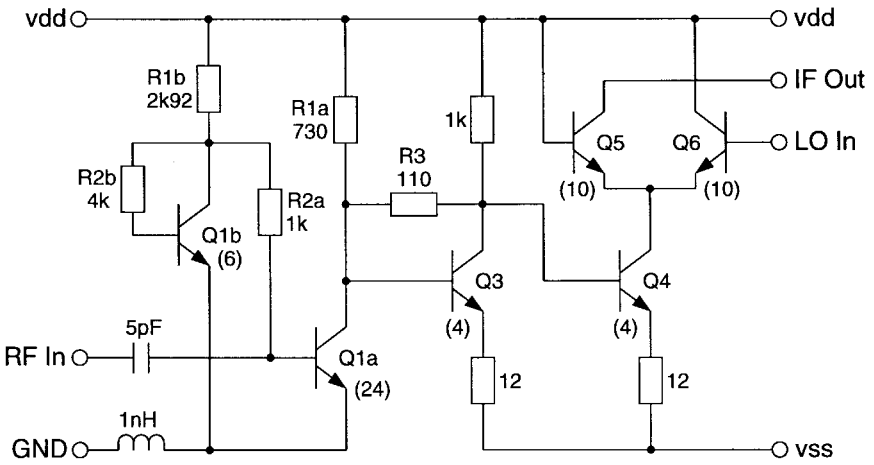

Fig. 3. Schematic diagram of the LNA-mixer combination.

words, low gain LNA combined with a low noise mixer may not offer a significant advantage in total power consumption over high gain LNA combined with a mixer with higher NF.

For the GPS signal itself, front-end nonlinearity is not much of a problem. The received signal level is in fact very low and relatively constant, consisting mainly of thermal (cosmic) noise. The linearity specification is dictated by the required system performance in the presence of external interfering signals. The very small patch antenna required by wearable applications has necessarily low gain. This tends to relax the linearity requirement somewhat, but imposes a low noise figure for the receiver. A front end with relatively high gain has therefore been chosen. Fig. 2 shows the resulting receiver specifications with gains, NF, and −1 dB compression points (CP) given below each block. The total single sideband (SSB) noise figure, referred to the input of the on-chip LNA, is 7.43 dB. At the receiver input it is 3.81 dB, which is adequate considering the application of this receiver. The first RF amplifier block (active antenna) is not on-chip. It will be constructed using a discrete transistor and a few passive components and will not be discussed further in this paper.

A. Low Noise Amplifier

In this application, the gain of the LNA was specified as 15 dB, while the requirements for both the noise figure and 1-dB compression point were quite moderate, 7 and −43 dBm, respectively. Gain independence from temperature, process tolerances or V_{DD} variation is desirable, as is 50-Ω input impedance, to avoid external matching networks.

To obtain a gain of 15 dB at 1.57 GHz, a two-stage amplifier is needed. The schematic diagram is shown in Fig. 3. It is a transconductance amplifier driving a transimpedance load, similar to [6]. The main difference is the much higher current levels required by this design, dictated by the higher operating frequency. This requires a different strategy for transistor sizing to minimize NF. The noise here is dominated by r_B, while shot noise is negligible due to the high input transconductance implemented by transistor Q_{1a}. A large transistor, 24 times the minimum emitter, has been used to reduce r_B, and thus thermal noise. The replica circuit (Q_{1b}, R_{1b}, and R_{2b}) is used to set the collector current of Q_{1a} to 3 mA, which is sufficient to achieve the required bandwidth. The input impedance of the amplifier at high frequency is mainly defined by r_B and the reactance of C_π and C_μ. A small, partially capacitive impedance around 12 Ω is therefore expected. Matching this impedance to 50 Ω could be easily obtained with an external low Q LC-network, but such external components are undesirable in our application and should be replaced with on-chip components whenever possible. A common technique to obtain approximate matching is to add a small inductance at the emitter of Q_{1a}, which will set the input impedance of the amplifier to approximately $2\pi f_T L_e$. The required value is about 1 nH, which can be realized using bonding wires. Since this value is quite small, the emitter connection of Q_{1a} has been brought out on two separate pads, such that the emitter inductor may be realized as two bonding wires in parallel, effectively halving the total inductance. In our test circuit, however, the best results were obtained with a single, short, bonding wire. Wide bandwidth and low sensitivity to manufacturing tolerances may be obtained if the Q of the matching network is low. In this case, the Q is about 1.3, thus ensuring good matching over a wide bandwidth that includes the image frequency. Had there been a mismatch at the image frequency, the noise figure of the front end would have been degraded, because no image filter is used before the mixer. Using this technique, matching to 50 Ω is achieved with no external component, and a very satisfactory S_{11} of −10.6 dB has been achieved, as shown in Fig. 4. The first LNA stage, with its bonding wire matching network, has a voltage gain of 12 dB.

The transimpedance stage is formed by Q_3 and R_3 and is dc coupled to the first stage. Using dc coupling between stages helps minimize the parasitic capacitances on sensitive nodes and allows a flat frequency response (without peaking) to be achieved. In order to save chip area, external components, and the power required to go off-chip and drive a 50-Ω load, the image-reject filter has been omitted. The output of the LNA has been connected directly to the mixer at the expense of an increased noise figure due to the LNA noise at the image frequency of the mixer. As explained later, the use of an image reject filter could improve the noise figure by about 1.4 dB.

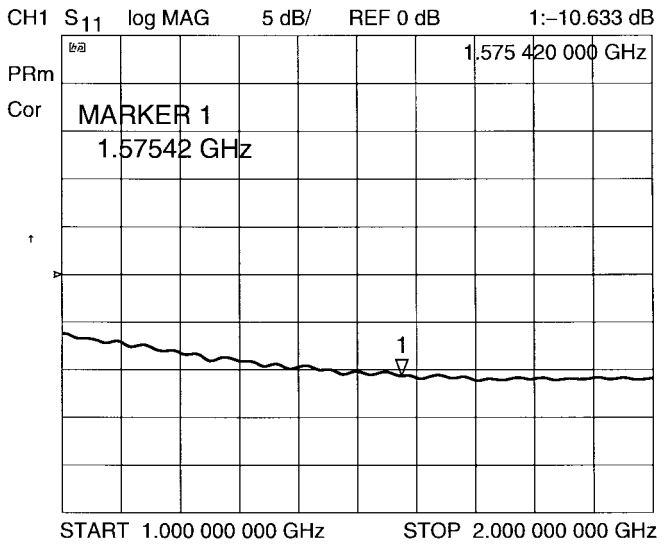

Fig. 4. Measured S_{11} of the LNA-mixer combination.

To reduce power consumption further, a small transistor (four emitters) with low parasitic capacitances has been used as Q_3. To obtain the required gain and bandwidth, a collector current of only 2 mA was required. At this current, the voltage gain for the second stage is 4.7 dB, yielding a total LNA gain of 16.7 dB. Linearity performance is decreased at low current, but the moderate requirement of our receiver is easily fulfilled at 2 mA. Having a high r_B, transistor Q_3 is the main noise source of the second stage, but its contribution to LNA noise is low because it is scaled by the gain of the first stage. In fact, the noise of the second stage is only about 30% of the total. Q_3 also generates the bias voltage for the mixer.

Since the g_m of a bipolar transistor is inversely proportional to the absolute temperature, temperature compensation of the LNA gain requires that its bias current have a proportional to absolute temperature (PTAT) characteristic. In this prototype, no temperature compensation has been implemented, but this can be easily obtained by regulating the LNA supply voltage as shown in Fig. 5.

Due to the internal connection to the mixer, no measurement can be performed on the LNA alone, thus performance has been estimated with calculations and SPICE simulations only. The voltage gain of the LNA, including its impedance matching network, is 16.7 dB at 1.57 GHz, while its noise figure is about 2.5 dB. The voltage gain of the complete front end is 26.7 dB. The 1 dB CP of the LNA alone is dominated by the second stage and is calculated to be -22.7 dBm, which is much better than the specification. The overall front end 1 dB CP, however, will be dominated by the mixer. Measurements on the whole front end, as shown later, confirm these estimates.

B. Single Balanced Mixer

In order to minimize power consumption, a single balanced RF mixer has been chosen. The conversion g_m of a single balanced mixer is roughly twice that of a double balanced mixer for the same bias current, but is less linear and has a high local oscillator feedthrough to the IF port. This mixer, also shown in Fig. 3, consists of Q_4, a 12-Ω emitter degeneration

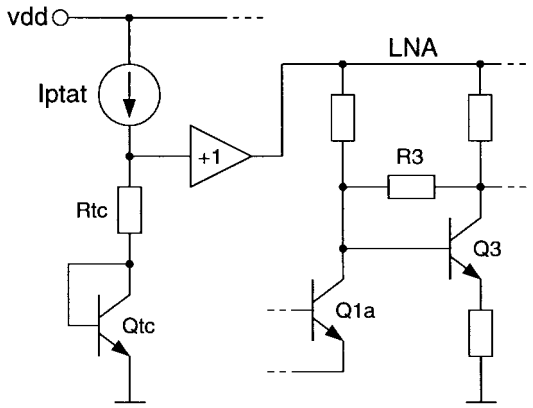

Fig. 5. Temperature compensation of LNA gain.

resistor and the chopping differential pair Q_5 and Q_6. The IF output is high impedance open collector, which will be connected to the external SAW filter via an RCL matching network. The nominal source and load impedances for the SAW filter are specified as 500 Ω. Assuming ideal switching, the conversion g_m of a single balanced mixer is

$$g_{mc} = \frac{1}{\pi}\, g_{m(Q4)}.$$

Assuming a 250-Ω total load (500 Ω for the SAW filter, in parallel with its 500-Ω matching resistor), a g_m of 12.6 mS is required to obtain a gain of 10 dB. Taking into consideration the effect of the emitter degeneration resistor, a bias current of 2 mA is required for Q_4. The emitter degeneration resistor was added to improve both linearity and dc bias stability, with only a slight degradation of noise figure. The latter is in fact dominated by the noise generated by the switching differential pair. The large local oscillator feedthrough typical of single balanced mixers is of no consequence in this application, since the oscillator signal is removed by the external IF filter.

DC biasing of the mixer is provided by the LNA second stage, Q_3, with which Q_4 forms a current mirror. By biasing the LNA as in Fig. 5, the bias current of Q_4 will have a PTAT characteristic. This means that temperature compensation of the mixer g_m is also obtained. DC bias of the local oscillator (LO) port is provided by a 5-kΩ resistor to $V_{\rm dd}$. The resistor is also part of the local oscillator.

The performance of this mixer, as in the case of the LNA, can only be estimated, since the internal connection to the LNA prevents any direct measurement. The noise figure of a mixer is quite difficult to predict, because it depends on the precise switching behavior of Q_5 and Q_6. When one of the two transistors is completely cut off, the mixer looks like a cascode amplifier, thus the noise is mostly contributed by Q_4. Around the zero-crossing of the LO signal, however, both Q_5 and Q_6 conduct, during which time they form a differential amplifier that contributes its own amplified noise to the total noise of the mixer. Experience has shown that the double sideband (DSB) noise figure of a mixer of this type is around 16–18 dB, with a moderate LO drive around 0 dBm. Given the DSB noise figure of the mixer, and considering the 3-dB loss due to the unfiltered noise at the image frequency for the LNA, the noise

figure of the whole front end can be calculated with

$$F_{\text{tot}} = 2F_{\text{lna}} + 2\frac{F_{\text{mix}} - 1}{G_{\text{lna}}}.$$

Assuming $F = 2.5$ dB for the LNA, an SSB noise figure between 7.1 and 7.9 dB will then result. The measured value was 8.1 dB, which corroborates the estimate. The 1 dB compression point of the front end will be dominated by that of the mixer, which is around 5 dB below the compression point of the LNA. A value of -28 dBm has been measured at the input of the front end, which corresponds to -11.4 dBm at the mixer input.

If the relative contribution of the mixer noise is small, the noise figure of the front-end can be improved by using an image filter between LNA and mixer, at the expense of extra external components and higher power consumption. If the relative mixer noise contribution is high, as is often the case, the noise figure improvement by image-reject filter is very inefficient. Assuming an ideal filter that is lossless at the desired frequency and rejects the noise of the LNA at the image frequency completely, the total SSB noise figure of the front end can be calculated with

$$F_{\text{tot}} = F_{\text{lna}} + 2\frac{F_{\text{mix}} - 1}{G_{\text{lna}}}.$$

For the same noise figures of 18 and 2.5 dB for mixer and LNA, respectively, a noise figure of 6.5 dB can be calculated, which corresponds to a 1.4 dB improvement over the case without filter. This is lower than the 3 dB one might have expected, because the image filter, in fact, cannot suppress the noise at the image frequency generated by the mixer itself. A real filter will result in an even smaller improvement, due to insertion losses and imperfect image rejection. A suitable image-reject filter is a high-Q *LC* or a SAW filter. If a second-order *LC* bandpass with, e.g., a Q of ten is used, it will reject the 1.217 GHz image frequency by only 15 dB. Despite the relatively moderate performance, such a filter cannot be easily integrated, because it will require high Q inductors, which will be difficult to implement using on-chip inductors or bonding wires. More importantly, since the latter's values cannot be readily adjusted, tolerances in the resonant frequency will incur unacceptable loss of gain. An off-chip SAW filter, on the other hand, typically has a high insertion loss, although its center frequency is better defined. Both approaches partially defeat the purpose of the LNA. For these reasons, no filter has been used in this design.

C. LC Local Oscillator

In our application, the local oscillator must provide a 1.4-GHz signal to the mixer, with an amplitude of about -3 dBm, or 450 mV_{pp}, for best performance. With GPS being a spread spectrum system, phase noise is not a critical parameter, and even a value around -80–85 dBc/Hz at 100 kHz offset is still acceptable.

From the point of view of only phase noise, many oscillator architectures such as fully integrated ring or relaxation oscillators, or *LC* oscillators with integrated low-Q inductor, fulfill these specifications. Integrated oscillators, however, tend to consume much more power—a critical parameter in our application—than those based on an external high-Q resonator. The local oscillator chosen for our application is therefore the varactor-tuned Colpitts oscillator with external *LC* tank, whose schematic diagram appears in Fig. 6. Transistor Q_1 forms the active part of the oscillator, while Q_2 to Q_4 form a 10:1 biasing current mirror.

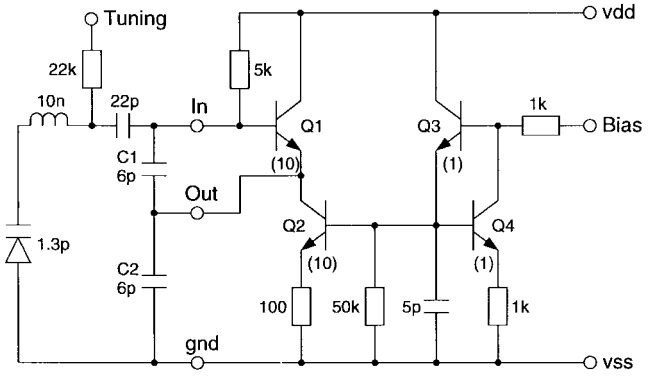

Fig. 6. Schematic diagram of the local oscillator.

The bias current is a function of the required signal amplitude and the Q of the external resonator and can be calculated from the formula [5]

$$V_p = 1.9\left(1 - \frac{1}{n}\right)R_L I_b$$

where V_p is the peak voltage at Q_1 base, n is the voltage divider ratio $(C_1 + C_2)/C_2$, and R_L is the total parallel resistive loss of the *LC* tank. To estimate the Q of the tank, a few low-cost 10-nH inductors have been measured, showing a Q around 30–50 at 1.4 GHz. The corresponding series resistance is therefore 1.8 to 2.9 Ω. To account for the losses in the capacitors, connections, and bonding pads, a total series resistance of 4 Ω has been assumed. Based on this estimate and knowing that $n = 2$ in this circuit, we can derive that $I_b = 900$ μA is required for -3 dBm amplitude. This current is less than 9% of the total current consumption of the front end.

The oscillator is connected to the rest of the circuit directly, without using any buffer, again in order to save power. The mixer LO port is connected to the base of Q_1, while the divide-by-eight prescaler is ac coupled to its emitter. Usually, a buffer with high reverse isolation is required at the input of the prescaler to prevent the latter from injecting the switching transients at submultiples of the oscillator's frequency back to the oscillator, thus degrading its performance. In our design, a symmetrical layout, as explained later, has been used to reduce these transients, thereby enabling the unbuffered connection. During the measurements, no spurious signals originating from the prescaler has been noticed, while oscillator performance was not affected substantially by switching the prescaler on and off.

D. Divide-by-Eight Prescaler

Since in a GPS receiver only one local oscillator frequency has to be synthesized, fixed dividers with simple division ratios can be used. In order to save power, for the first divider, a

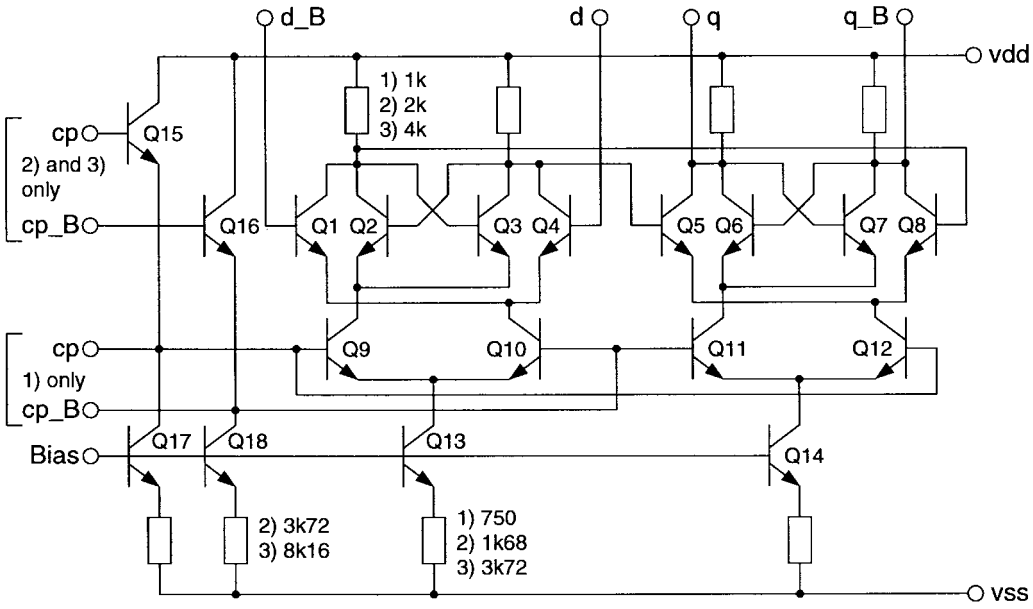

Fig. 7. Schematic diagram of the ECL prescaler.

divide-by-eight prescaler has been chosen which consists of a cascade of three ECL flip-flops. A schematic diagram of these flip-flops is shown in Fig. 7. A signal amplitude of 200 mV_{PP} has been chosen as a compromise between noise immunity, speed, and signal coupling into the substrate. The first flip-flop is biased with 400 μA and is ac coupled to the oscillator's emitter with a 2-pF capacitor. Its bias voltage is established with a voltage divider such that no level shifters are needed, therefore the input buffers Q_{15} and Q_{16} have been omitted. Since the operating frequency of the second and third flip-flops are 1/2 and 1/4 of the input frequency, the bias current has been scaled down proportionally to 200 and 100 μA, respectively. These two flip-flops require input buffers (Q_{15} and Q_{16}) which are biased with 50 and 25 μA, respectively. This results in a current consumption of 850 μA for the whole prescaler. The output of the prescaler is then buffered with a differential pair and brought off-chip for measurements. This buffer consumes 400 μA and is only required for this prototype. In the final single-chip version of the receiver, the buffer is no longer required since the output of the prescaler stays on-chip and is connected directly to the rest of the frequency synthesizer.

E. Biasing

The local oscillator and the prescaler require a bias current source of 90 and 40 μA, respectively. These currents are generated by the ΔV_{BE} current source shown in Fig. 8. A ΔV_{BE} current source has been used here because of its PTAT temperature coefficient, which compensates that of the g_m of the bipolar transistors. The ΔV_{BE} core is formed by Q_1 (4×) and Q_2 (1×) and is cascoded by Q_3 and Q_4 for better precision. Transistors Q_5, Q_6, and related parts form a start-up circuit that inject some current into Q_4. This circuit is then shut down just before the output current reaches its nominal value.

V. Power Consumption

Due to its high operating frequency, the power consumption of the complete GPS receiver is dominated, as expected, by the front end. The nominal supply current of this front-end chip, including all the biasing circuitry and the output buffer for the prescaler, is only 10.3 mA at 3 V, resulting in a power consumption of 30.9 mW. The remainder of the receiver is expected to draw approximately 1.7 mA, resulting in an estimated power consumption for the complete receiver chip of about 36 mW, which is sufficiently low for our application and which compares very well to existing solutions to date. While having a performance similar to our chip, the typical consumption of existing commercial GPS chips is from 2.5 to 11 times higher [1].

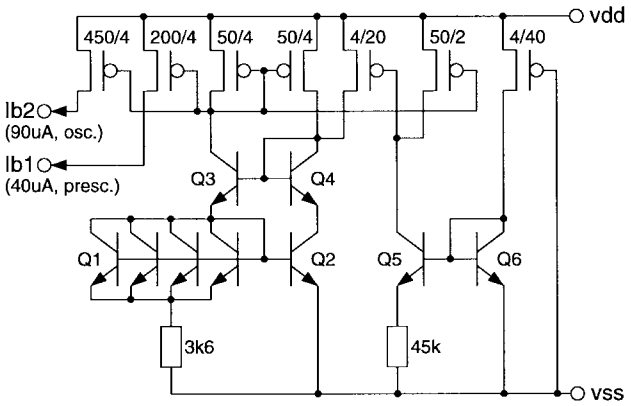

Fig. 8. Schematic diagram of the bias current source.

VI. Layout

A chip photomicrograph is shown in Fig. 9, the chip size is 1134 × 982 μm^2. In a chip working at 1.57 GHz, many layout issues may affect the performance, as, for example, component and pad placement, coupling through the substrate, and between parallel lines, etc.

During the placement of the various blocks, attention has been paid to parasitic coupling which could degrade performance or cause oscillation. The LNA and mixer are the block

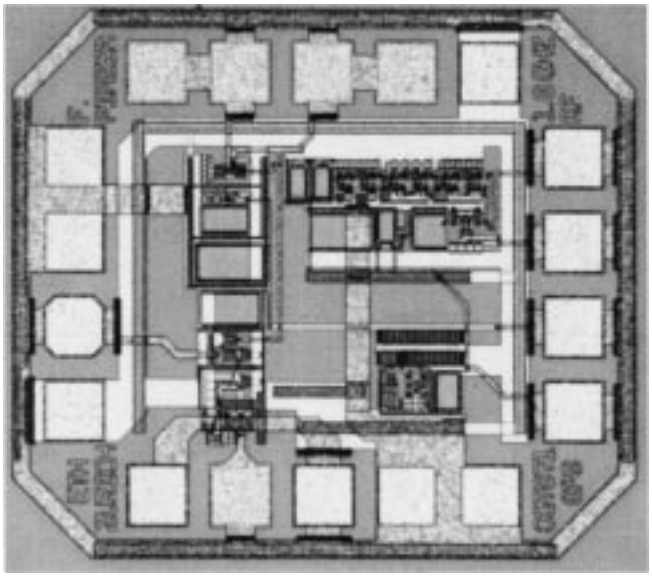

Fig. 9. Photomicrograph of the chip.

at the bottom left, the VCO is placed top left, while the pads of LNA and VCO are on opposite sides of the chip. All signal pads are placed between ground pads or pads at ac ground ($V_{\rm dd}$, bias). Large substrate contacts and guard rings separate all stages. Since the substrate is high ohmic, guard rings are an effective means to prevent parasitic coupling. More than 30 pF of on-chip decoupling capacitors has been placed between the supply lines to prevent coupling through them. The ECL prescaler has been placed top right, with the low-speed stages and the output buffer far right, to prevent interaction with the VCO. Particular attention is paid to layout symmetry, while the lines carrying true and complement have been routed in parallel. The bias circuit is located bottom right and has its own supply decoupling capacitor. Its outputs are connected to pads and decoupled externally to ground with low ESL ceramic surface mounted (SMD) capacitors.

Metal layers 1 and 2 have been used in most pads, while the pads carrying high frequency signals are metal2 only for lower capacitance against substrate. All pads have ESD protection diodes, 50 μm wide for the high frequency pads and 100 μm wide for the rest. The $V_{\rm dd}$ pads have an NPN clamp. A total of six pads are dedicated to ground, two for the LNA input and four on opposite sides for the rest. Double pads have been used for the VCO to maintain the stray inductance of the connections (bonding wires) as low as possible.

Thick metal2 or metal1–metal2 lines have been used for the ground connections, while metal1 has been used for the $V_{\rm dd}$. The RF connections are mainly metal2 and have been kept short wherever possible, routed away from other sensitive lines and partially shielded with metal1.

VII. Measurements

In this application, due to its stringent space constraints, hybrid construction technique using unpackaged chips will be used. For the measurements, a similar technique has been used. The naked chip has been directly bonded to a small printed circuit board (PCB), which contains all the necessary external components. The PCB, measuring 25.4 $\times$ 25.4 mm^2, has one signal plane and one ground plane on opposite sides and is mounted on a test fixture that holds PCB and connectors in place. Only SMD components have been used, while the VCO inductor has been constructed with a loop of copper wire. The supply voltage was set to its nominal value of 3 V.

TABLE I
GPS Front-End Characteristics

Process	1.0 μm BiCMOS
Front-end size	1134 μm x 982 μm
Front-end supply current	10.5 mA at 3 V
Front-end voltage gain	26.5 dB
-1dB compression point	-28 dBm
Noise figure (SSB)	8.1 dB
Mixer LO range	-15..+3 dBm
LO phase noise (100kHz)	-95.1 dBc/Hz
Prescaler self osc. freq.	1728 MHz

The measured voltage gain of the front-end is 26.5 dB, with the mixer output terminated on 250 Ω and driven by about -3 dBm of local oscillator amplitude. The acceptable local oscillator range is -15 dBm to $+3$ dBm. At the two extremes, the gain of the front end decreases by 1 dB. The S_{11} is -10.6 dB at 1575.42 MHz and -8.4 dB at the image frequency of 1217 MHz. The S_{11} is plotted in Fig. 4 from 1 to 2 GHz. The SSB noise figure is 8.1 dB, slightly higher than the specified 7.43 dB, while the input-referred 1 dB compression point is -28 dBm. No IP3 measurement has been performed, but a value of -18 dBm can be estimated from the compression point measurement.

Due to the lack of a direct output, the phase noise of the oscillator has been measured after mixing its signal down to IF with a clean 1.57 GHz signal using the internal mixer. A value of -95.1 dBc/Hz at 100 kHz offset has been measured. Since the local oscillator was not fast enough to measure the maximum operating frequency of the prescaler, the self-oscillating frequency with the oscillator stopped has been measured, in addition to the regular divide-by-eight operation at the local oscillator frequency. Self-oscillation with no input signal is a normal behavior of any ECL divider. In fact, with no input signal, all transistors from Q_2 to Q_8 (see Fig. 7) are biased and form, together with the stray capacitances, a relaxation oscillator. A value of 1728 MHz has been measured. The maximum operating frequency is expected to be about 10 to 20% higher.

The bias currents generated by the internal current source were 96.4 and 43 μA at 3 V, while the total current consumption of the chip was 10.5 mA at the same supply voltage.

Although no temperature and supply voltage independent biasing has been implemented in this prototype for the LNA and mixer, the chip is fully functional over the specified 2.4 to 3.6 V supply voltage range, but some gain variation must clearly be expected. The front-end gain varies between 22

and 29 dB for a 2.4 to 3.6 V supply voltage variation, while the total current consumption varies from 8.1 to 12.8 mA. Using the bias scheme shown in Fig. 5, the supply voltage dependence will be reduced to approximately that of the bias current source. For the latter, the bias currents were 94.5 and 42.2 μA at a supply voltage of 2.4 V, increasing to 98.2 and 43.8 μA for a supply voltage of 3.6 V.

A summary of the most important characteristics of this GPS front end is shown in Table I.

VIII. Conclusions

A low-power RF front end suitable for small portable GPS receivers has been demonstrated. Power consumption as low as 31.5 mW, combined with a minimal number of external components, has been achieved with nearly no compromise to performance. The front-end gain of 26.5 dB and the noise figure of 8.1 dB are comparable with most existing chips to date while consuming much less power.

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Francesco Piazza was born in Olivone, Switzerland, on January 5, 1962. He received the Dipl.Ing. degree in electrical engineering from the Swiss Federal Institute of Technology (ETH), Zurich, in 1992.

Since May 1992, he has been with the Integrated Systems Laboratory at the same university where he is working toward the Ph.D. degree in the area of RF and other high-speed integrated circuits.

Qiuting Huang (S'86–M'87–SM'96) graduated from the Department of Precision Instruments, Harbin Institute of Technology in 1982. He received the Ph.D. degree from Katholieke Universiteit Leuven, Departement Elektrotechniek, ESAT Laboratories, Heverlee, Belgium, in 1987.

Between 1987 and 1992, he was a Lecturer at the University of East Anglia, Norwich, UK. Since January 1993, he has been Assistant Professor at the Integrated Systems Laboratory, Swiss Federal Institute of Technology, Zurich. His general field of research is in analog and mixed analog-digital integrated circuits and systems. His current research projects include RF front-end for wireless communications, interface circuits to sensors and actuators, and low-noise, low-power IC's for biomedical applications.