5-GHz CMOS Radio Transceiver Front-End Chipset

Ting-Ping Liu, *Member, IEEE*, and Eric Westerwick, *Member, IEEE*

***Abstract*—Incorporating the direct-conversion architecture, a 5-GHz band radio transceiver front-end chipset for wireless LAN applications is implemented in a 0.25-μm CMOS technology. The 4-mm^2 5.25-GHz receiver IC contains a low noise amplifier with 2.5-dB noise figure (NF) and 16-dB power gain, a receive mixer with 12.0 dB single sideband NF, 13.7-dB voltage gain, and −5-dBm input 1-dB compression point. The 2.7-mm^2 transmitter IC achieves an output 1-dB compression of −2.5 dBm at 5.7 GHz with 33.4-dB (image) sideband rejection by using an integrated quadrature voltage-controlled oscillator. Operating from a 3-V supply, the power consumptions for the receiver and transmitter are 114 and 120 mW, respectively.**

***Index Terms*—transceiver front-end, low-noise amplifier, I/Q downconversion mixer, quadrature modulator, quadrature VCO, VCO buffer, driver amplifier, CMOS radio, wireless LAN transceiver.**

I. Introduction

WITH THE FCC's allocation of 300 MHz of bandwidth in the 5-GHz frequency band (5.15–5.35/5.725–5.825 GHz) for the unlicensed national information infrastructure (UNII), high data rate (up to 50 Mb/s) wireless local area networks (LAN) have become increasingly popular and important for mobile computing devices such as notebook computers. The European counterpart is the HIPERLAN (High Performance Radio LAN) system, which also operates in the 5-GHz band (5.15–5.35/5.47–5.725 GHz). In order to meet the potentially high demand for such wireless LAN products, low-cost silicon-based radio transceiver front-ends capable of performing at 5.15–5.825 GHz are essential. There have been a number of 5-GHz silicon transmit and receive ICs reported in the literature [1]–[4]. Most of them were implemented either in silicon BiCMOS or SiGe technology. Nevertheless, the transmit power level is limited to less than −10 dBm and the receiver single sideband (SSB) noise figure (NF) is above 5 dB.

This paper describes the design and implementation of a pair of 5-GHz CMOS radio transceiver front-end ICs for wireless LAN applications. This is the first CMOS transceiver chipset operating in the 5.2–5.7-GHz band ever reported in the literature. The 4-mm^2 5.25-GHz receiver IC contains a low-noise amplifier (LNA) with 2.5-dB NF and 16-dB power gain, a receive mixer with 11.95-dB SSB NF, 13.7-dB voltage gain, and −5-dBm input 1-dB compression point. The 2.7-mm^2 transmitter IC achieves an output 1-dB compression of −2.5 dBm at 5.7 GHz with 33.4-dB (image) sideband rejection by using an integrated quadrature voltage-controlled oscillator (VCO). Operating from a 3-V supply, the power consumptions for the receiver and transmitter are 114 and 120 mW, respectively.

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II. Transceiver Architecture

This prototype CMOS radio transceiver front-end chip set is intended for small low-cost wireless LAN mobile units. External RF band-select filters, a frequency synthesizer, and a power amplifier (PA) complete the radio front-end. The transceiver architecture is shown in Fig. 1. To achieve the highest level of integration and to reduce cost and power consumption, the transceiver incorporates the direct conversion (homodyne) architecture to eliminate the image reject filters needed between the LNA and mixer in the superheterodyne architecture. The differential circuit topology is employed throughout both the receiver and transmitter circuits to minimize the undesired coupling, especially the local oscillator (LO) leakage through the mixers to the antenna as it causes the dc offset to corrupt the desired low-frequency signal.

As shown in Fig. 1, the receiver IC integrates an LNA, a set of I/Q down-conversion mixers, an integrated quadrature VCO, and a pair of LO buffers. The quadrature VCO is based on the ring-coupled topology and the frequency tuning is performed without any external tank components by varying the currents of two transconductance stages [5]. The LNA is followed by a set of mixers, which are driven by quadrature LO signals LOI and LOQ at the output of the VCO buffers. The purpose of the VCO buffer is twofold: to improve the isolation (about 20 dB) between the mixers and quadrature VCO, therefore reducing frequency pulling of the VCO, and to provide large LO drives to optimize the mixer linearity and noise performance.

In the direct downconversion architecture, where the RF and LO frequencies are identical, the receiver IC generates the in-phase and quadrature baseband signals RI and RQ which can be readily processed by other CMOS-based low-frequency analog circuits, such as filters and amplifiers, before the analog–digital data converters. This is very attractive in terms of low cost and high integration. For testing purpose, the receive mixer differential output is converted to single-ended operation with external baluns. Similarly, baluns are used at other differential ports for measurements.

It is interesting to note that the receiver architecture in Fig. 1 can be configured as a superheterodyne image-reject receiver architecture by adding an IF 90° combiner at the output of the mixers to suppress the image signal before being further filtered and amplified by the following stages.

The transmitter IC is comprised of a quadrature modulator, a driver amplifier, and an on-chip quadrature VCO as well as buffers. Note that only one quadrature VCO is needed for the whole transceiver to drive both transmit and receive mixers. To

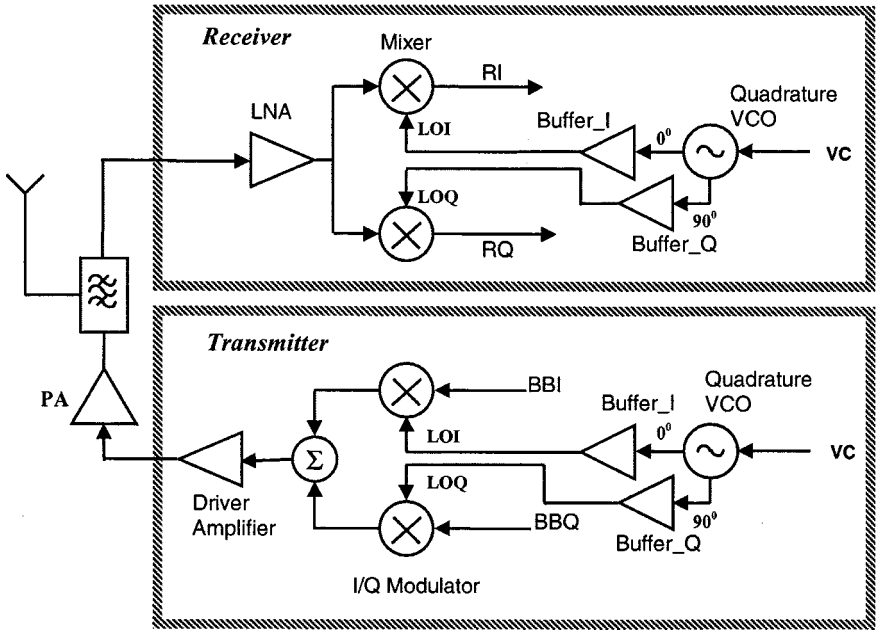


Fig. 1. Radio transceiver architecture.

facilitate testing, the VCO is included on the transmitter IC. The I/Q modulator takes large differential (up to 1.8 V, peak) baseband inputs BBI and BBQ, frequency up-converts with the quadrature LO signals, and sums the output current signals. On-chip inductors are used as loads at the I/Q modulator output to increase the headroom and voltage swing. Finally, the driver amplifier boosts the output power to a level capable of driving the external high-power transmit amplifier.

The inclusion of an on-chip VCO is especially important for the transmitter with the direct up-conversion architecture because it can minimize the radiation leakage from the strong PA output back to the core oscillator circuit and thus improve frequency purity. Using LO buffers between the VCO and modulator also helps isolate the sensitive VCO circuit from the high-power large voltage or current swing circuit blocks.

As with other transceiver architectures, accurate quadrature LO signals LOI and LOQ are important for the direct conversion architecture. Any amplitude mismatch or phase difference apart from 90° between LOI and LOQ causes degradation in signal-to-noise (S/N) ratio for the received signal, or spectrum regrowth for the GMSK-modulated transmit signal. The phase error is more troublesome than the amplitude imbalance and in general should be kept to no more than 5° [6].

III. Circuit Implementation

A. LNA

The simplified schematic of the LNA is shown in Fig. 2(a). It is a differential modified common-source amplifier. The on-chip gate and source inductors L1 and L2 are used to achieve 50 Ω impedance matching. A large input device M1 with 260-μm gate width is normally biased at 8 mA to attain noise and gain performance. Higher bias current would yield lower noise at the expense of higher power consumption. Cascode device M2 improves the amplifier reverse isolation (S12) and reduces the LO leakage from the mixer back to the LNA input, an important issue for the direct conversion receiver. Inductor L3 and capacitor C1 form the L-matching network for optimal power transfer

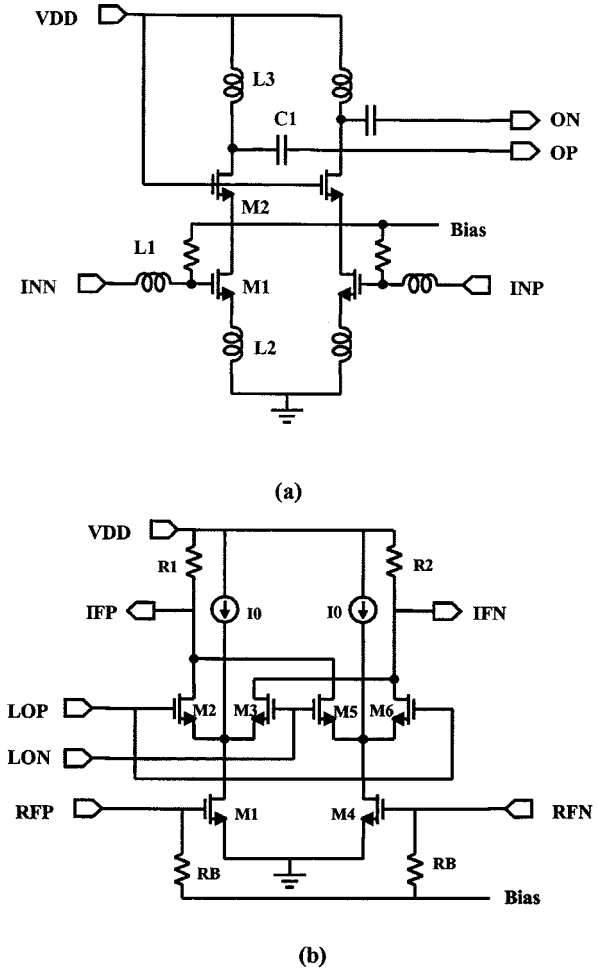


Fig. 2. (a) Simplified LNA schematic. (b) Simplified receive mixer schematic.

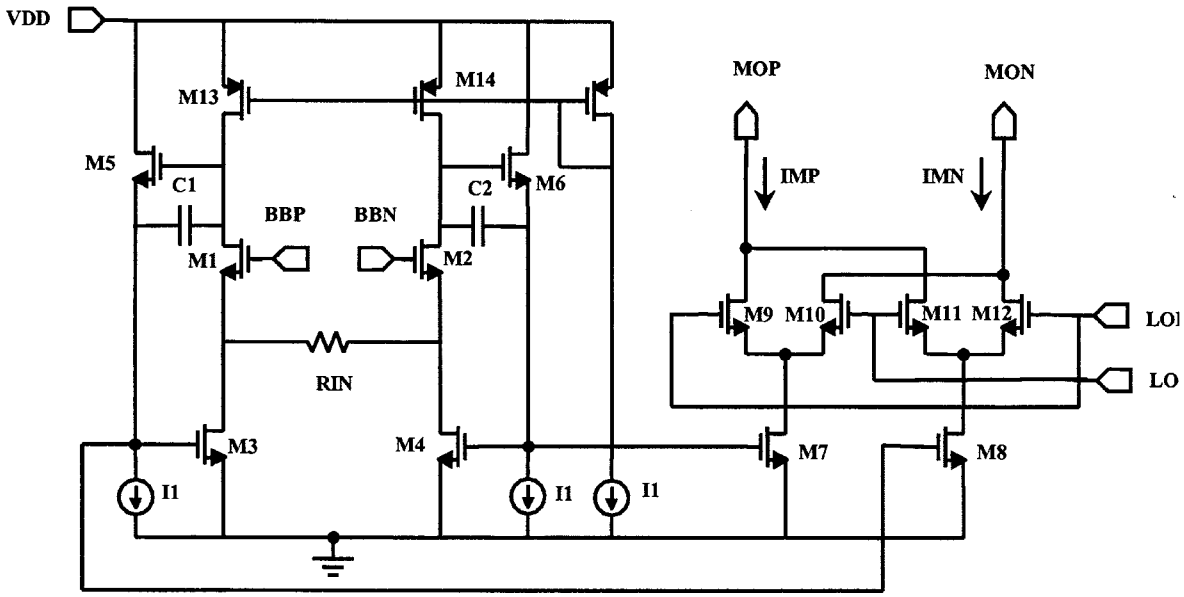


Fig. 3. Simplified modulator schematic.

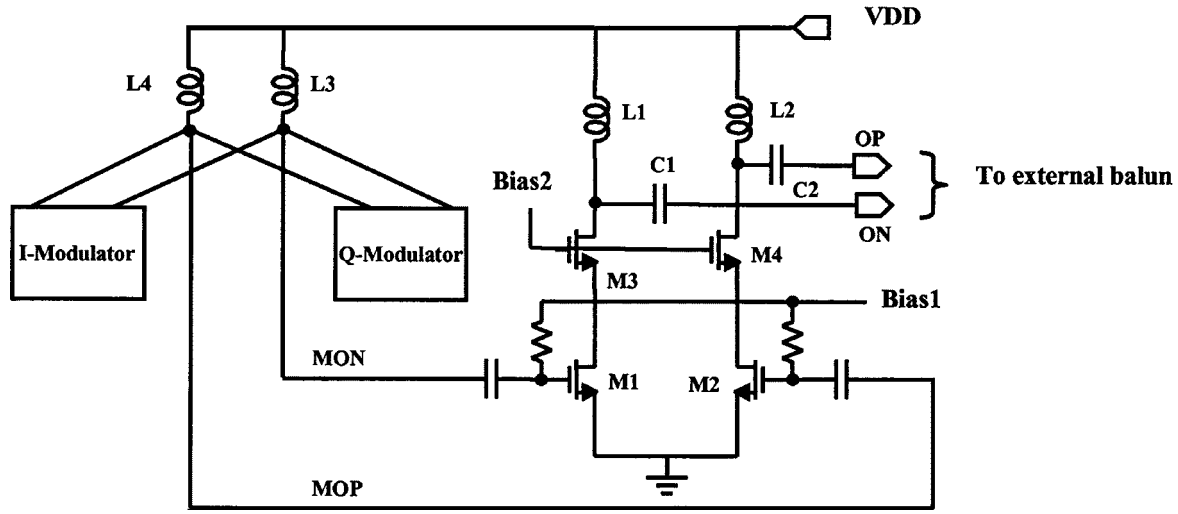


Fig. 4. Driver amplifier schematic.

to the following stage. Capacitor C1 also blocks the low-frequency second-order intermodulation products generated in the LNA which otherwise will be passed on to the mixers, another important issue for the direct conversion receiver.

B. Receiver Mixer

Fig. 2(b) is a simplified schematic of the receive mixer. It is a modified double-balanced Gilbert quad active mixer. Two constant current sources I0 are employed to reduce the required LO overdrive to completely switch the quad devices M2, M3, M5, and M6, and effectively increase the conversion gain. This also improves the voltage headroom for the quad switches. However, this is achieved at the cost of linearity degradation when I0 approaches the bias current of M1. Setting I0 to be three-quarters of the M1 bias current appears to be a good compromise. The LNA outputs OP and ON are coupled to the mixer input transistors M1 and M4, whose sources are directly connected to ground to produce lower third-order nonlinearity than if connected to a current source. Differential LO signals LOP and LON come from the on-chip VCO and buffers that also supply a dc bias voltage for the mixer. Differential IF outputs are available through two on-chip 500 Ω resistors R1–R2.

C. Modulator

The I/Q modulator is composed of two identical modulators driven by the quadrature LO signals. The modulator, as shown in Fig. 3, essentially converts the baseband differential voltage signals BBP–BBN to currents in the linear transconductance stage M1 through M6, and then frequency-up-converts the scaled current signals in transistors M7–M8 by the quad switches M9–M12 to produce output currents MOP and MON. The 5-kΩ resistor RIN sets the transconductance and 0.4-pF compensation capacitors C1–C2 allow flat voltage–current frequency response for the baseband signals up to 2 GHz. As in

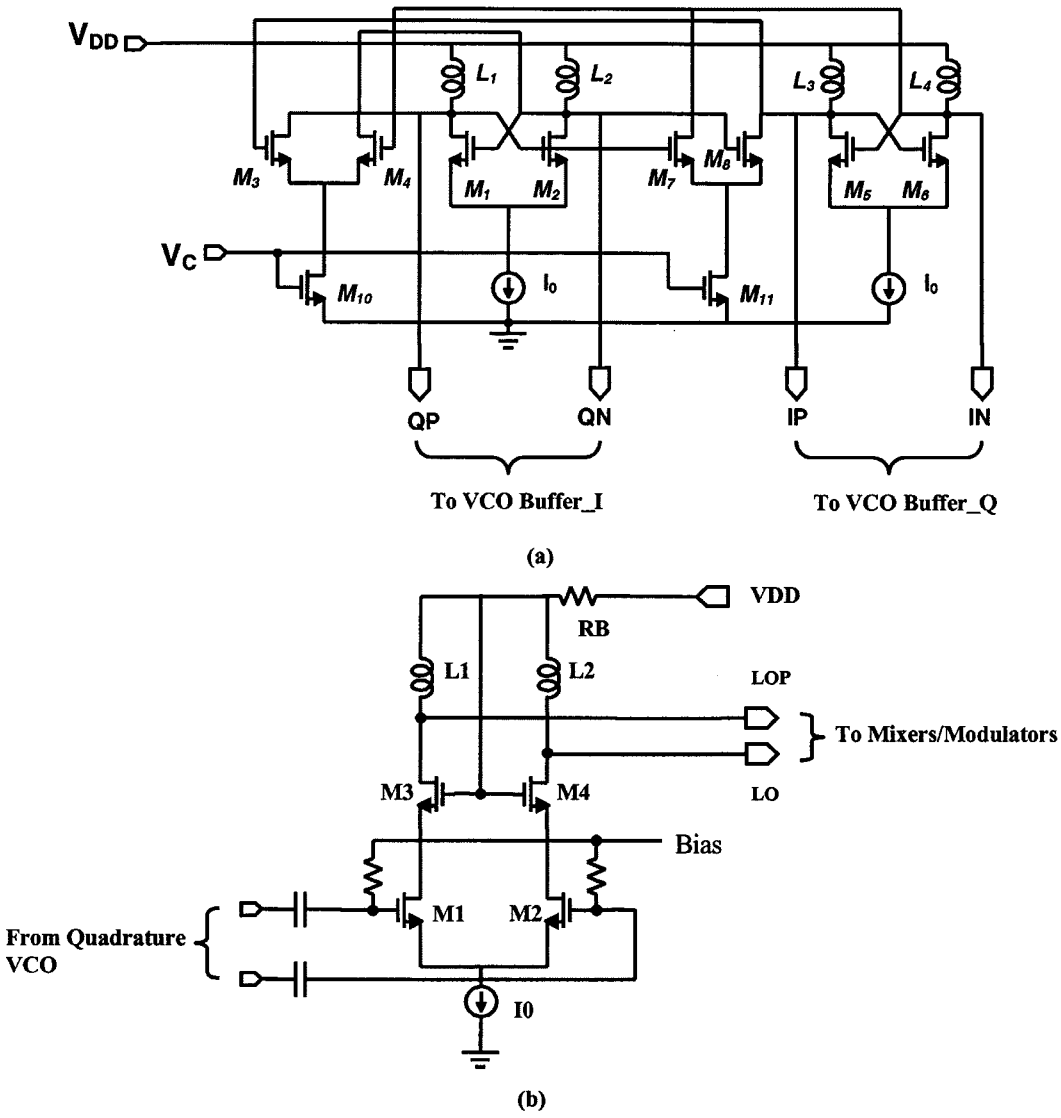


Fig. 5. (a) Quadrature VCO schematic. (b) VCO buffer schematic.

the receive mixer, source-grounded M7–M8, instead of operating then as a source-coupled pair with a tail current source, allows the quad switches to operate with lower supply voltage.

D. Quadrature Modulator and Driver Amplifier

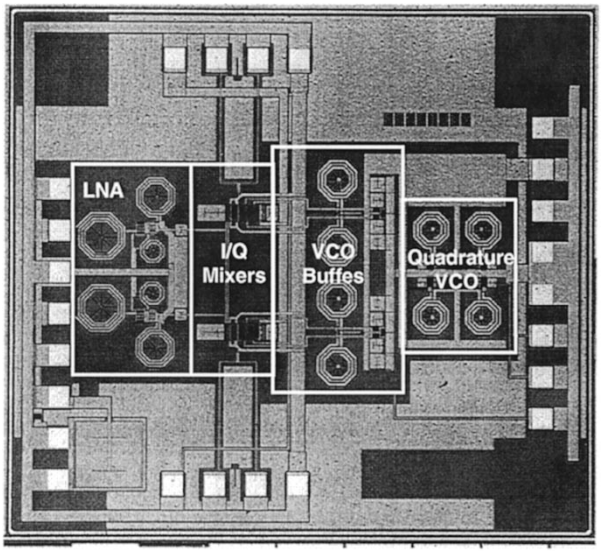
As illustrated in Fig. 4, the outputs of the I and Q modulator are summed in the current domain and are pulled up by 3-nH on-chip inductors L3–L4. The use of L3–L4 not only increases the headroom but also tunes out the parasitic drain–bulk and drain–source capacitance at the summing nodes MOP and MON, yielding a higher voltage swing. The following driver amplifier, M1–4, is a common-source common-gate amplifier with 10-dB power gain when driving a 50-Ω load. M3 and M4 isolate the output impedance transformation network L1–C1 and L2–C2 from the resonators associated with L3–L4 to smooth the output frequency response. Typically, M1 (M2) is biased with 10-mA current to achieve an output power of 3 dBm.

E. Quadrature VCO

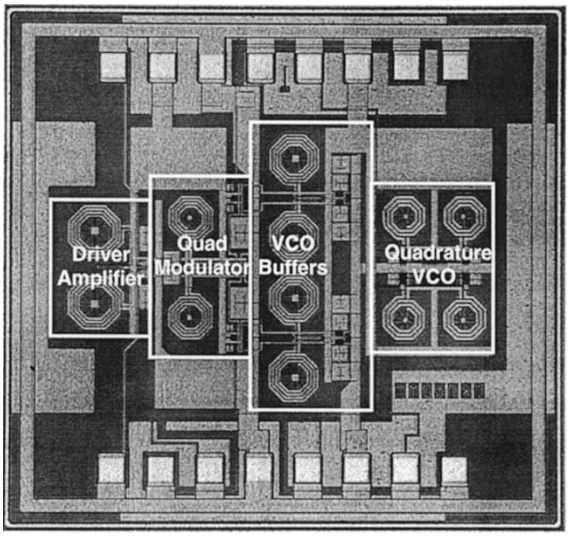
A ring-coupled VCO with differential quadrature outputs IP-IN and QP-QN is shown in Fig. 5(a). It consists of two *identical LC* oscillators M1–2 and M5–6, which inject-lock to each other through coupling stages M3–4 and M7–8. It can be shown that the outputs of two oscillators, QP-QN and IP-IN, always differ in phase by 90°. Furthermore, the synchronous oscillation frequency can be tuned without using the varactor by varying the bias currents in M3–4 and M7–8 via control voltage V_C [5].

F. VCO Buffer

The VCO buffer, shown in Fig. 5(b), shares the same circuit topology as the drive amplifier but is biased with a current source to have better common-mode rejection. Inductors L1–L2 act as loads and tune out the capacitance looking into the mixer/modulator quad switch devices, thus generating high-swing sinusoidal LO drives even with small bias current I0. Resistor RB and I0 set the dc bias voltage supplied to the mixers/modulators.



(a)



(b)

Fig. 6. (a) Receiver chip micrograph. (b) Transmitter chip micrograph.

IV. Measurement Results

The radio transceiver front-end has been fabricated in a 0.25-μm single-poly five-level metal CMOS process. The die photos of the receiver and transmitter ICs are shown in Fig. 6. Their die areas are 2.1 mm $\times$ 1.9 mm and 1.7 mm $\times$ 1.6 mm, respectively. Thick-metal inductors with simulated Q of more than 10 are used where needed. The circuits have been tested on-wafer using high-frequency probes.

The LNA and mixer have been laid out as stand-alone circuits and were tested and characterized individually. External baluns were used to generate differential inputs and to combine differential outputs to single-ended. The cable, balun, and probe losses have been calibrated out. The measured LNA power gain and noise (both under 50-Ω system impedance) performance with operating current are shown in Fig. 7. The LNA achieves an NF of 2.5 dB and 16-dB power gain at 5.15 GHz with 16-mA current drain from a 3-V supply. This is the lowest NF reported to date for a CMOS LNA operating in 5-GHz band. Even at a much lower supply current (4 mA), both the NF (3.5 dB) and power gain (11.6 dB) performance are still quite good. The receiver mixers were also individually characterized. When biased

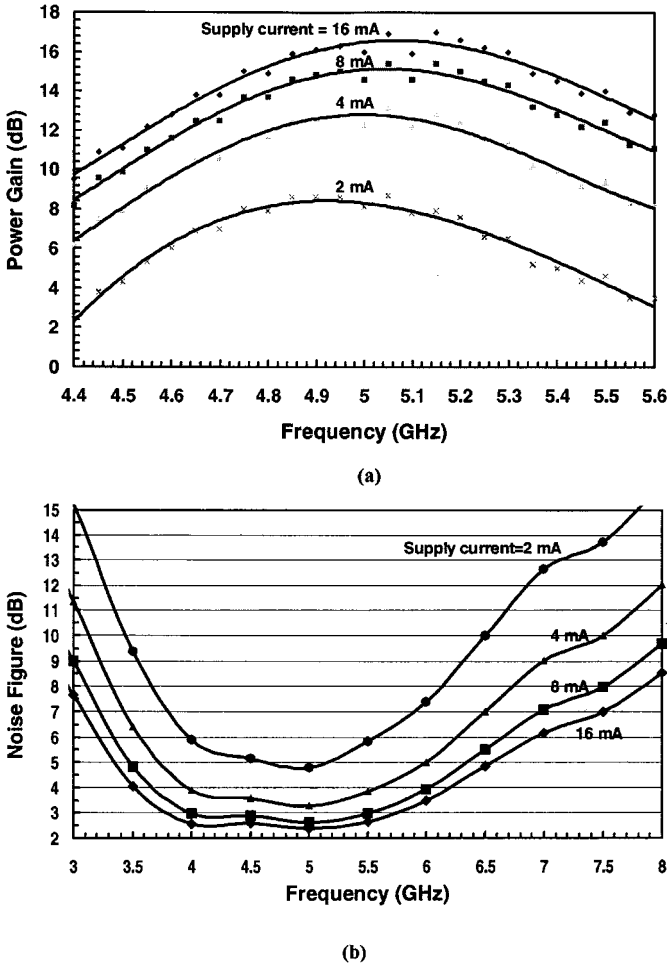


Fig. 7. (a) Measured LNA gain versus frequency. (b) Measure LNA NF versus frequency.

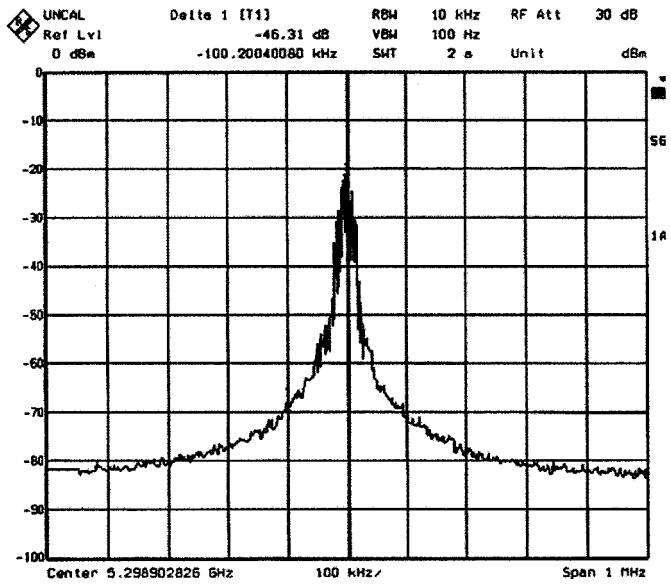


Fig. 8. Measured quadrature VCO phase noise.

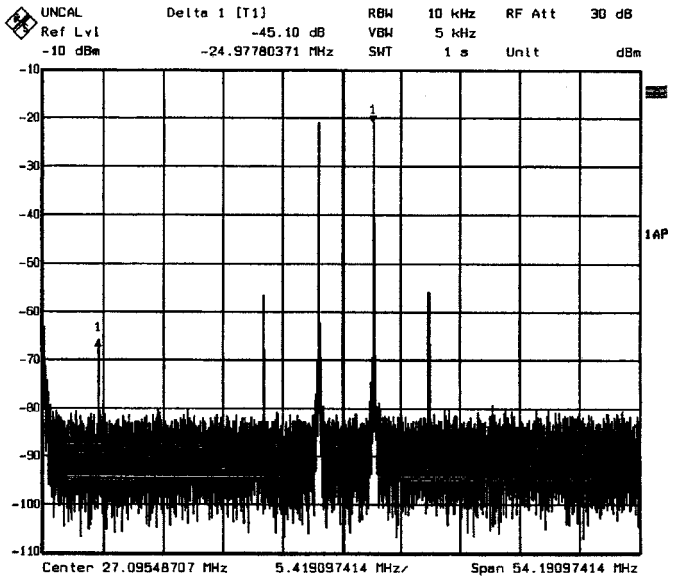


Fig. 9. Measured receiver output spectrum.

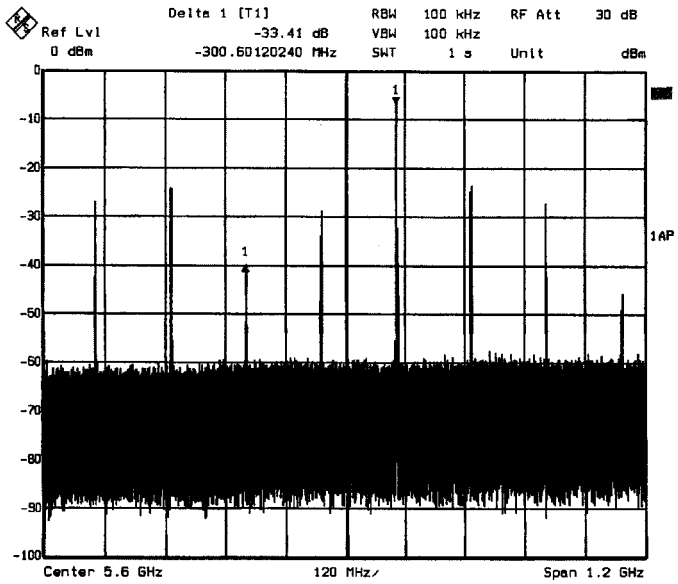


Fig. 10. Measured transmitter output spectrum.

with 12-mA current and driven by +1-dBm LO signal, the mixer has a voltage conversion gain of 13.7 dB, an input 1-dB compression of −5 dBm, an input IP3 of 4.3 dBm, an input IP2 of +41 dBm, and an SSB NF of 12.0 dB. The quadrature VCO covers a wide operating frequency range, from 4.9 to 6.5 GHz. The measured phase noise of the 12-mA quadrature VCO is −86 dBc/Hz at 100 kHz away from 5.3-GHz center frequency, as shown in Fig. 8.

Fig. 9 shows the measured receiver two-tone test output spectrum. The two-tone input signals are at 5.25 and 5.255 GHz with power levels of −29 dBm. The second-order intermodulation product, which is located at 5 MHz, is 45.1 dB below the main signal. This translates to an input-referred second-order intercept point (IP2) of 16.1 dBm for the receive path. Similarly, the input-referred third-order intercept point (IP3) for the receive path is −11.3 dBm.

Fig. 10 shows the measured transmitter output spectrum when the 150-MHz quadrature signals, generated from a 90° hybrid, are applied to the baseband inputs BBI and BBQ in Fig. 1. The VCO frequency is tuned so that the (desired) upper sideband (USB) is at 5.7 GHz while the (undesired) lower sideband (LSB) is at 5.4 GHz. When the baseband input signal is 1.8 V, measured in terms of differential amplitude, the transmitter reaches its output 1-dB compression point at −2.5 dBm. Note that the displayed 1-dB compression point is 4 dB lower due to cable, probe, and balun loss in the test setup. The LSB is 33.4 dB below the desired signal, indicating that the on-chip quadrature VCO produces an I/Q phase error of 2.45° or 0.4-dB amplitude imbalance. The LO leakage, located in the middle of USB and LSB, is 22.4 dB below the desired output. Table I summarizes the measured transceiver performance.

TABLE I
TRANSCEIVER PERFORMANCE

Receiver Performance *(RF=5.25 GHz, LO=5.26 GHz)*	
DSB Noise Figure	**3 dB**
Conversion Gain (50 Ω/1M Ω)	**8.7/18 dB**
Input S11	**-9.4 dB**
Input 1-dB compression	**-21 dBm**
IP2	**16.1 dBm**
IP3	**-11.3 dBm**
LO-RF Leakage	**-60 dBm**
Power Dissipation @ 3V	**114 mW**
Die Size	**4 mm²**
Transmitter Performance *(Baseband=150MHz, LO=5.55 GHz)*	
Output 1-dB compression @5.7 GHz	**-2.5 dBm**
Input 1-dB compression (peak, differential)	**1.8 V/channel**
LO Leakage	**-22.4 dBc**
Sideband Rejection	**-33.4 dBc**
Equivalent Phase Error	**2.45 degree**
Equivalent Amplitude Imbalance	**0.4 dB**
Power Dissipation @ 3V	**120 mW**
Die size	**2.7 mm²**

V. CONCLUSION

A 3-V 5-GHz radio transceiver frond-end chipset with integrated VCO for UNII devices has been implemented in a 0.25-μm CMOS technology. The 5.2-GHz receiver achieves 3-dB double sideband (DSB) NF, 18-dB voltage gain, and −11-dBm input IP3 while dissipating 114 mW. The transmitter delivers −2.5-dBm power to a 50-Ω load at the 1-dB compression point and attains −33.4-dB sideband rejection, all at 5.7 GHz and 120-mW power consumption. The experimental results of the transceiver chipset clearly demonstrate the microwave frequency capability of CMOS technology in the critical areas of gain, NF, linearity, large signal operation, and frequency purity, required in wireless communications applications.

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Eric H. Westerwick (M'00) was born in Pittsburgh, PA, in 1952. He received the E.E.T. degree in electrical engineering from the Pennsylvania State University, Monaca, PA, in 1974, and the B.S. degree in electronic engineering from Monmouth University, West Long Branch, NJ, in 1989. He is certified as an Engineering Technician by the National Institute for Certification in Engineering Technologies.

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